FUZZY CONTROLLED TRANSFORMER-LESS UPFC FOR AC GRID WITH CASCADED MULTILEVEL INVERTERS

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ABSTRACT : This paper proposes transformer-less Unified Power Flow Controller (UPFC) with fuzzy logic controller which can have the capacity to control the parameters of the transmission line and power flow between two interconnected synchronous AC grid. The active power and also the reactive power can be autonomously controlled by the new transformer-less UPFC. Moreover, the system semiconductor gadget appraisals (SSDPRs) of consecutive HVDC system and transformer-less UPFC system are looked at. The expansion of fuzzy logic controller decreases the harmonics in the system. It tends to be discovered that course multilevel inverter based transformer-less UPFC has much lower SDPR when contrasted with MMLC based consecutive HVDC system, showing critical cost sparing when utilize transformer-less UPFC for power flow control. Simulation results based on transformers-less UPFC are obtained in MATLAB-Simulink to approve the analysis.

I. INTRODUCTION

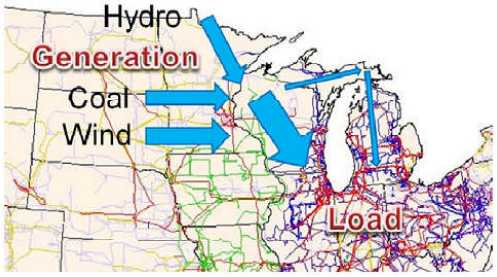
The North American power grid is a confounded work structure. These coincided networks are stuffed and are regularly subject to extreme blockages. One commonplace case is the Michigan Upper Peninsula (UP) grid situation as appeared in Fig. 1 [1]. The Power request is high on south and east side of Lake Michigan. The majority of the power flow takes after the low impedance way south of Lake Michigan; be that as it may, a little, yet critical, bit of power discovers its way through high impedance way in the UP. Because of this circle flow issues, Eastern UP grid is "split" from that of West UP with a specific end goal to forestall overloading of lines/gear and to dispose of under voltage. UP split is essential for 95% time of a year. Subsequently, it's hard to perform planned maintenance, to control voltage in eastern UP. To tackle this issue, the East UP will associate with Lower Peninsula (LP) through the voltage source converters (VSC) consecutive high voltage direct present (HVDC) system [1]. Generally, HVDC transmission systems have been utilized for long separation power transmission and interconnecting asynchronous grids. As of late, VSC based consecutive HVDC system was additionally connected to interconnect synchronous grids for power flow control [1], [2]. VSC based consecutive HVDC system has extra advantages, for example, the capacity to dark begin and the capacity to utilize either converters to function as STATCOMs in an islanded case [1].

Be that as it may, the main downside of the consecutive HVDC system is the prerequisite of two full-power rating converters to interface two grids, which fundamentally diminishes the system productivity and builds the cost. As of late, a course multilevel inverter (CMI) based secluded transformer-les unified power flow controller (UPFC) has been proposed [3], which has a few points of interest, for example, entire transformer-less, light weight, high productivity, high unwavering quality, ease, and quick dynamic reaction.

In this paper, the transformer-less UPFC is connected to interconnect two synchronous AC grids for autonomous active/reactive power control. Initial, a correlation of the total semiconductor gadget power appraisals (SDPR) between various power flow arrangements (mainly consecutive HVDC and transformer-less UPFC) is dissected. The investigative results will demonstrate that the SDPR of transformer-less UPFC could be 8 times littler than the consecutive HVDC system when utilized for power flow control. The comparing system configuration, power flow and dc-link voltage control of transformer-less UPFC will be presented and tentatively confirmed at 13.8 kV/2MVA test setup.

II. OPERATION PRINCIPLE OF THE TRANSFORMER-LESS UPFC

Fig. 2 demonstrates the configuration of the new transformer-less UPFC. As appeared in Fig. 2 (a), the transformer-less UPFC comprises of two course multilevel inverters (CMIs), one is series CMI, which is directly associated in series with the transmission line; while the other is shunt CMI, which is associated in parallel to the sending end after series CMI. Each CMI is made out of a series of cascaded H-bridge modules as appeared in Fig. 2 (b) [3]. Fig. 3 demonstrates the phasor diagram for the transformer-less UPFC, where 0 JG S V and JG R V are the first sending-end and getting end voltage, separately. Here, 0 S V JG is lined up with genuine pivot, which means phase edge of 0 JG S V is zero. The series CMI is controlled to create a coveted voltage JG C V for acquiring the new sending-end voltage JG S V , which thusly, controls active and reactive power flows through the transmission line. Meanwhile, the shunt CMI infuses a present G P I to the new sending-end bus to make zero active power into both CMIs, i.e., to make the series CMI current G C I and the shunt CMI current G P I be opposite to their voltages JG C V and JG S V , individually. Thus, both series and shunt CMIs just need to give the reactive power. In such a way, it is conceivable to apply the CMIs to the transformer-less UPFC with drifting dc capacitors for H-bridge modules.



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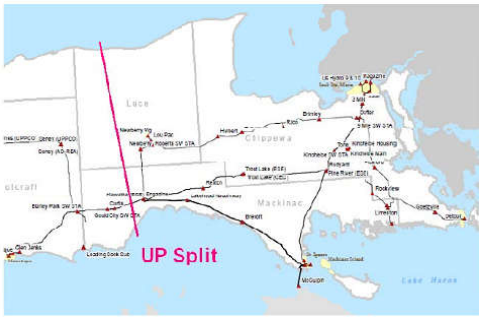

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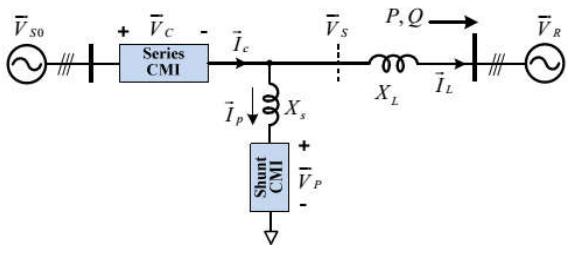
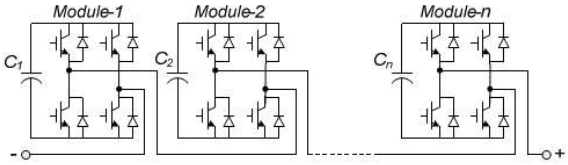
Fig. 1. Michigan UP grid scenario, (a) Illustration of power flow in Upper Midwestern US, and (b) Eastern UP transmission system with split



(a)



(b)

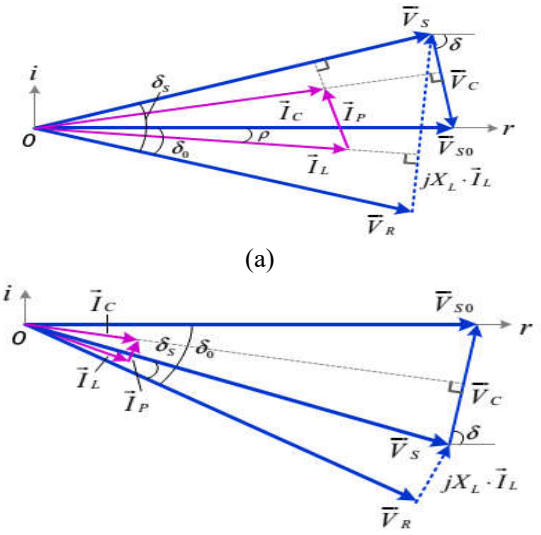
Fig. 2. New transformer-less UFPC, (a) System configuration , (b) One phase of the cascaded multilevel inverter.

For the system without UPFC compensation or $\overline{V_C} = 0$the original active power P_0 and reactive power $Q_0$are decided as

$$P_o=\frac{V_{S0}V_R}{X_L}\sin\delta_0\ ,\quad Q_0=\frac{V_{S0}V_R\cos\delta_0-V_R^2}{X_L} \qquad (1)$$

It shows that the power flow is chosen by the parameters of voltage amplitude 0 S V and R V, line impedance L X and phase edge distinction 0 δ between sending-end voltage and accepting end voltage. As a rule, the active power is more identified with phase edge and the reactive power is more identified with the voltage amplitude. At the point when UPFC is connected for interconnecting synchronous AC grids, two unique situations are considered: 1) UPFC connected to build the power flow: the first phase edge distinction 0 δ between 0 JG S V and R V JG is little. Power/current flow can be controlled to a higher esteem when the phase edge diverse is controlled from δ0 to δs by UPFC. The comparing phasor diagram is appeared in Fig. 3 (a). 2) UPFC connected to diminish the power flow: For this situation, the first phase point distinction δ0 between 0 JG S V and R V JG is huge, e.g. 30°. Hence, it is difficult to close this line directly; something else, embrace current/power will experience the line to cause the overload. Here, series voltage VC JG is infused to alter the phase edge 0 δ to s δ with a littler esteem, the power flow through the line at that point is controlled to a constrained esteem.

The comparing phasor diagram is appeared in Fig. 3 (b).



(a)

(b)

Fig. 3. Illustration of UPFC power flow regulation, (a) UPFC applied to increase the power flow and (b) UPFC applied to decrease the power flow.

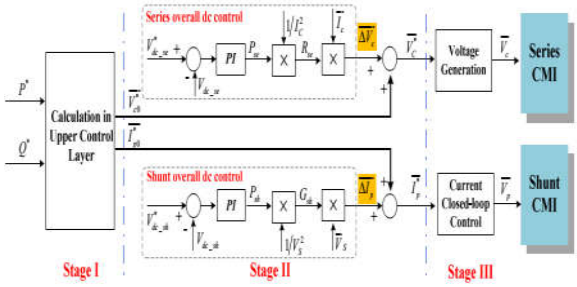


Fig. 4. Overall control diagram of the transformer-less UPFC.

It is desired to design a control system, which can independently regulate the active power Pand reactive Qin the line, at the same time, maintain the capacitor voltages of both CMIs at the given value. Fig. 4 shows the overall control system, which is divided into three stages, i.e. stage I to stage III [9].

Stage I: the calculation from $\frac{P^*}{Q^*}$to$\overline{V_{CO}^*}$ and $\overline{I_{PO}^*}$. As mentioned before, the$\overline{V_{CO}^*}$is the voltage reference for series CMI, which is generated according to the transmission line power command, while$\overline{I_{PO}^*}$ is current reference for shunt CMI, which is used to keep zero active power for both CMIs.

Stage II: overall dc-link voltage regulation. In order to control dc-link voltage with better robustness, two variables Δ $\overline{V_C}$and $\Delta\overline{I_P}$were introduced for the independent dc-link voltage regulation of series CMI and shunt CMI, respectively, as shown in Fig. 4 (a). In this figure, $V_{dc\_sh}^*$ and $V_{dc_se}^*$are dc voltage references for shunt and series CMIs, respectively; V_{dc_sh} and $V_{dc_se}$are the averaged dc feedback of shunt and series CMIs, respectively. For the series CMI, P_{se} is the output of overall dc-link voltage regulation loop, R_{se} is then calculated by dividing P_{se} by I_C^2 (square of rmsvalue of series CMI current), finally $\Delta\overline{V_C}$ is the product of R_{se} and series CMI current $\overline{I_C}$. Obviously, the introduced $\Delta\overline{V_C}$is always in phase with series CMI $\overline{I_C}$, which can be regarded as active-voltagecomponent. Basically, R_{se} is the equivalent resistance of series CMI, and the dc-link can be balanced when se Pis equal to P_{loss} (total power loss of series CMI). For the shunt CMI, $\Delta\overline{I_P}$is introduced for the dc-link voltage control in a similar way.

Stage III: voltage and current generation for series and shunt CMI, respectively. For series CMI, output voltage could be directly generated from the reference$\overline{V_c^*}$by fundamental frequency modulation (FFM). While for shunt CMI, decoupling feedback current control is used to control output current to follow the reference current$\overline{I_p^*}$, as shown in Fig. 4 (c). The transformer-less UPFC modulation and control method has been introduced in [9] in detail.

III. FUZZY LOGIC CONTROLLER

Unlike Boolean logic, Fuzzy Logic (FL) allows states (membership values) between 0 and 1. Its major features are the use of linguistic variables rather than numerical variables. Linguistic variables, defined as variables whose values are sentences in a natural language (such as small and big), may be represented by fuzzy sets. The general structure of an FLC is represented in Fig. 5.

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

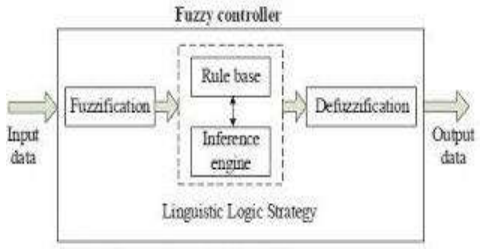


Fig. 5: Basic configuration of FL controller

TABLE I: FUZZY RULES

$e/\Delta e$	LP	MP	SP	S	SN	MN	LN
LP	PB	PB	PB	PM	PM	PS	Z
MP	PB	PB	PM	PM	PS	Z	NS
SP	PB	PM	PM	PS	Z	NS	NM
S	PM	PM	PS	Z	NS	NM	NM
SN	PM	PS	Z	NS	NM	NM	NB
MN	PS	Z	NS	NM	NM	NB	NB
LN	Z	NS	NM	NM	NB	NB	NB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (2)$$

$$CE(k) = E(k) - E(k-1) \quad (3)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output.

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (4)$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable. A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible.

IV. SSDPR COMPARISION BETWEEN BACK TO BACK HVDC SYSTEM AND TRANSFORMER-LESS UPFC SYSTEM

Semiconductor Device Power Rating (SDPR) means that how much total silicon zone is required for the semiconductor devices, which is a standout amongst the most essential pointers to gauge the inverter/converter cost. The individual gadget power rating is characterized as the result of voltage and current worry of the semiconductor gadget, the inverter/converter SDPR is the summation of individual gadget power rating [4], [5]:

$$SDPR = \sum_{k=1}^{n} V_k I_k , \quad (1)$$

Wheren is the total number of semiconductor devices in the inverter/converter, and V_k , I_k are the voltage and current stress of the k_{th} semiconductor device (e.g. IGBTs) respectively. The overall system SDPR (SSDPR) is then decided by

$$SSDPR = SDPR*\eta \quad (2)$$

Where,η represents the inverter/converter rating with respect to system rating. For instance, the

MVA rating of a series Flexible AC Transmission System (FACTS) device will often be a small fraction of the throughput line MVA, considering the per unit line impedance is usually a small fraction of the line [5]-[7].

A.SDPR of the Basic

Three-phase Converter Fig. 6 (a) demonstrates the topology of essential three-phase inverter/rectifier. The present worry of the IGBT is √2Ig , where Ig is the rms estimation of output current. The voltage push is equivalent to the dc-link voltage, and its base esteem is √2Vg when SVPWM or SPWM with 3 rd harmonic infusion is utilized with maximum adjustment record, where the Vg is the rms estimation of line-to-line grid voltage. Consequently, the general SDPR for each of the 6 IGBTs is

$$\text{SDPR} = 6.\sqrt{2}I_g.\sqrt{2}V_g = 12\ V_gI_g \quad (3)$$

In all analysis, the line to line AC voltage and line currents are considered as the base values. Hence, the SDPR for a three phase inverter or rectifier is

$$\text{SDPR} = 12 \text{ pu} \quad (4)$$

Hence, the SDPR for a three phase inverter/rectifier is 12 pu when the power exchange between inverter and AC grid is equal to 1 pu.

B. SDPR of Half-bridge MMLC

Fig. 6 (b) demonstrates the topology of half-bridge based particular multilevel converters (MMLC), which is the most prominent VSC topology for HVDC system [8]. Here, g Vis the line-to line AC voltage, arm I is the current through the upper arm, DC I *f*is the current through the DC link, and g I is the current through AC grid. Contrasting the essential cell (half bridge) of the MMLC to the fundamental cell (a solitary switch) of the essential three-phase converter appeared in Fig. 5 (an), it very well may be observed that the quantity of IGBTs in the fundamental cell is multiplied. So also, the base dc voltage for a given AC voltage is √2Vg, which is basically the voltage worry of the switches. As indicated by the current and voltage deductions in [8], the current through each arm of the MMLC circuit is given as

$$i_{arm} = i_g/2 + i_g/3 \quad (5)$$

Considering unity power factor and the power balance between dc side and ac side, we have

$$P = \sqrt{3}V_gI_g = V_{dc}I_{dc} \quad (6)$$

Where $V_{dc}=\sqrt{2}V_g$. Then we can derive the arm current from (5) and (6) as

$$i_{arm} = \left(\frac{1}{2} + \frac{1}{\sqrt{6}}\right) I_g \quad (7)$$

The arm current $i_{arm} \approx i_g$ with consideration of circulating current, As a result, the current stress of each of the IGBTs is considered as $\sqrt{2}I_g$. Therefore, the overall SDPR for all 12 IGBTs is

$$\text{SDPR} = 12.\sqrt{2}I_g.\sqrt{2}I_g = 24 \text{ pu.} \quad (8)$$

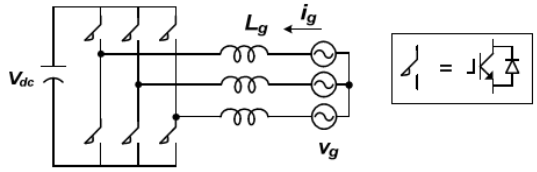
It is notable that the SDPR of Half-bridge MMLC is independent of the number of modules. For instance, if the number of half-bridge modules in each arm is doubled, the overall SDPR still remains the same.

C. SDPR of the Cascade Multilevel Converter

Fig. 6 (c) demonstrates the topology of cascaded multilevel inverter (CMI). Contrasted with the topology of fundamental three-phase converter appeared in Fig. 6 (a), the quantity of IGBTs of CMI is multiplied, and each IGBT has same current rating yet 50% of the voltage rating.

$$\text{SDPR} = 12.\sqrt{2}I_g.\frac{\sqrt{2}}{2}V_g = 12\text{pu.} \quad (9)$$

It should be noted again that the SDPR for CMI is independent of number of H-bridge modules. Increasing the number of H-bridge modules for CMI doesn't help to reduce the SDPR.



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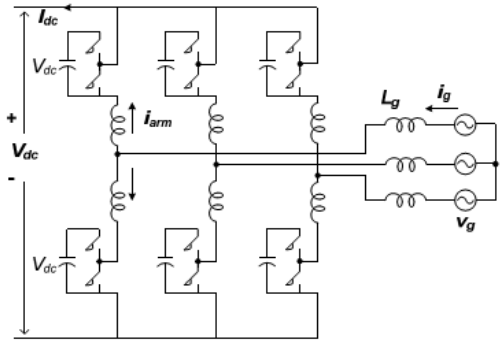

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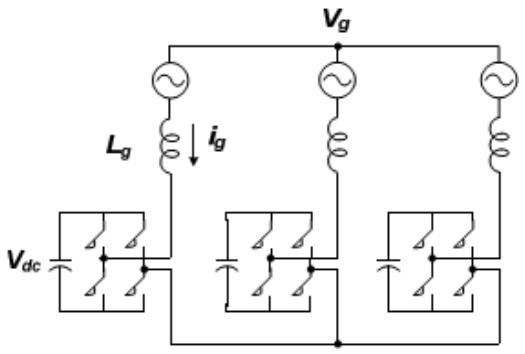


(c)

Fig. 6. Different inverter/converter topologies, (a) basic three-phase inverter/ rectifier, (b) half-bridge MMLC, and (c) cascade multilevel inverter (CMI).

D. SSDPR Comparison between Back to Back HVDC System and Transformer-less UPFC System

Keeping in mind the end goal to perform power flow control, two MMLC converters as appeared in Fig. 6 (b) must be associated in a consecutive way. Along these lines, the SSDPR for the consecutive MMLC based HVDC system is

$$SSDPR_{HVDC}=2.24 \text{ pu} =48 \text{ pu} \quad (10)$$

For a UPFC based Power flow control system, considering 30^0 phase angle difference between two synchronous grids $\overrightarrow{V_{S0}}$ and$\overrightarrow{V_R}$, the total UPFC rating is 1pu as analyzed in [3], [9], therefore, the SDPR for a transformer-less UPFC is calculated as

$$SSDPR_{UPFC} = 1.12 \text{ pu} =12 \text{ pu} \quad (11)$$

which is not as much as ¼ of consecutive HVDC system. It ought to be noticed that the transformer-less UPFC can likewise control power flow without shunt CMI, for this situation, UPFC works simply like the Static Synchronous Series Compensator (SSSC). The system rating is 0.5 pu without shunt CMI, and the general SDPR becomes0.5*12 = 6 P.U which is 8 times littler than that of consecutive HVDC system. In synopsis, the course multilevel inverter based transformer-less UPFC has much lower SDPR when contrasted with MMLC based consecutive HVDC system, showing huge cost sparing when utilized for power flow control.

V. SIMULATION RESULTS

A 13.8-kV/2-MVA transformers-less UPFC model has been created to approve the UPFC power flow control functionality. The test setup is appeared in Fig. 7, and the main system parameter for the model is given in TABLE I. In Fig. 7, the sending-end voltage 0 S V JG has indistinguishable amplitude from accepting end voltage R V JG (13.8 kV), yet 30° phase driving. This 30° phase driving is presented by the Y/ẵ transformer. As said previously, it is difficult to directly close this line without UPFC pay, generally enormous current/power will flow through the line because of the 30-degree voltage distinction. At the point when the new transformer-less UPFC is connected to interconnect these two grids, it gives finish adaptability and controllability, which means the present/power can be controlled to any coveted esteem.

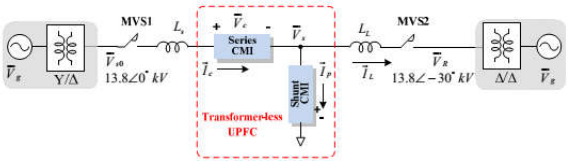


Fig. 7. The system configuration for 13.8-kV/ 2-MVA UPFC test setup.

TABLE I. System Parameters of the Transformer-less UPFC Test Setup

Parameters	Value
Rated power	2 MVA
V_{S0} (Phase-phase rms)	13.8 kV ∠0°, 60 Hz
V_R (Phase-phase rms)	13.8 kV ∠-30°, 60 Hz
Equivalent line inductance L_s	0.12 *pu*
Equivalent line inductance L_L	0.36 *pu*
Series CMI per phase	8 H-bridge modules
Shunt CMI per phase	20 H-bridge modules
Nominal Series CMI V_{dc}	450V~600V
Nominal Shunt CMI V_{dc}	550V
DC capacitance of each CMI	2350 μF

An UPFC can just control the size and phase edge of the infused voltage progressively to direct the active and reactive power flow in the line to fulfill load request and system working conditions. It is prominent that the UPFC can control, at the same time or specifically, every one of the parameters influencing power flow in the transmission line (i.e., voltage extent, impedance, and phase point). Here the series CMI is utilized as impedance compensator, while the shunt CMI is utilized as reactive power compensator. The shunt CMI will remunerate the line reactive power and to ensure the reactive power for both side grids are the same. Along these lines, the infused series CMI voltage C V JJG and the shunt CMI current P I JJG references are figured as takes after:

1) δ_S is decied firstly according to the system power command;

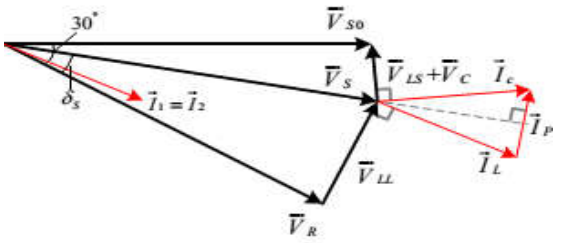
2) $\overline{V_C}$is assumed in phase with $\overline{V_{LS}}$, of course the following equation holds: $\overline{V_{SO}} = \overline{V_S} + \overline{V_C} + \overline{V_{LS}}$;

3) The amplitude of $\overline{V_S}$is then decided to guarantee the phase angle of $\overline{V_C}$ (or$\overline{V_{LS}}$;) leads $\overline{V_S}$by 105º.

In such a case, it can be proven that the phase angle of $\overline{V_{LL}}$;would lead $\overline{V_S}$by 75º.Since the currents of $\overline{I_C}$and $\overline{I_L}$lag their voltages by 90º, the phase angle of $\overline{I_C}$ would lead $\overline{V_S}$by 15º, while the phase angle $\overline{I_L}$of would$\overline{V_S}$ lag by 15º.

4) The shunt current will be chosed to guarantee current amplitude of $\overline{I_C}$ is equao to that of $\overline{I_L}$, as a result, the shunt current $\overline{I_P}$would be perpendicularwith S V JJG .

Fig. 8 shows the phasor diagram for different operating points of UPFC power flow control, two cases are shown here: (a) Case A: δ_S =22°and (b) Case B: δ_S =7°.



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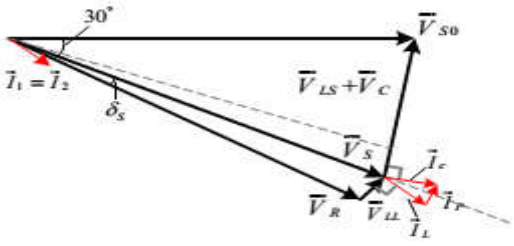


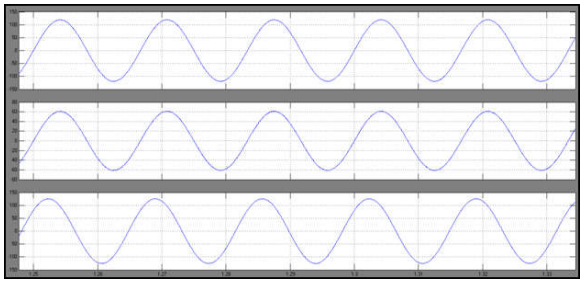
(b)

Fig. 8. Phasor diagram for different operating points of UPFC power flow control,

(a) Case A: δ_S =22 °and (b) Case B: δ_S =2°.

Fig. 9 demonstrates the test waveform of transformer-less UPFC worked at Case A: δS =22°: (a) transmission line current I_{La}, sending-end current Ica and shunt current I_{pa}, and (b) V_{inv_ab} and I_{La}, where the V_{inv_ab} is the voltage of series CMI output voltage V_{C_ab} in addition to shunt CMI output voltage V_{P_ab}.The showed line voltage V_{inv_ab} is the voltage estimated at the secondary of the potential transformer (PT) with turn ratio is 120 41:1 ×. For this situation, because of the expansive estimation of power edge δ_S , the comparing line current I_L=84 An, active power P =1.8MW , and reactive power Q = 0.6MVar. What's more, Fig. 10 demonstrates found the middle value of dc link voltage for both series and shunt CMIs, where the dc voltage reference for series CMI is 450 V and voltage reference for shunt CMI is 550 V. The dc voltage references are kept the balance file (MI) of inverter close solidarity to accomplish the most reduced total harmonic distortion (THD) of output voltage. As can be seen from the trial waveform, all the dc voltages are very much controlled and maintained inside ±5% of their ostensible dc esteem.

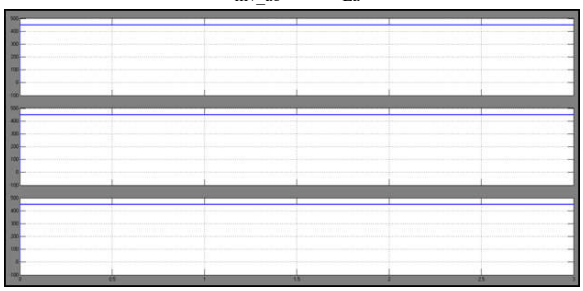
Fig. 11 demonstrates the trial waveform of transformer less UPFC worked at Case B: δ_S =2°: (a) transmission line current I_{La}, sending-end current Ica and shunt current I_{pa}, and (b) V_{inv_ab} and I_{La}. For this situation, since the power S δ is lessened fundamentally, the come about line current I_L=7 An, active power P = 0.14MW, and reactive power Q =0.07MVar. Moreover, Fig. 12 demonstrates found the middle value of dc link voltage for both series and shunt CMIs. Since substantially higher output voltage of series CMI is expected to remunerate the phase edge distinction, the dc voltage reference for series CMI changed from 450 V to 600 V, and the voltage reference for shunt CMI remains at 550 V. Fig. 13 demonstrates the transmitted P/Q between working points An and B. The transformer-less UPFC can easily control the power through the transmission line from low (5%) to high (100%), or the other way around.



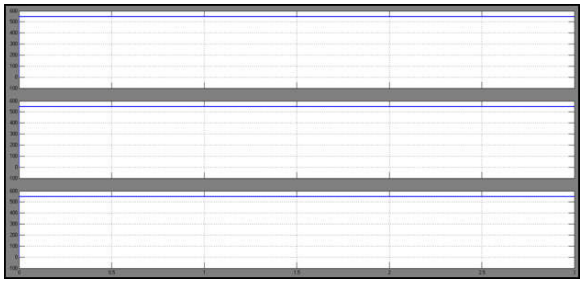
(a)

(b)

Fig. 9. Simulation waveform of UPFC operating at Case A: δ_S =22°: (a) transmission line current I_{La}, sending-end current I_{ca} and shunt current I_{pa}, and (b) V_{inv_ab} and I_{La}.

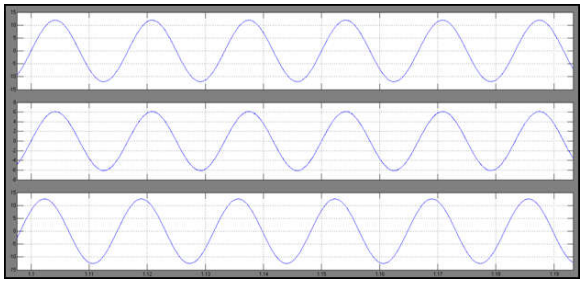


(a)

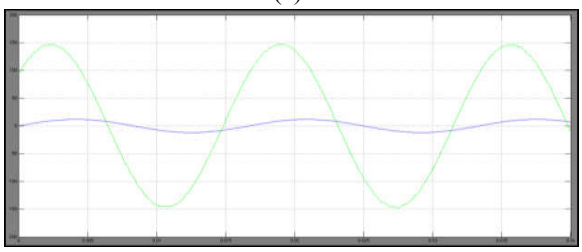


(b)

Fig. 10. Simulation Results of average dc capacitor voltage of (a) series CMI and (b) shunt CMI, operating at Case A

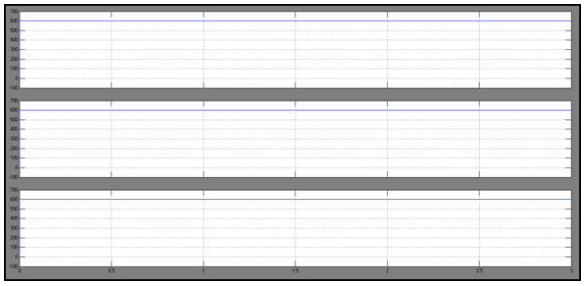


(a)

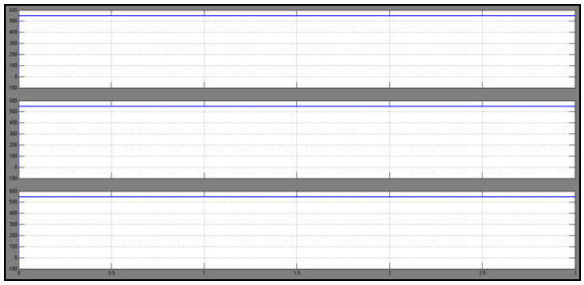


(b)

Fig. 11. Simulation Results of UPFC operating at Case B: 2 S δ =°: (a) transmission line current ILa, sending-end current Icaand shunt current Ipa, and (b) Vinv_aband ILa.



(a)



(b)

Fig. 12 Simulation Results of average dc capacitor voltage of (a) series CMI and (b) shunt CMI, operating at Case B.

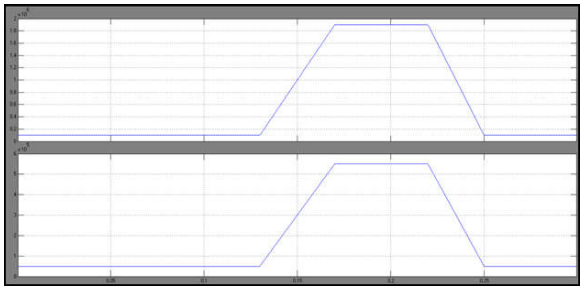


Fig. 13. Experimental results of P/Q between operating points A and B.

VI. CONSLUSIONS

In outline, the transformer-less UPFC is proposed for interconnection between two synchronous grids. The active power and additionally the reactive power can be autonomously controlled by the series and shunt cascaded staggered inverters in transformer-less UPFC. The controlling of new transformer less UPFC has progressive improvements: 1) to a great degree bring down switching losses and more prominent productivity of CMI by utilizing FFM procedure; 2) whole UPFC functions are accomplished and 3) snappy dynamic reaction of the

system. The operation and execution of new transformerless UPFC have been broke down by simulink demonstrate. Contrasted with HVDC answer for interconnecting two synchronous grids, the transformer-less UPFC has much lower system rating, demonstrating noteworthy cost sparing.

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