Design and Analysis of Low Power MTCMOS using SRAM cell

[1]Dr.S.A.Sivakumar, [2]S.Geetha

[1]Assistant Professor, Department of ECE, Info Institute of Engineering, Coimbatore, Tamilnadu.

[2]PG Scholar, Department of ECE, Info Institute of Engineering, Coimbatore, Tamilnadu.

[1]siva3cool@gmail.com, [2]20geetha25@gmail.com

Abstract

A rapid growth of portable battery operated devices has made low power IC design a priority in recent years. Conventional SRAM cell designs are power hungry and poor performers in this new fast mobile computing. In this paper, low power SRAM cell designs have been analyzed for power consumption and write power delay. Gated VDD and MTCMOS design techniques have been employed to reduce the power consumed by the SRAM cell. These designs are compared with the conventional 6T SRAM cell. The result show that the MTCMOS based SRAM cell is the best performer in terms of power consumption and write delay. It is less power than the conventional 6T SRAM cell. Furthermore, the MTCMOS based SRAM cell is faster than the conventional 6T SRAM cell. The Gated VDD SRAM cell also less power than the conventional 6T SRAM cell and is faster than the conventional 6T SRAM cell.

Keywords: Low Power SRAM; Gated VDD SRAM Cell; MTCMOS; MTCMOS SRAM Cell; 6T SRAM; Power Reduction in SRAM Cell.

1. Introduction

The rapid development and usage of portable devices, battery life is a major concern. As new devices are developed like smart watches, small sensor nodes, wireless communication units, etc. Energy efficient hardware architecture is required. Random Access Memory (RAM) chips are used virtually in every digital system.

Static Random Access Memory (SRAM) cells don't require constant refreshing to retain its contents as long as power is supplied to the cell. SRAM's integration with standard CMOS technology gives it the opportunity to become the highest area consumer on System on Chips (SoCs).

As the current technologies are scaling down to deep submicron levels, leakage power is a major source of power consumption. Furthermore, majority of the transistors on a chip sit in the SRAM unit. Since cache memory uses array architecture, power reduction in a single SRAM cell can contribute to huge power savings in the overall system.

The conventional 6 transistor (6T) SRAM cell is widely used primarily because of its simple design. The 6T SRAM cell is a good performer in terms of delay and power. The analysis of the conventional 6T SRAM architecture good performer shows a lot of room for improvement in terms of power consumption.

Extensive research has been performed on 6T SRAM cells to improve delay and power consumption so it can be adopted widely in industry. The total energy consumption of a SRAM array can be modelled as: $E_{(Switching)}$ and $E_{(leakage)}$.

E (Switching) represents the energy consumed in switching activities (read and write operations) and represents the static energy consumption due to the leakage current in the SRAM cell. It has analyzed various other SRAM architectures like 7T, 8T and a novel 9T design, the overall complexity of these circuits compared to the conventional 6T SRAM cell makes it more difficult to implement and ensure stable operation. Multi Threshold CMOS (MTCMOS) technique has been applied to a 7T SRAM cell achieving promising results in terms of power reduction.

In a 10T SRAM cell is designed achieving high Static Noise Margin (SNM) and a power reduction compared to the conventional 6T SRAM cell. The major drawback with this design is the increased area. When implementing this design in an array, due to the huge multiplying factor, the area of the overall memory chip increases. It explores a 9TSRAM cell which includes Stacking and Dual Threshold Voltage implementations to reduce leakage power.

In a two SRAM cells are presented: one structure using NMOS pass transistors to reduce gate leakage current and the other structure using PMOS pass transistors. Additionally, Dual Threshold Voltage technology with forward body biasing is used, reporting a considerable reduction in power with a very slight access time degradation.

It presents various power reduction techniques in CMOS circuits concluding MTCMOS as one of the best techniques to combat leakage power. A 10T SRAM cell using the Column Line Assist (CLA) scheme shows considerable area reduction compared with other 10T designs and improved delay. Low leakage SRAM cells have been developed using Upper Self-Controllable Voltage Level (SVL) and Lower SVL.

In this paper, various SRAM cells have been designed and analyzed for delay and power consumption. Gated VDD and MTCMOS design techniques have been used to compare the delay and power parameters with those of the conventional 6T SRAM cell.

2. Conventional 6T SRAM Cell

The conventional 6T SRAM cell uses two cross coupled inverters and two access transistors as shown in Figure 1.These access transistors connect the cell to the outside. The inverters are the storage element and reinforce the data bit within the cell as long as the power is supplied (VDD). P1, P2 are PMOS transistors and N1, N2, N3, N4 are NMOS transistors. N3 and N4 are the access transistors (or pass transistors) connecting the cell to the Bit Lines (BL and BL). The different modes of operation of the SRAM cell are detailed below

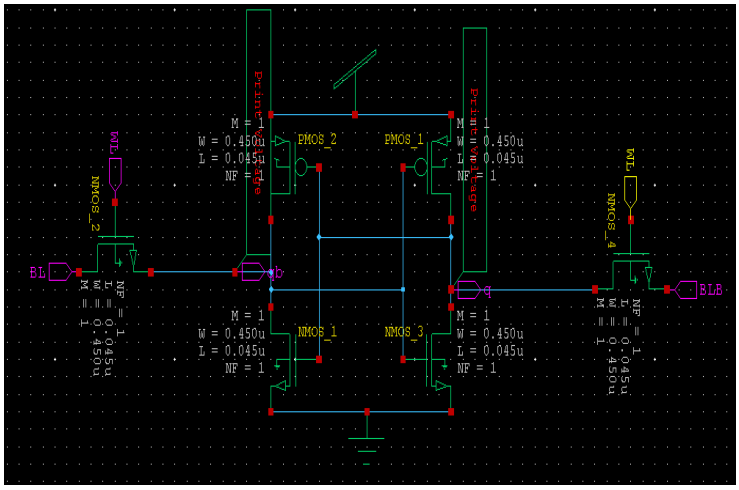

Figure 1. Conventional 6T SRAM cell

2.1 Standby/Hold Mode

When the Word Line (WL) is at logic '0', the access transistors N3 and N4 disconnect the cell from the Bit Line(BL and BL).The two cross coupled inverters in the cell continue to reinforce the data bit present in the cell as long as power is supplied(VDD). The current drawn in this mode from VDD is termed as standby current.

2.2 Write Mode

For a write operation, the Word Line (WL) is set to logic '1' enabling the access transistors N3 and N4 thereby connecting the cell to the outside of (BL and BL). The contents from the Bit Lines (BL and BL) are then transferred into the cell via the access transistors. After a successful write operation, the Word Line (WL) is set to logic '0'. For example, to write logic '0' into the cell, initially BL is set to logic '0' and BL is set to logic '1'. The Word Line (WL) is then set to logic'1' thereby allowing the access transistors to pass the logic value from (BL and BL) into the cell. After the data bit is successfully written into the cell, the Word Line (WL) is set to logic '0' thereby disconnecting the cell from the outside(BL and BL).

2.3 Read Mode

To read the data bit present in the cell, Bit Lines (BL and BL) are initially pre charged to VDD i.e. logic '1'. The Word Line (WL) is then enabled by setting it to logic '1'. Depending on the data bit stored in the cell, a Bit Line (BL or BL) gets discharged slightly (and slowly) via an access transistor and pull down transistor thereby developing a differential voltage drop between the Bit Lines (BL and BL).This small differential voltage drop across BL and BL is then detected by a Sense Amplifier which determines the data bit stored in the cell. Charging and Discharging of large capacitive loads is done by the Sense Amplifier. The higher sensitivity of the Sense Amplifier, the faster the read operation. However, the differential voltage should not be too large as it could flip the state of the cross coupled inverters.

3. Power Reduction Techniques for SRAM Cell

Two important and effective power reduction techniques are employed: Gated V_{DD} and MTCMOS. Detailed discussions of the two methods are presented below.

3.1 Gated V_{DD}

This technique introduces a control mechanism which can disable the supply voltage (VDD) when the SRAM cell is not in use thereby eliminating any leakage current. It reduces the leakage power dissipation by a great amount. In order to achieve this control mechanism, a High Threshold Voltage (High Vt) transistor is introduced in the supply (VDD) or the ground path of the SRAM cell while modelling all other transistors as Low Threshold Voltage (Low Vt) transistors. Low Vt transistors are used as they switch faster than High Vt transistors. This makes the SRAM cell operate fast. This configuration results in optimum power consumption and delay.

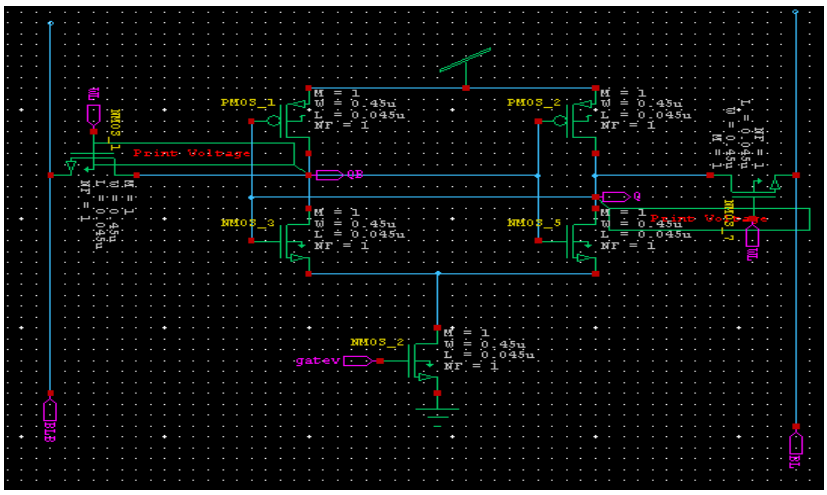

Figure 2. Gated VDD SRAM cell

Figure 2 shows a Gated VDD SRAM design. The 'Gated V_{DD} Control' signal is used to turn on or turn off the SRAM cell. The primary advantage of this technique is the maintenance of system performance even when supply voltage and threshold voltages of the transistors are reduced.

3.2 MTCMOS (Multi Threshold CMOS)

In this technique uses transistors with multiple threshold voltages to optimize delay and power. Low Vt transistors switch faster but have higher static power leakage and High Vt transistors reduce static power leakage but switch slower. MTCMOS design techniques used to design the circuits to optimize the power and delay without incurring penalties.

The most common implementation of MTCMOS to reduce leakage power uses sleep transistors. With the help of sleep transistors, virtual power rails are created which supply the logic. High Vt sleep transistors are used to connect the physical power rails to the virtual power rails. These transistors are turned on in active mode and off in sleep mode by the Clock signal. These sleep transistors help reduce static leakage power by a great amount when the SRAM cell is not in use.

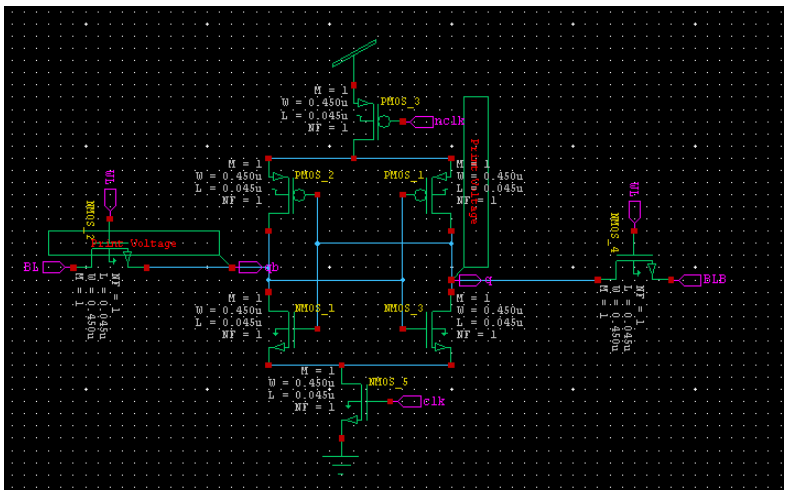

Figure 3. SRAM cell using MTCMOS technique

In Figure 3 shown below, a PMOS (High Vt) transistor is used between the pull up network and VDD while a NMOS (High Vt) transistor is used between the pull down network and ground.

The critical path transistors are required to switch fast in order to avoid incurring a penalty in delay times, all the transistors in the SRAM cell are modeled as Low Vt. Only the sleep transistors are modeled as High Vt to reduce leakage power. This configuration gives an optimized result in terms of power consumption and write/read delay.

In power gating techniques, such as Gated VDD and MTCMOS, the formation of virtual power rails (virtual VDD and ground) is very important and these are formed only when the sleep transistors are turned off. Due to the cross coupled inverters, data bits '0' (ground) and '1' (VDD) are present on either side of the SRAM cell at all times. So when the sleep transistors are turned off, VDD and ground get disconnected from the cell, and the data bits '0' and '1' on either side of the SRAM cell create the virtual power rails by charging them via the pass transistors of the inverters. These virtual power rails will always have a lower potential than VDD. To perform an operation (read/write), we switch the sleep transistors on, thereby restoring the actual VDD and ground.

In sleep mode, virtual VDD and virtual ground are responsible for data retention in the cell and as time progresses in sleep mode, the virtual VDD slowly discharges. This phenomenon thus only allows for a particular amount of time, in sleep mode, for which data in the SRAM cell can be retained after which it will be lost. To solve this problem, the sleep transistors can be turned on before this particular amount of time elapses. This then restores actual VDD and ground thereby preventing data loss in the cell. Therefore, the designer must take great care in setting the frequency of the Clock pulse that controls the sleep transistors. Alternatively, a smart power management unit can be designed which provides the Clock signal to the sleep transistors as and when required.

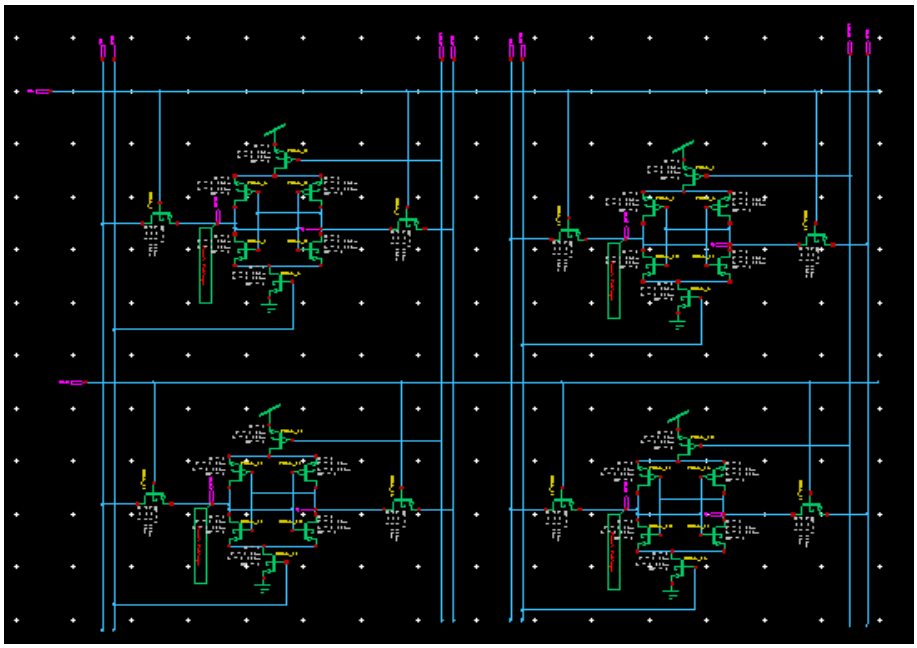

Figure 4. MTCMOS SRAM Cell array of data storage on row and column selected cell

4. Results

The average power consumption and average write power delay are calculated for various SRAM cells: Conventional 6T SRAM cell, Gated VDD SRAM cell, MTCMOS based SRAM cell and MTCMOS based SRAM array cell. Schematics of the circuits are designed and simulated in 45nm technology using tanner EDA tool. The transistors are sized in a way to obtain equal delay for the pull up and pull down networks. NMOS and PMOS transistors are sized at 45nm. The sleep transistors (High Vt PMOS and High Vt NMOS) in the MTCMOS based SRAM cells are both sized at 45nm to obtain optimum delay and power consumption.

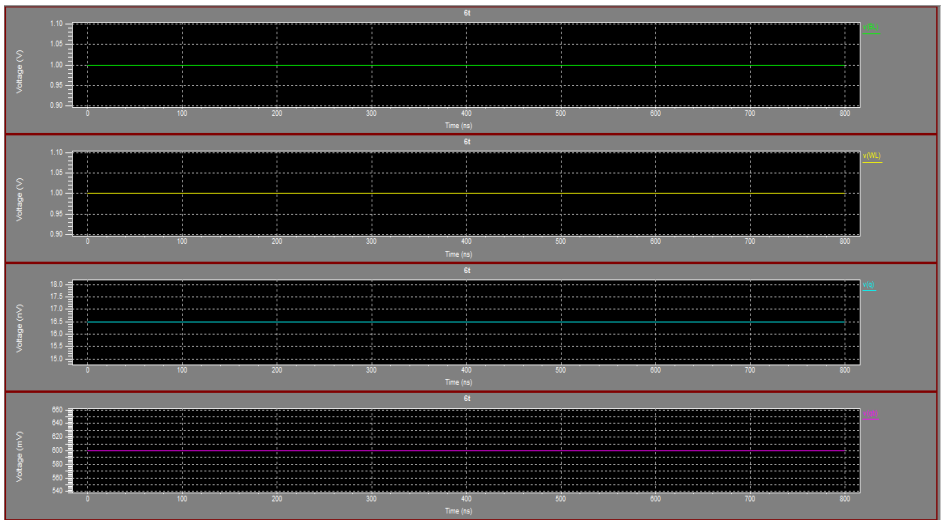

Figure 5. Conventional 6T Cell simulation

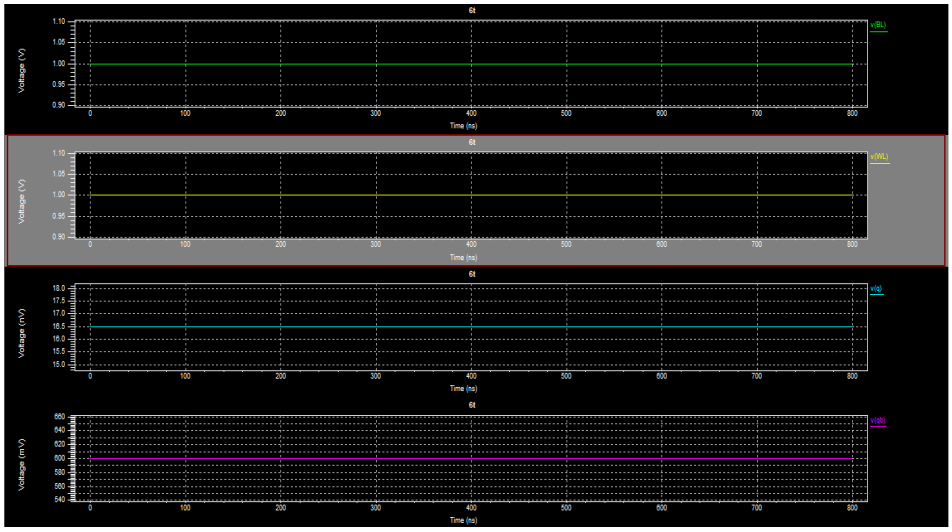

Figure 6. Gated VDD Simulation

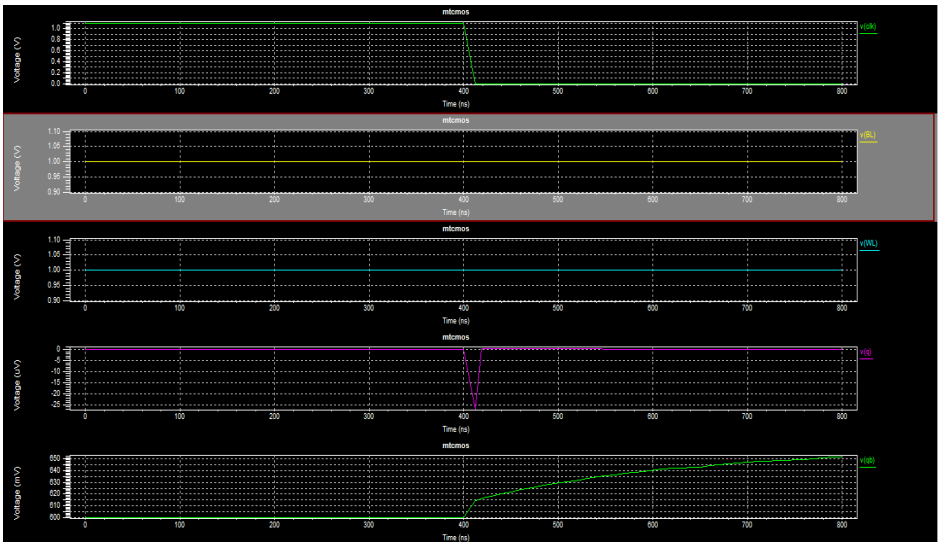

Figure 7. MTCMOS Simulation

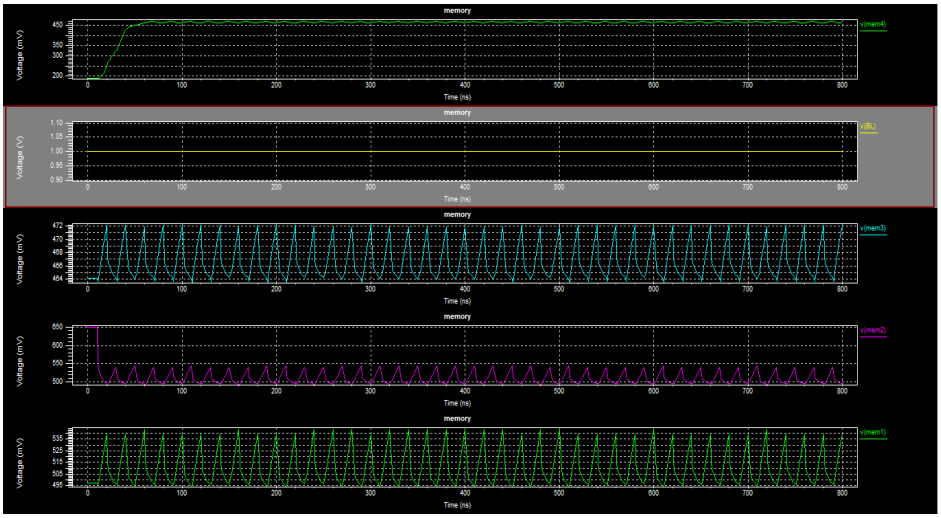

Figure 8. MTCMOS SRAM Cell array simulation

Table 1. Comparison of Various Parameters

	Conventional	Gated VDD	MTCMOS
Average Power	2.410e-009watts	1.231e-009watts	3.778e-010watts
Write power delay	2.25e-008watts	1e-008watts	4.18e-007watts

From TABLE I, the average power is computed for one clock cycle during which one write or one read operation can take place. Average power consumed by the conventional 6T SRAM cell is 2.410e-009watts, Gated VDD SRAM cell is 1.231e-009watts and MTCMOS based SRAM cell is 3.778e-010watts.

Table 2. MTCMOS based SRAM cell array parameters

	MTCMOS based SRAM Cell array
Average Power	8.251e-011watts
Write power delay	2e-008watts

The average write power delay for the conventional 6T SRAM cell is 2.25e-008watts, Gated VDD SRAM cell is 1e-008watts and MTCMOS based SRAM cell is 4.18e-007watts as shown in TABLE I.

From TABLE II, Average power consumed by total MTCMOS based SRAM Cell array (memory) is 8.251e-011watts and average write power delay is 2e-008watts as shown in TABLE II.

5. Conclusion

Two power reduction techniques for SRAM cells have been analyzed Gated VDD and MTCMOS based designs in 45nm technology. The MTCMOS based SRAM cell uses the least power and is the fastest among the three designs discussed in this paper. The MTCMOS based SRAM cell is faster than the conventional 6T SRAM cell while the Gated VDD SRAM cell is faster than the conventional 6T SRAM cell. In Gated VDD and MTCMOS designs, the transistor count increases which in turn increases the area overhead. This is the main trade off associated with these designs. With the huge reduction in power and higher speeds of operation of these SRAM cells, engineers should be motivated to use the power reduction techniques outlined in this paper for designing SRAM architectures.

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