A 102 GHz Active MMIC Tripler for sub-mm wave Receiver Development

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Abstract—

This paper presents the design and development of a 102 GHz active MMIC (Monolithic Microwave Integrated Circuit) frequency tripler using UMS 100nm pHEMT process. The multiplier is a single stage tripler followed by a BPF designed at the output frequency for high rejection of unwanted harmonics. The conversion loss achieved is 19-20 dB for an input power of 10dBm at 34 GHz of input frequency. The fundamental, second and fourth harmonic rejection is about 37dBc, 43dBc and 55dBc respectively. The tripler is simulated using 2.5D EM solver. The chip size is 2.1 mm x 2.7 mm x 0.1 mm. The efficiency of the tripler is 1.28%.

Keywords- Active, Tripler, MMIC, UMS, Conversion loss

I. INTRODUCTION

The mm and sub-mm wave region of the EM spectrum is the least explored region due to lack of sensitive receivers and technologies. Also, there are huge water absorption bands at these wavelengths making exploration difficult. The purpose of this paper is to design a frequency multiplier for sub-mm wave receiver development. The proposed design is a 102 GHz MMIC single stage tripler with an input frequency of 34 GHz. The software used for simulation is ADS (Advanced Design System).

Several MMIC based multipliers are developed from previous works as reported in the reference but most of them are mainly doublers. Comparatively less number of triplers are designed in the mm-wave band. A 47 GHz power efficient tripler is presented in [1]. In [8], a 38 GHz MMIC tripler is reported by Ali Boudiaf. Another 12GHz to 36GHz tripler has been reported in [9]. Our work describes the performance of an active MMIC tripler in the mm-wave band with high harmonic rejection.

The advantage of MMIC lies in its low cost, small size and reliability. However, at high frequencies there are certain limits encountered that needs to be addressed. Firstly, at high frequencies where the operating frequency is close to the f_{max} of the transistor, the device will show a low gain. Also, skin effect and substrate coupling degrades the performance efficiency of the device.

Secondly, the non-linearity of the device determines the harmonic power content and we need to obtain the power from the fundamental for maximum power that can be obtained at our desired harmonic. This in turn further improves the power efficiency of the device. In this paper, a single stage active tripler is designed at 102 GHz consisting of a BPF designed at the output stage at the center frequency for high harmonic rejection and passing the third harmonic content with minimum conversion loss. Active multipliers are preferred over passive multipliers because of its better gain and low noise at high frequencies. For active multipliers FETs and BJTs are mostly in use while for passive multipliers Step recovery diode, Schottky diode and varactor diode are commonly in use.

The tripler thus, designed can be used for driving the mm-wave mixer for the sub-mm receiver development in space based applications.

II. CIRCUIT DESIGN

The tripler is designed using a single-ended common source pHEMT based topology in microstrip configuration. The required MMIC foundry has been supported by *United Monolithic Semiconductor (UMS)*, France. The active device used is a non-linear hot FET model of gate length 0.1 µm and gate width 120 µm (4 x 30 µm). Nonlinearities of a FET that generate harmonic signals, when driven by a fundamental frequency of 34 GHz. The device is class A biased where the drain to source biased is kept at 3V, while the gate-to-source voltage has been carefully selected in the saturation region to efficiently produce the third order harmonic frequency, using the non-linearity of the device.

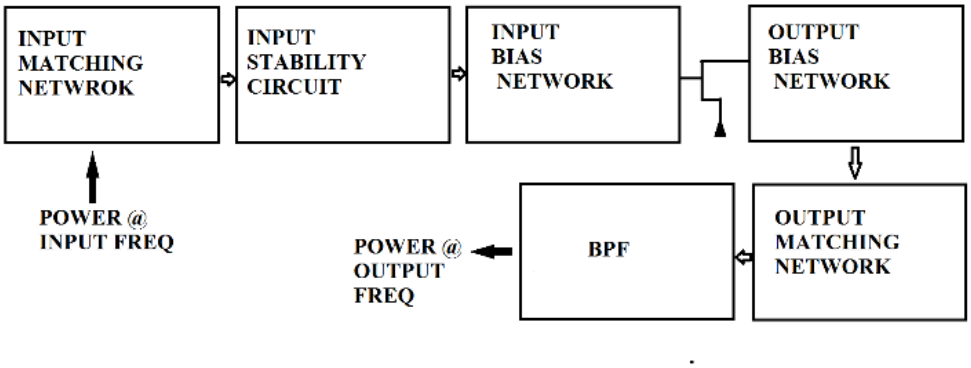


Figure.1. Block diagram of the proposed multiplier

A single stage frequency tripler scheme is shown in Fig.2. Input power at fundamental frequency is fed to the tripler circuit through the input bias network that isolates the input RF signal and gate bias voltage from each other. Similarly, the output bias network isolates the output third order harmonic and drain bias voltage from one another. The bias network is designed using λ/4 series and open circuit microstrip lines. Blocking and Bypass capacitors are chosen according to the foundry specifications. Stability of the overall circuit has been analysed for the entire frequency range from DC to f_{max} to ensure unconditional stability.

An additional stability network is added at the gate side in order to stabilise the transistor, which consists of a shunt arrangement of a RC network. The circuit consists of distributed elements realized using microstrip network and capacitors along with the device compatible with the UMS foundry specifications.

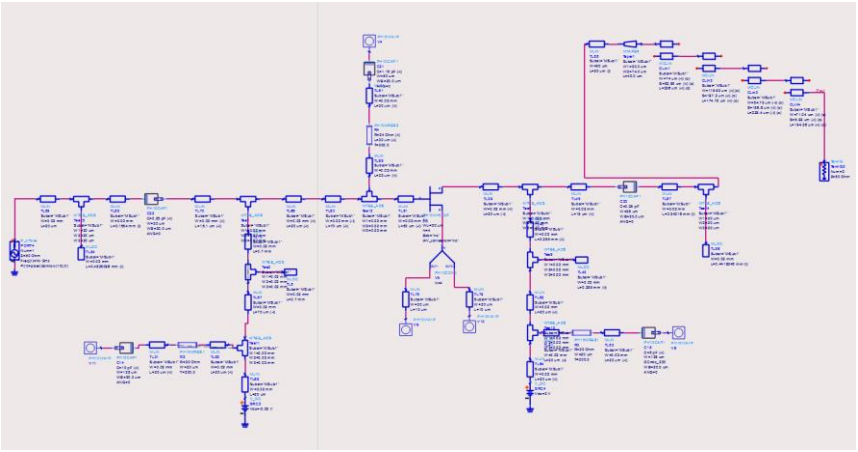


Figure.2. Schematic of the tripler

The bias network is designed following fixed bias configuration. Next, the device is made stable for the optimum operating bias condition and the input and output matching network is designed using single stub matching at 50 Ohm. The length of the stubs is adjusted to optimize the tripler performance. A BPF at 102 GHz with impedance of 50 Ohm is designed to reject the unwanted harmonics. The rejection with a BPF is much high as compared to λ/4 idlers at the unwanted harmonics. This is because when we use a λ/4 idler to reject the fundamental, it becomes 3λ/4 at the third harmonic thereby reducing the power content which is our requirement.

In the proposed design for biasing and matching, the design since distributed is done by using only two microstrip lines. One parallel and one series inductive stubs are used at the input and output, respectively to provide required inductive impedances to the pHEMT device. Length of the inductive stubs are adjusted for optimum multiplier performance.

III. TRIPLER SIMULATION

The tripler designed at 102 GHz is designed obtaining maximum power output for the third harmonic content. The EM simulation is carried out in ADS for the entire cascaded design part by part and then integrated altogether. The manufacturing needs to be performed in a 70µm thick GaAs substrate.

The bias network, stability circuit and the matching networks are EM simulated and their results are matched with the original schematic result by adjusting the length of the stubs and bringing them at the center frequency.

The tripler circuit has been modeled in schematic design of ADS for circuit level simulation and its performance has been evaluated through Harmonic Balance (HB) analysis. Stability analysis of the tripler has also been performed with S-parameter simulation. After the schematic design, total circuit except the pHEMT, has also been modeled in 2.5D planar electromagnetic simulator *Momentum* available in ADS. A co-simulation has been performed using the EM model of the circuit and the non-linear hot-FET model of the pHEMT. The integrated co-simulated circuit of the multiplier is shown in Figure 4. The best output was obtained when the input frequency is 34 GHz with 10dBm of input power. The BPF designed at 102 GHz is individually simulated for S11 and S21 to be minimum and maximum respectively. However, it introduces an additional loss of 4dB to the design that has to be taken into account. The layout of the tripler is shown in the figure below.

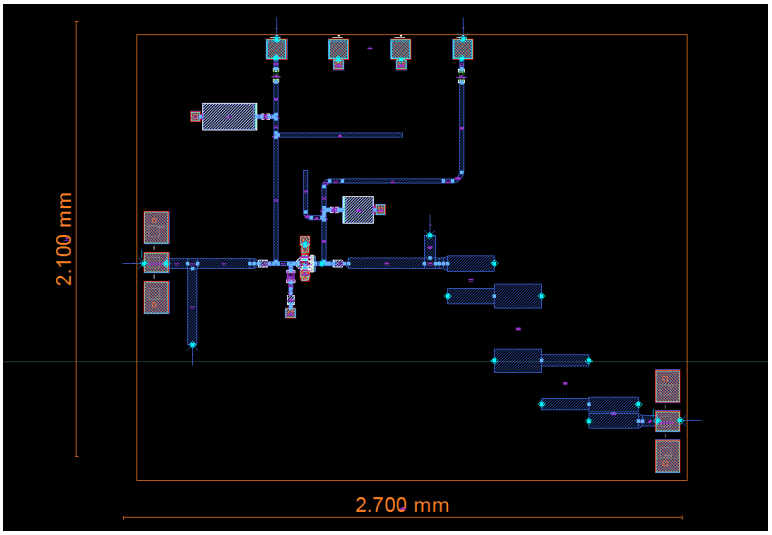


Figure.3. Layout of the tripler

IV. SIMULATION RESULTS

The chip dimension is of 2.1 mm x 2.7 mm x 0.1 mm. The tripler is biased using an external power source. The Vgs and Vds for the tripler are set as -0.05V and 3V respectively. Power efficiency for the designed tripler is 12.8%. The input power is fixed at 10dBm while the input frequency is swept from 25GHz to 35GHz corresponding to a third harmonic output frequency around 75-105 GHz. Hence the dc power consumption is 52.8 mW for an output drain current of 17.6 mA. The bandwidth of the designed multiplier is 140-180 MHz.

The layout for the tripler is shown. For an input frequency of 34 GHz and 10 dBm input power the output power for the third harmonic content is -9.3 dBm exhibiting a conversion loss of 19.3dB. The rejection of the fundamental, second and fourth harmonics are shown by the HB analysis which indicates a rejection of 37dB, 43dB and 55dB respectively. The BPF simulated at 102 GHz when cascaded with the tripler introduces an additional loss of 3-4 dB thereby degrading the conversion loss to about 19 dB which was otherwise 15 dB without the incorporation of the filter. The design is developed to bear the mechanical/electrical stress during fabrication and is tolerant to the coupling due to substrate and nearby microstrip components. It is to be ensured that there should be a high series impedance, like a spiral inductor or a large resistor between the RF signals and the dc bias pads or there is a low impedance path near the pads, like a large capacitor that is well grounded. The components must be kept at a minimum distance of 50µm from each other in order to prevent undesired parasitic coupling between them. The RF and the dc probes connected with the pads are shown in the layout above. A performance comparison of the tripler is shown in Table. I which compares the multiplier with previously reportedly works.

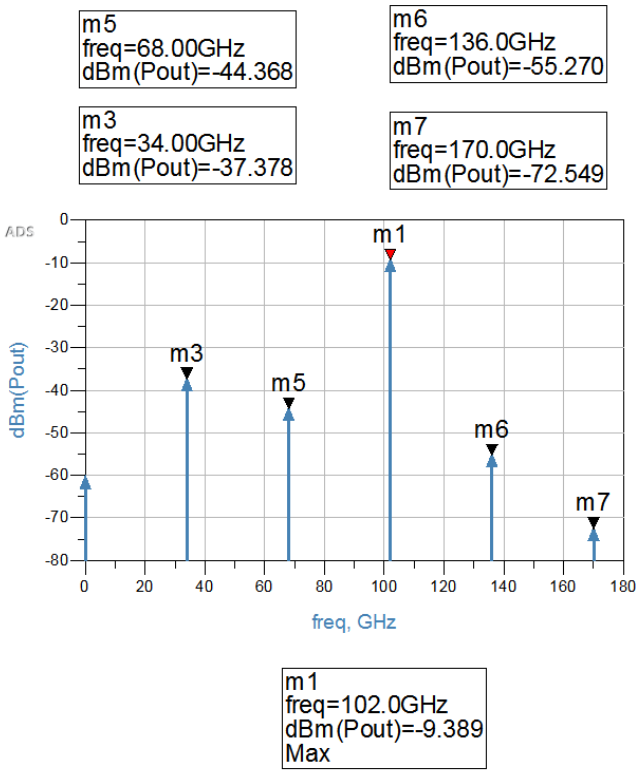
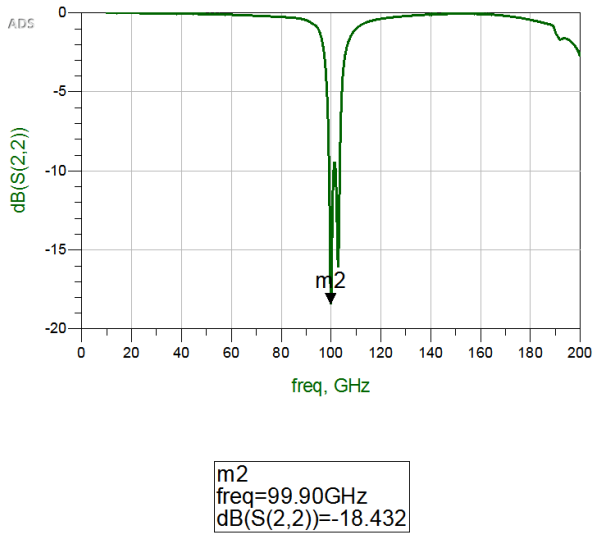


Figure.4. Output power of all harmonics vs frequency



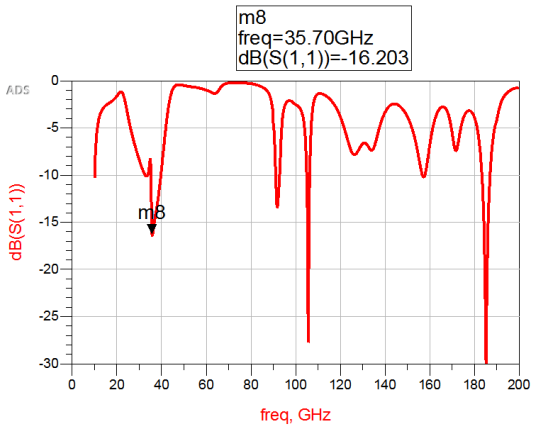


Figure.5. Return loss vs frequency

TABLE I. PERFORMANCE COMPARISON OF MMIC TRIPLERS

References	**[7]**	**[8]**	**[9]**	**[1]**	**This work**
Configuration	**Single pHEMT**	**Single pHEMT**	**Balanced pHEMT**	**Single pHEMT**	**Single pHEMT**
F_{out} (GHz)	76.5	38.64	36	47	102
P_{out}(dBm)	4.2	3.1	-0.4	1.5	-9.3
Conversion Loss	4.3	3.4	9.4	3.5	19.3
Rejection @f_0 (dBc)	16	41	21	31	37.3
Rejection @$2f_0$ (dBc)	32	26	22	27	44.3
Rejection @$4f_0$ (dBc)	13	-	-	28	55.2

V. CONCLUSION

Design techniques and implementation steps for a 102 GHz MMIC single stage tripler has been described in MMIC configuration. The rejection for the unwanted harmonics are all below 30dB which exhibits a high suppression due to the incorporation of the BPF. The design is DRC verified. The measured conversion loss ranges between 18-20 dB for a frequency range 100-107 GHz with a power efficiency of 12.8%. The tripler can be used for driving a mm-wave mixer for a sub-mm receiver development.

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