A SINGLE SWITCH NONISOLATED BUCK BOOST DC- DC CONVERTER

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ABSTRACT-In this paper a single switch nonisolated Buck-Boost DC-DC converter . The proposed converter voltage gain is higher than that of the conventional boost, buck, CUK, SEPIC, and ZETA converters, and high voltage can be obtained with a suitable duty cycle. This paper shows the comparison between boost converter, buck converter and the proposed buck-boost converter. In this converter, only one power switch is utilized. The volt age stress across the power switch is low. Hence, the low on-state resistance of the power switch can be selected o decrease conduction loss of the switch and improve efficiency. The presented converter has simple structure, therefore, the control of the proposed converter will be easy. The principle of operation and the mathematical analyses of the proposed converter are explained. results. The proposed converter validation is done by using MATLAB software.

Keywords: **Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Equivalent Series Resistance (ESR)**

INTRODUCTION

IN recent years, environmental troubles, such as climate change and global warming by increased emissions of carbon dioxide, are very important. With increasing attention to environmental problems, energy achieved from the fuel cell systems is focused on the low environmental effects and clean energy. Fuel cells are an effective alternative to replace fuels in emergency power systems and vehicles. User can use fuel cells as clean energy with low emissions of carbon dioxide. Due to steady operation with renewable fuel supply and high effectiveness and efficiency, the fuel cell has been recognized increasingly as a suitable alternative source. There are some problems of this fuel, such as high costs, but they have brilliant features, such as high efficiency and small size. Due to this explanation, the fuel cell is appropriate as power supplies for telecom back-up facilities and hybrid electric vehicles. The output voltage of the fuel cell unit cell is low and is not steady and it cannot be directly connected to the load. For applications that need a steady dc voltage, buck–boost dc–dc converter is required [1]–[5].

However, the traditional buck–boost converter is not suitable for fuel cells sources. The traditional buck–boost converter efficiency is expected to be high, however, it is low and is limited by the effects of diodes, switches, and equivalent series resistance (ESR) of capacitors and inductors [6]. In order to obtain the high efficiency and high voltage gain, many high step-up dc–dc converters have been proposed and in order to use the low duty cycle, adding a new control method is a good choice [7], [8]. For example, the high step-up voltage gain can be achieved by using a flyback converter with low duty cycle. The voltage gain of the flyback converter can be increased by raising the turns ratio of the transformer. Although the flyback converter can obtain the high step-up voltage gain, the power switches suffer a voltage spike across the switches and the converter efficiency is not high because of the reverse-recovery problems and leakage inductor [9]–[11]. In [12] and [13], high voltage gain dc–dc converters with a coupled inductor are proposed. The leakage inductance of the coupled inductor is so important that it causes high voltage spikes and adds the voltage stress.

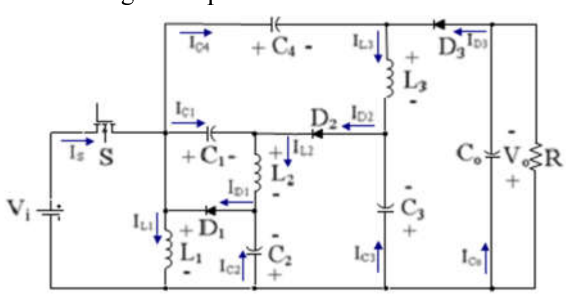
In [14], the switched capacitor method is used to obtain high step-up voltage gain. In [15], a high step-up bidirectional dc–dc converter with low voltage stress on the switch is proposed. In [16], a high conversion ratio bidirectional dc–dc converter is proposed. However, this converter has five power switches that increase the conduction losses and the cost of the circuit and decrease the efficiency. In [17], a transformerless interleaved high step-down converter is proposed, but, in the presented converter, two power switches have been utilized and the capacitors of the converter are suddenly charged. In [18], transformerless high step-up dc–dc converters are proposed. In [19], a transformerless buck–boost dc–dc converter is proposed. The voltage gain for this converter is twice as large as that of the conventional buck–boost converter. In [20], a buck–boost converter based on KY converter is proposed. In this converter, two main switches are used and the voltage gain of the presented converter is 2D. In [21], a transformerless buck–boost dc–dc converter based on CUK converter is proposed. The voltage transfer gain for the presented converter is twice as large as that of the conventional buck–boost converter. In [22], a multi-output buck–boost dc–dc converter is proposed. This converter has several output voltages, but, in the presented converter, many power switches have been used. In [23], a two-stage inverting buck–boost converter is proposed.

The presented converter is constructed of two parallel conventional buck–boost converters. In [24], a two-stage buck–boost converter for power factor correction is presented and this converter does not require additional power switch. In this paper, a single-switch buck–boost dc–dc converter with high step-up voltage gain and low voltage stress on the power switch is proposed. The voltage transfer gain of the proposed converter is higher than that of the classic buck–boost converter, SEPIC, CUK, and ZETA converters. The structure of the proposed converter is simple, hence the control of the converter will be easy. In this converter, only one main switch is used.

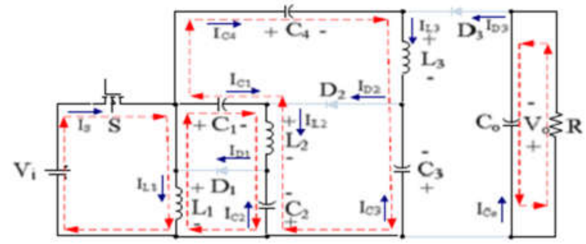
The voltage stress across the power switch and diodes is less than the output voltage, hence the conduction loss of the power switch is low and the efficiency of the presented converter can be improved. The presented converter operates as a universal power supply and it is appropriate for low-voltage and low-power applications and the proposed converter input current is discontinues. The proposed buck–boost converter is utilized in many applications, like fuel-cell systems, car elec tronic devices, LED drivers, and gadgets, such as mobile phones and notebooks. In this paper, the mathematical analyses of the proposed converter are explained. Besides, to verify the feasibility of the converter, experimental results are provided.

OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

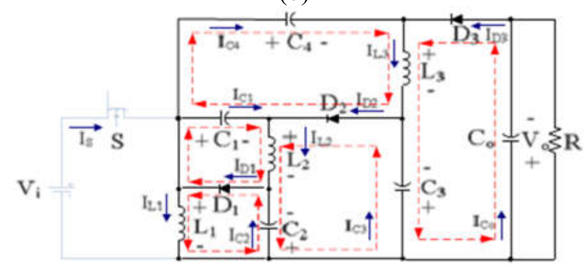
The proposed converter is shown in Fig. 1(a). This converter consists one power switch S, three diodes D1, D2, and D3, three inductors L1, L2, and L3, five capacitors C1, C2, C3, C4, and Co and load R. For simplicity of the analysis of the operating principles, the following assumptions are considered.



(a)



(b)



(c)

Fig.1. (a) Equivalent circuit of the proposed converter. (b) Mode 1. (c) Mode 2

1) The capacitors of the presented converter are large enough, hence the voltage across capacitors are assumed to be constant.

2) The main switch of the proposed converter is treated as ideal and the parasitic capacitor of the main switch is neglected.

The presented converter can be operated in both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The CCM can be divided into two operation modes. The analysis of the presented converter in one switching period under CCM is explained in detail as follows:

1**) First mode [0 ≤ t ≤ DTs]:** During this time interval as shown in Fig. 1(b), the switch S is turned ON and the diodes D1, D2, and D3 are turned OFF. The inductors L1, L2, and L3 are magnetized linearly. The capacitors C1 and C4 are charged by the capacitors C2 and C3. Thus, the relevant equations can be expressed as follows:

$$V_{L1} = V_i \qquad (1)$$

$$V_{L2} = V_{C2} - V_{C1} + V_i \qquad (2)$$

$$V_{L3} = V_{C3} - V_{C4} + V_i \qquad (3)$$

2**) Second mode [DTs ≤ t ≤ Ts]:** The equivalent circuit is shown in Fig. 1(c). During this time interval, the switch S is turned off and the diodes D1, D2, and D3 are turned on. The inductors L1, L2, and L3 are demagnetized l_{in} early. The capacitor C2 is charged by the inductor L1 and the capacitor C3 is charged by the inductors L1 and L2 and the capacitors C1 and C4 are discharged. The corresponding equations can be written as follows:

$$V_{L1} = -V_{C2} \qquad (4)$$

$$V_{L2} = -V_{C1} = V_{C2} - V_{C3} \qquad (5)$$

$$V_{L3} = V_{C1} - V_{C4} = V_{C3} - V_o \qquad (6)$$

STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

A. Voltage Gain

By applying volt-sec balance principle on the inductors L1, L2, and L3 and using (1)–(6), we have

$$\frac{1}{T_S}\left(\int_0^{DT_S} V_i dt \int_{DT_S}^{T_S}(-V_{C2})dt\right) = 0 \quad (7)$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} (V_{C2} - V_{C1} + V_i)dt \int_{DT_S}^{T_S}(-V_{C1})dt\right) = 0 \quad (8)$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} (V_{C3} - V_{C4} + V_i)dt \int_{DT_S}^{T_S}(V_{C1} - V_{C4})dt\right) = 0 \quad (9)$$

By using (5) and (7)–(9), the voltage across capacitors C1, C2, C3, and C4 (VC 1, VC 2, VC 3, and VC 4) can be achieved as follows:

$$V_{C1} = V_{C4} = \frac{2DV_i}{1-D} \quad (10)$$

$$V_{C2} = V_{C3} = \frac{DV_i}{1-D} \quad (11)$$

Using (10) and (11), the voltage transfer gain (MCCM) can be found as follows:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{V_{C3} + V_{C4}}{V_i} = \frac{3D}{1-D} \quad (12)$$

According to (12), the voltage gain of the proposed converter is higher than that of the conventional boost, buck–boost, CUK, SEPIC, and ZETA converters and is thrice as large as the voltage gain of the conventional buck–boost converter. Fig. 2 shows some typical key waveforms of the proposed converter in CCM.

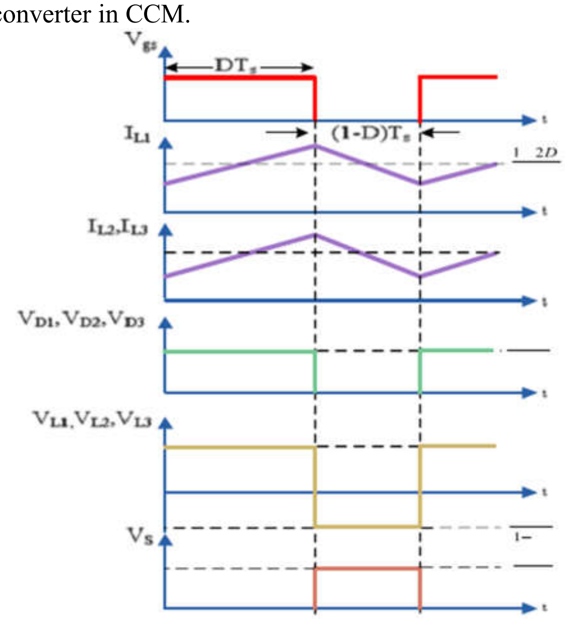


Fig.2 Some typical waveforms of the proposed converter.

The voltage gain curves for the proposed converter, conventional boost, buck—boost, and CUK converters, proposed converter III in [18] and proposed converter in [19] are shown in Fig. 3. It is seen that the proposed converter is buck–boost and the voltage transfer gain of the converter is higher than that of the other converters.

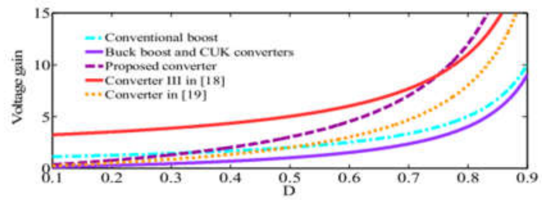


Fig.3 Curves of voltage gain comparison of proposed converter and other converters at CCM operation.

B. Calculation of the Currents

The average current that flows through the capacitor Co during switch ON period ($I_{Co,on}$) can be achieved as follows:

$$I_{Co,on} = -I_o \quad (13)$$

The average current that flows through the capacitors C1 and C2 and the inductor L2 ($I_{C1,on}$, $I_{C,on}$, and I_{L2}) during switch ON period can be obtained as follows:

$$I_{C1,on} = -I_{C2,on} = I_{L2} \quad (14)$$

The average current that flows through the capacitors C3 and C4 and the inductor L3 during switch ON period ($I_{C3,on}$, $I_{C4,on}$, and I_{L3}) can be earned as follows:

$$-I_{c3,on} = I_{C4,on} = I_{L3} \quad (15)$$

The average current that flows through the capacitor C1 during switch off period (IC 1,off) can be earned as follows:

$$I_{C1,off} = I_{L2} - I_{C3,off} - I_{L3} \quad (16)$$

Where, IC 3,off is the average current that flows through the capacitor C3 during switch OFF period. The average current that flows through the capacitors C4 ($I_{C4,off}$) during switch OFF period can be achieved as follows:

$$I_{C4,off} = I_{L3} - I_{Co,off} - I_o \quad (17)$$

Where, $I_{Co,off}$ is the average current that flows through the capacitor Co during switch OFF period. By applying current-sec balance principle on capacitors C1, C2, C3, C4, and Co, the following equation is derived as follows:

$$\frac{1}{T_S}\left(\int_0^{DT_S} I_{C1,2,3,4,o,on} dt \int_{DT_S}^{T_S}(I_{C1,2,3,4,o,off})dt\right) \; 0 \quad (18)$$

Where $I_{C2,off}$ is the average current that flows through the capacitor C2 during switch OFF period.

By substituting (13)–(17) into (18), the average current that flows through the inductors L2 and L3 (IL2 and IL3) and the capacitors C1, C2, C3, C4, and Co (IC 1,on, IC 2,on, IC 3,on, IC 4,on, and IC o,on) can be obtained as follows:

$$I_{L2} = I_{L3} = I_{C1,on} = -I_{C2,on} = -I_{C3,on} = I_{C4,on} = -I_{Co,on} = I_o \quad (19)$$

According to Fig. 1(c), the average current that flows through the inductor L1 (IL1) can be earned as follows:

$$I_{L1} = (I_{L2} + I_{C2} - I_{C1} - I_{C4})_{off} = \frac{1+2D}{1-D} I_o \quad (20)$$

According to Fig. 1(b), the average current that flows through the switch S (IS) can be obtained as follows:

$$I_S = I_{L1} + I_{C1,on} + I_{C4,on} = \frac{3}{1-D} I_o \quad (21)$$

The average of input current (Ii) can be achieved as follows:

$$I_i = \frac{1}{T_S}\left(\int_0^{DT_S} (I_{L1} + I_{C1,on} + I_{C4})_{on} dt\right) = \frac{3D}{1-D} I_o \quad (22)$$

The currents that flows through the diodes D1, D2, and D3 (ID1, ID2, and ID3) can be achieved as follows:

$$I_{D1} = (I_{L1} - I_{C1,off} - I_{C4,off}) = \frac{I_o}{1-D} \quad (23)$$

$$I_{D2} = I_{L2} + I_{C1,off} = \frac{I_o}{1-D} \quad (24)$$

$$I_{D3} = I_{L3} + I_{C4,off} = \frac{I_o}{1-D} \quad (25)$$

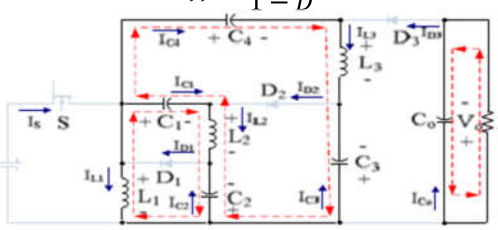


Fig. 4 Equivalent circuits of the presented converter in third mode at DCM operation.

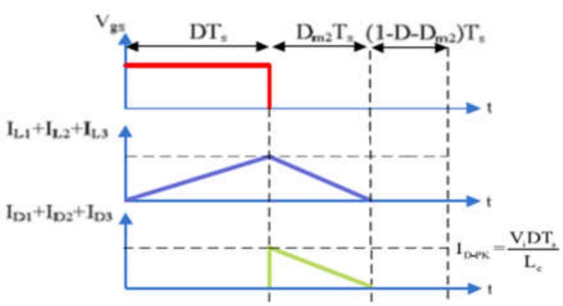


Fig.5 Some illustrated waveforms of the proposed converter at DCM operation.

The currents ripple of inductors L1, L2, and L3 ($\Delta I_{L1,2,3}$) can be calculated as follows:

$$\Delta I_{L1,2,3} = \frac{DV_i}{L_{1,2,3} fs} = \frac{(1-D)}{3L_{1,2,3} fs} = \frac{V_o V_i}{(V_o + 3V_i) L_{1,2,3} fs} \quad (26)$$

C. Discontinuous Conduction Mode

The operation modes in DCM can be divided into three modes. The first mode in DCM is the same as the first mode in CCM. In the second mode, the diodes currents are decreasing and in the third mode the diodes D1, D2, and D3 currents will be zero and the diodes and switch will turn OFF. The equivalent circuit and the typical waveform in third mode are shown in Figs. 4 and 5. In this mode, the inductors L1, L2, and L3 currents will be constant; therefore, the voltage of the inductors L1, L2, and L3 will be zero.

According to (23)–(25), the sum of the diodes D1, D2, and D3 currents can be obtained as follows:

$$I_{D1} + I_{D2} + I_{D3} = I_{L1} + I_{L2} + I_{L3} \quad (27)$$

By using (23)–(25), the average currents of diodes D1, D2, and D3 ($I_{D1,av}$, $I_{D2,av}$, and $I_{D3,av}$) can be achieved as follows:

$$I_{D1,av} = I_{D2,av} = I_{D3,av} = \frac{V_o}{R}$$

According to Fig. 4, the sum of the diodes D1, D2, and D3 average currents during one switching period can be obtained as follows:

$$I_{D1,av} + I_{D2,av} + I_{D3,av} = \frac{1}{2} \times D_{m2} \times I_{D-PK} \quad (29)$$

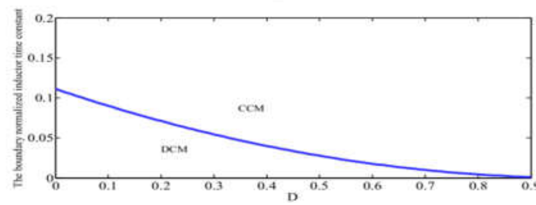


Fig. 6 Boundary normalized inductor time constant versus duty cycle.

Where D_{m2} is duty cycle in second mode at DCM and ID−PK is sum of the peak currents of inductors L1, L2, and L3

$$I_{D-pk} = I_{L1-pk} + I_{L2-PK} + I_{L3-PK} = \frac{V_i D T_S}{L_{eq}} \quad (30)$$

Where

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \quad (31)$$

By applying volt-sec balance principle on inductors L1, L2, and L3, duty cycle in second mode at DCM (D_{m2}) can be achieved as follows:

$$D_{m2} = \frac{3V_i D}{V_o} \quad (32)$$

By using (27)–(32), the voltage transfer gain in DCM (MDCM) can be earned as follows:

$$M_{DCM} = \frac{D}{\sqrt{\tau_L}} \quad (33)$$

where the parameter τ_L is expressed as follows:

$$\tau_L = \frac{2L_{eq}}{RT_S} \quad (34)$$

D. Boundary Condition Mode

In this mode, the voltage transfer gain of the CCM is equal to the voltage transfer gain of the DCM. According to (12) and (33), the boundary normalized inductor time constant (τ_b) can be earned as follows:

$$\tau_b = \frac{(1-D)^2}{9} \quad (35)$$

The curve of the boundary normalized inductor time constant (τ_b) is shown in Fig. 6. If τL is larger than τ_b, the proposed buck–boost converter operates in CCM.

The boundary normalized inductor time constant curves for the proposed converter, proposed converter III in [18] and proposed converter in [19] are shown in Fig. 7.

E. Efficiency Analysis

For efficiency analysis of the proposed converter, parasitic resistances are defined as follows: rDS is switch ON-state resistances, RF 1, RF 2, and RF 3 are the diodes D1, D2, and

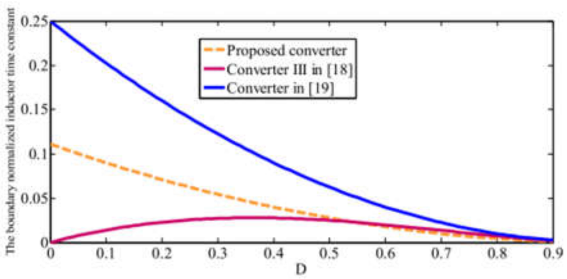


Fig.7 Curves of boundary inductor time constant comparison of proposed converter and other converters.

D3 forward resistances, respectively, VF 1, VF 2, and VF 3 are the diodes D1, D2, and D3 threshold voltages, respectively, RL1, RL2, and RL3 are the ESR of inductors L1, L2, and L3, respectively. rC1, rC2, rC3, rC4, and r_{Co} are the ESR of capacitors C1, C2, C3, C4, and Co, respectively, and the voltage ripple across the capacitors and the inductors is ignored.

The power loss of the switch S (PrDS) can be earned as follows:

$$P_{rDS} = r_{DS} I_{S,rms}^2 = r_{DS} \frac{9D}{(1-D)^2} I_O^2 \qquad (36)$$

The switching loss of the proposed converter (P_{Sw}) can be obtained as follows:

$$P_{Sw} = f_s C_S V_S^2 = f_s C_S \left(\frac{V_i}{1-D}\right)^2 \qquad (37)$$

The total losses of the switch S (P_{Switch}) can be expressed as follows:

$$P_{Switch} = P_{rDS} + \frac{P_{Sw}}{2} \qquad (38)$$

The diodes D1, D2, and D3 forward resistance losses ((PRF)D1,2,3) can be achieved as follows:

$$(P_{RF})_{D1,2,3} = R_{F1,2,3} I_{D1,2,3,rms}^2 = R_{F1,2,3} \frac{1}{1-D} I_O^2 \qquad (39)$$

The diodes D1, D2, and D3 forward voltage losses ((PVF)D1, 2, 3) can be obtained as follows:

$$(P_{VF})_{D1,2,3} = V_{F1,2,3} I_{D1,2,3,av} = V_{F1,2,3} I_o \qquad (40)$$

The power losses of capacitors C1, C2, C3, C4, and Co (PRC1,2,3,4,o) due to them ESR, can be earned as follows:

$$P_{RC1,2,3,4,o} = r_{C1,2,3,4,o} I_{C1,2,3,4,o,rms2} = \frac{D}{1-D} I_O^2 \qquad (41)$$

The conduction losses of inductors L1, L2, and L3 (PrL1 and PrL2,3) can be earned as follows:

$$P_{rL1} = R_{L1} I_{L1,rms}^2 = R_{L1} \left(\frac{1+2D}{1-D}\right)^2 I_O^2 \qquad (42)$$

$$P_{rL2,3} = R_{L2,3} I_{L2,3,rms}^2 = R_{L2,3} I_O^2 \qquad (43)$$

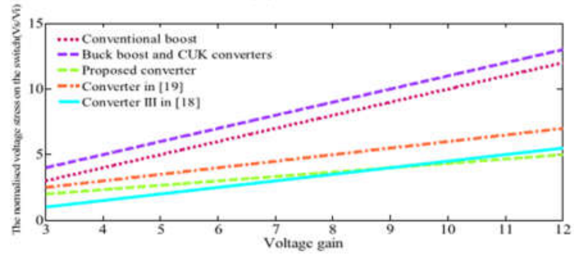


Fig.8 Normalized switch voltage stress of the proposed converter versus voltage gain.

TABLE I
COMPARISON BETWEEN PROPOSED CONVERTER AND OTHER STRUCTURES

Converter in	Proposed converter	Converter in ref.	Conventional buck–boost converter
Quantities of switches	1	1	1
Quantities of diodes	3	2	1
Quantities of capacitors	5	4	1
Quantities of inductors	3	3	1
Total device count	12	10	4
Voltage stress of the switch	$\frac{V_o+3}{3}$	$\frac{V_o+2}{2}$	V_o+1
Voltage gain	$\frac{3D}{1-D}$	$\frac{2D}{1-D}$	$\frac{D}{1-D}$

The total power loss of the proposed converter (P_{Loss}) can be obtained as follows:

$$P_{Loss} = P_{Switch} + \sum_{u=1}^{3} (P_{RF})_{Du} + \sum_{u=1}^{3} (P_{VF})_{Du} + \sum_{u=1}^{4} P_{RCu} + P_{RCo} + P_{rL!} + P_{rL2} + P_{rL3} \qquad (44)$$

The efficiency of the proposed converter (η) can be defined as follows:

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1 + \frac{P_{Loss}}{P_O}} \qquad (45)$$

According to above equations, the efficiency of the proposed converter can be rewritten as follows:

$$\eta = \frac{1}{1 + \frac{\pi}{R(1-D)^2} + \frac{f_s C_S V_i^2}{2(1-D)^2 R I_O^2}} \qquad (46)$$

Where

$$\pi = 9P_{rDS} + (1-D)(R_{F1} + R_{F2} + R_{F3}) + \frac{(1-D)^2}{I_o}(V_{F1} + V_{F2} + V_{F3}) + D(1-D)(r_{C1} + r_{C2} + r_{C3} + r_{C4} + r_{Co}) + (1+2D)^2 R_{L1} + (1-D)^2 (R_{L2} + R_{L3}) \qquad (47)$$

F. Voltage Stress of the Switch

In this converter, the voltage stress across the active components, such as switch and diodes, is lesser than output voltage. The voltage stress on power switch (VS) can be achieved as follows:

$$V_S = \frac{V_i}{1-D} \quad (48)$$

The relationship between the normalized voltage stress across power switch of the proposed converter and other converters is depicted in Fig. 8. According to Fig. 8, the normalized voltage stress of the switch in the proposed converter is lesser than that in other converters.

In order to show the total device number and voltage gain of the proposed converter, conventional buck–boost, and converter in [18], a comparison is made between the proposed topology and other converters.

The device number and voltage gain of the structures are given in Table I. As shown in Table I, the proposed structure uses higher number of elements. But, the total device of the other converters is higher comparing to their gains and voltage stresses. Based on the low voltage stress of the proposed converter, the efficiency of the proposed converter is higher comparing to its gain.

G. Calculation of the Voltage Ripple of the Capacitors

From Fig. 9, the voltage ripple of the capacitor C1 is rep resented by ΔVC 1. The voltage ripple on capacitor C1 created from the current that flows through the ESR is signified by ΔVC 1,ESR and the voltage ripple of capacitor C1 created from the charging and discharging is indicated by ΔVC 1,cap.

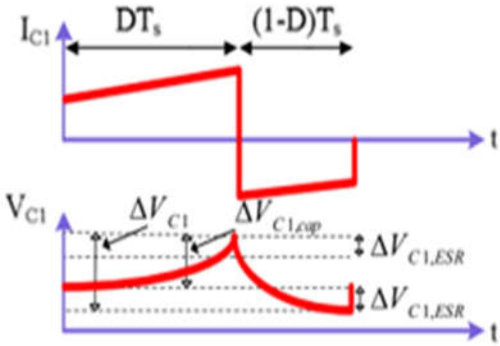


Fig. 9 Current and voltage of the capacitor C1

ΔVC 1,ESR can be calculated as follows:

$$\Delta V_{C1,ESR} = ESR_{C1}\Delta I_{C1} \approx ESR_{C1}\left(I_{C1,on} - I_{C1,off}\right) = \frac{ESR_{C1}I_o}{(1-D)} \quad (49)$$

Where

$$ESR_{C1} = \frac{\tan\delta_{C1}}{2\pi f_S} \quad (50)$$

where, tan δC 1 is the dissipation factor of capacitor C1 ΔVC 1,cap can be achieved as follows:

$$\Delta V_{C1,cap} = \frac{I_{C1,on}DT_S}{C1} = \frac{DT_S V_o}{RC1} \quad (51)$$

Hence, ΔVC 1 can be achieved as follows:

$$\Delta V_{C1} = \Delta V_{C1,ESR} + \Delta V_{C1,cap} = \frac{ESR_{C1}I_o}{1-D} + \frac{DT_S V_o}{R_{C1}} \quad (52)$$

Similarly, the voltage ripple of the capacitors C2, C3, C4 and Co (ΔVC 2,3,4,o) can be achieved as follows:

$$\Delta V_{C2,3,4,o} = \Delta V_{C2,3,4,o,ESR} += \Delta V_{C2,3,4,o,cap} = \frac{ESR_{C2,3,4,o}I_o}{1-D} + \frac{DT_S V_o}{R_{C2,3,4,o}} \quad (53)$$

The current and voltage of the capacitors C2, C3, C4, and Co are shown in Figs. 10—13.

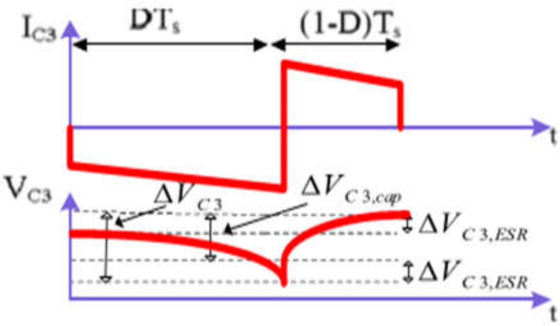


Fig. 10 Current and voltage of the capacitor C2 .

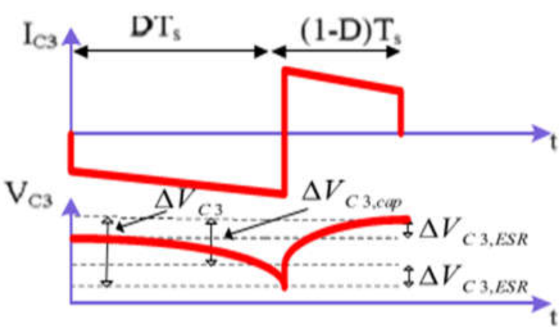


Fig.11 Current and voltage of the capacitor C3

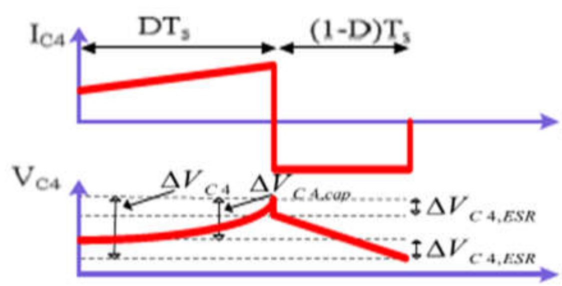


Fig. 12 Current and voltage of the capacitor C4

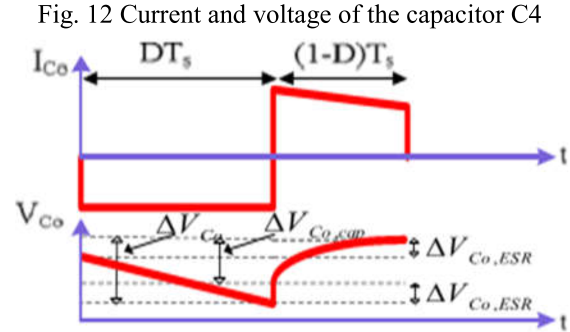
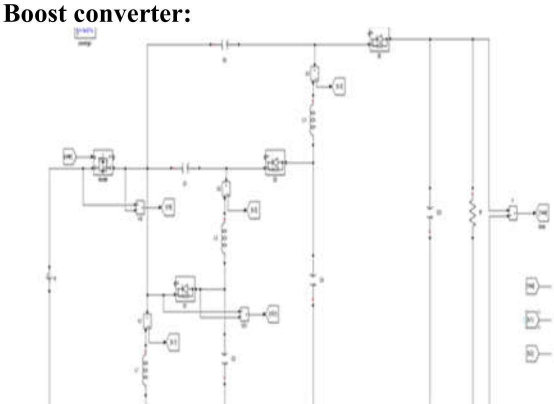


Fig.13 Current and voltage of the capacitor Co.

The proposed converter is tested in the buck and boost states operation. The proposed converter is operated in CCM operation mode. In the buck state operation, the output voltage waveform is shown in Fig.15(a). The output voltage is equal to 10 V. The inductors L1, L2, and L3 currents waveforms are shown in Fig.15(b), (c), and (d), respectively. According to (19) and (20), the average values of inductors L1, L2, and L3 currents are equal to 0.45, 0.24, and 0.24 A, respectively, which closely agree with the experimental results. The voltages of diodes D2 and D3 waveforms are not shown since the diodes waveforms are similar to diode D1 voltage waveform. The voltage of diodeD1 waveform is shown in Fig.15(e).The voltage of the switch S is shown in Fig.15(f).

SIMULATION RESULTS

Boost converter:



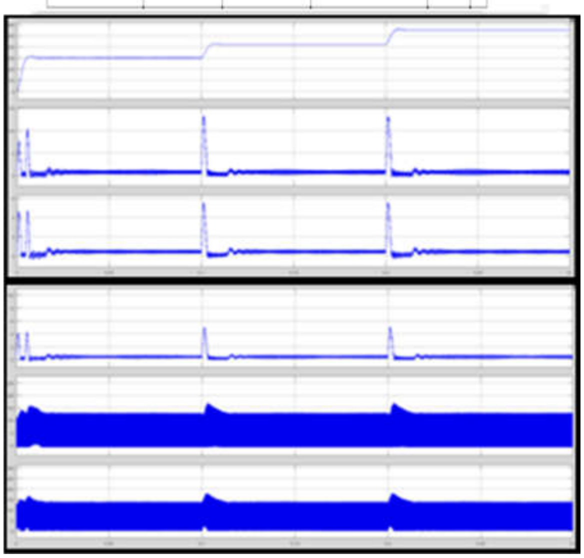
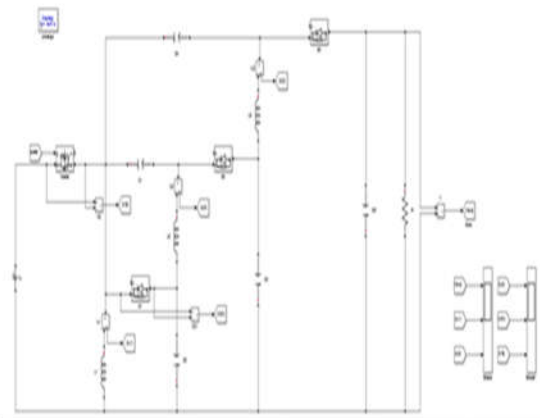


Fig.15 Waveforms of (a) output voltage, (b) inductor L1 current, (c) inductor L2 current, (d) inductor L3 current, (e) diode D1 voltage, (f) switch S voltage.

Buck converter:



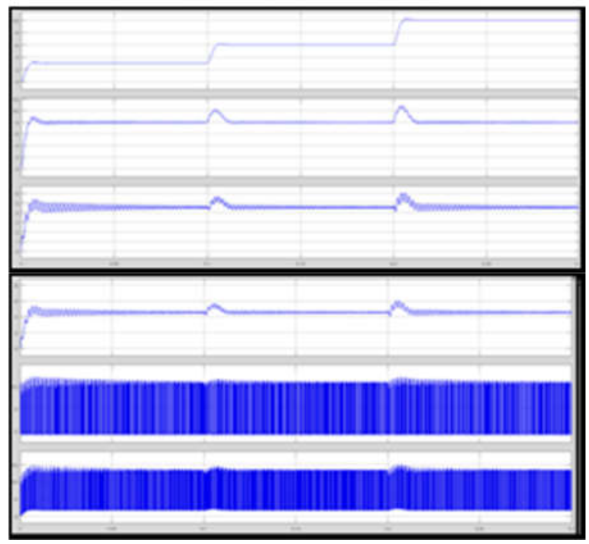
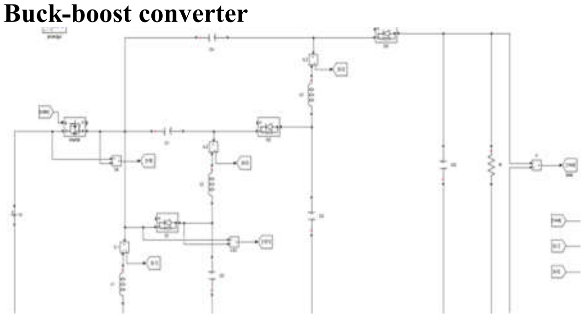
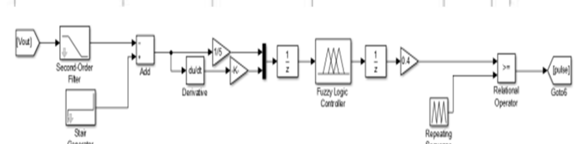


Fig. 15. Waveforms of Buck converter (a) output voltage, (b) inductor L1 current, (c) inductor L2 current, (d) inductor L3 current, (e) diode D1 voltage, (f) switch S voltage.

Buck-boost converter





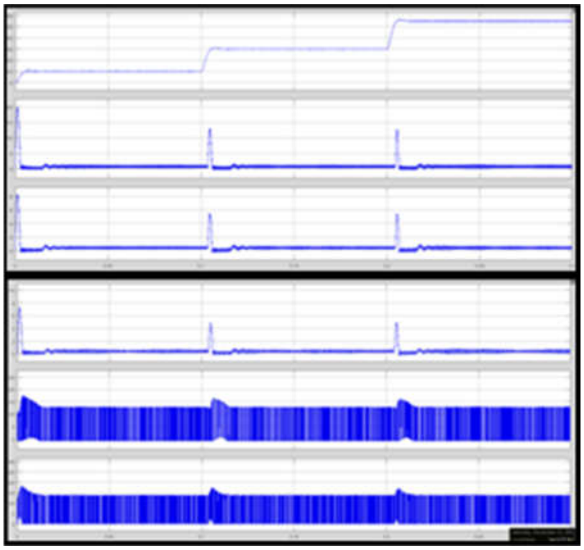


Fig.15 Waveforms of Buck-boost converter (a) output voltage, (b) inductor L1 current, (c) inductor L2 current, (d) inductor L3 current, (e) diode D1 voltage, (f) switch S voltage.

CONCLUSION

In this a single switch Nonisolated Buck–Boost Dc–Dc Converter was proposed. The structure of the presented buck– boost converter is simple. In the proposed converter, only one main switch is utilized, which decreases the conduction loss of power switch and improves efficiency. The voltage stress across the power switch is low and switch with low on-state resistance can be selected.

The step-up voltage gain of the proposed buck–boost converter is higher than that of the classic boost, buck converters and are compared in this paper using MATLAB software. The proposed converter has simple structure; therefore, the control of the presented converter will be easy. The buck–boost converter is utilized in many applications like gadgets such, as mobile phones and notebooks, fuel-cell systems, car electronic devices, and LED drivers. Finally, the experimental results were provided to verify the feasibility of the proposed converter.

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