# Optimization of The Breakdown Voltage of Soi Ldmos Using Tcad

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**Abstract- At first, SILVACO simulation tool is used to develop the simulation method and to study the devices. The threshold voltage influenced by the substrate bias on SOI LDMOSFET was discussed.**

**To remove effect of back gate bias of LDMOSFET a modified SOI design is optimized here. It improves the breakdown voltage with high margin. A buried layer of low doping silicon is introduced in between the SOI layer and silicon. This buried layer thickness plays a significant role in affecting strong inversion condition for the capacitor of the back MOS of new proposed diode.**

**Keywords- Silicon on Insulator (SOI), Lateral Diffused Metal-Oxide-Semiconductor Field Effect Transistor (LDMOSFET), Technology Computer Added Design (TCAD), Optimization, Breakdown. Low doped buried layer (LDBL)**

## 1. INTRODUCTION

In the recent years, the semiconductor manufacturing technology proceeded at a very rapid pace. The simulation of device's characteristics is always used to reduce the manufacturing cost and time in the semiconductor industry. Therefore, it is a very

important task to investigate the simulation method and use the simulation tools to develop the design structure of devices. Today silicon-on-insulator (SOI) technology has reached a new milestone for VLSI. Concentrating to the low doped buried oxide isolation structure, the source/drain parasitic capacitance can be significantly reduced. So this technology has high-speed and lower power consumption properties. From processing point of view, the device isolation for the SOI CMOS technology is much simpler than the bulk CMOS technology. Hence, the SOI CMOS technology has a higher device density. As the n-well and p-well is absent in the SOI CMOS technology therefore the problem of latch-up which is a effect of parasitic npn and pnp BJTs in the well and substrate will not exist. Moreover, the buried oxide isolation structure will offer the excellent immunity to against high-energy particle illumination that results in the generation of electron-hole pairs and produces a large amount of current. So the leakage current that is induced by the high-energy particle radiation can be reduced. Although the buried oxide offers many benefits in the SOI structure, some drawbacks such as the self-heating and floating body effect will be emerged. In view of suppressing the floating-body effect, the body-tied 2 configuration of SOI devices is proposed [1]. At the beginning, the motivation of the development of the SOI technology was from the radiation hard properties of the SOI devices [2]. Effect of radiation on bulk semiconductor and SOI device is shown in fig 1. It is nicely observed the difference of effect in both the device. When the devices are exposed to a ray of alpha-particles, bonds are broken in the silicon region due to passing of high-energy particles and electrons-holes are generated in pair. It produces huge amount of current which will pass through drain. On the contrary for the SOI MOS device an isolation layer separates the substrate and active region. Therefore, the alpha-particle induced current has little influence in the device performance. This induced current will flow in the active region in case of bulk silicon substrate. So the characteristics is hugely affected by this. That's why, Silicon on Insulator MOS devices are better suitable to work in an open are where the device will be most exposed to radiation.

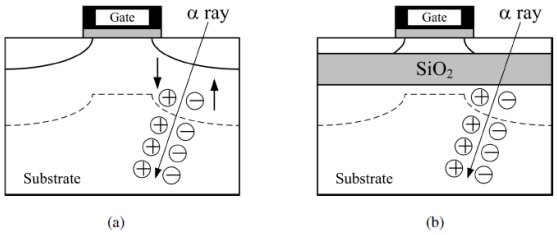


Fig-1: Radiation effect on (a) bulk and (b) SOI MOS devices

Dielectric isolation is a reliable approach for producing high voltage power ICs. Superior isolation with a low leakage current and as silicon dioxide can tolerate a higher voltage than silicon enable high-voltage lateral devices to be fabricated on a silicon-on-insulator (SOI) wafer [7]. One of the key aspects of the design of a lateral SOI power device is the reduction in the electric field along the surface of the semiconductor in the drift region. Since the area efficiency of the device is determined by its drift region length, the drift region length of a device with a given breakdown voltage should be minimized.

The substrate bias affects the high voltage performance of an SOI device [5]. The effect of the substrate bias on the breakdown voltage of a power diode constructed using SOI technology is eliminated by inserting a semi-insulating polycrystalline silicon layer (SIPOS). However, the SIPOS layer is not compatible with the standard power IC technology because SIPOS increases the leakage current over silicon interface traps. If a new approach can effectively weaken the effect of the substrate bias at low leakage current, then a novel high-breakdown voltage SOI diode can be obtained.

Silicon on Insulator technology will be grown in very near future due to the following critical reasons.

- Active areas remains isolated from the substrate to avoid any extra leakage.
- Problem of latch up and inter leakage can be completely avoided.

• Substrate coupling is effectively reduce in RF circuits. This increase quality and Q factor of the inductors.

• In mixed signal Integrated circuits Cross talk and interference is literally reduced.

• Bond breakage which generates electron hole pair and in turn creates soft errors is drastically reduced.

• Fabrication steps are easier if different potentials are required to use.

• Parasitic Capacitance is highly reduced as the junction capacitance of Source and Drain is lowered and hence device becomes faster.

• Power PCs developed by IBM are showing an enhance speed of 20% to 35% .

• Power consumption become very low as the operating voltage are lowered and parasitic componem=nts are reduced.

• Same power chips made by IBM shows a reduction of 35% to 70% in power consumption.

• This technology increases functions in the chip area because the design rules are tighter in Silicon on Insulator technology.

• It will improve performance without scaling effects.

• Fabrication steps are easy and simple.

## 2. DEVICE STRUCTURE AND PROCESS FLOW

An analysis of the substrate bias effect that affects the lateral and vertical surface potential is initially presented. A novel SOI device structure with a silicon low

doping buried layer (LDBL) is adopted to eliminate the substrate bias effect. Two-dimensional simulations of the substrate effect are performed using the SILVACO tool.

The device structure and proposed fabrication process of their SOI structure is shown in fig 2. The fabrication process of the SOI wafers is the following. First, a 0.8 μm Semi-Insulating Polycrystalline Silicon (SIPOS) layer and a 1 μm thick un-doped CVD oxide were subsequently deposited on a high resistance silicon wafer as shown in Fig. 2(a). Then, the wafer was bonded to substrate wafer as shown in Fig. 2(b). The wafer was grounded and polished to finally obtain a 5 μm thick silicon layer over the SIPOS layer as shown in Fig. 2(c). In addition, the LDBL was used to replace the SIPOS layer in the proposed structure.

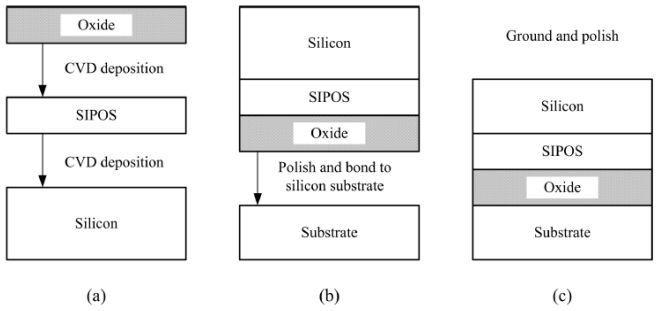


Fig-2: The process flow of the proposed SOI structure

The novel SOI structure is characterized by the insertion of a silicon LDBL between the silicon layer and the buried oxide layer. The LDBL replaces part of the depletion layer to reduce the effective substrate doping, and the absolute value of the threshold voltage is reduced.

## 3. SIMULATION RESULT AND ANALYSIS

Fig. 3 shows the influence of the breakdown characteristics of the conventional SOI LDMOSFET and the novel SOI LDMOSFET with LDBL. As was expected, it was confirmed that the back gate effect was eliminated at the novel SOI

LDMOSFET, and the breakdown voltage was increased by the LDBL.

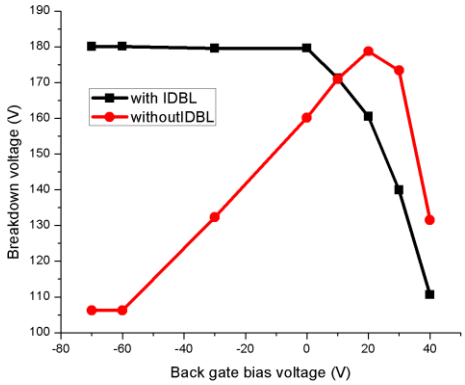


Fig-3 Effect of back gate bias voltage on breakdown voltage in the SOI

The goal of the optimization technology is proposed to design the SOI devices, when the concentration of the n-epitaxial layer varies. In order to find out the trend between the n-epitaxial layer and LDBL thickness, concentration $5\times10^{14}$ $cm^{-3}$, $2\times10^{15}$ $cm^{-3}$, and $3\times10^{15}$ $cm^{-3}$ of the n-epitaxial layer are used in the simulation. The simulated structure is the same. The optimal thickness of the concentration $5\times10^{14}$ $cm^{-3}$ and concentration $3\times10^{15}$ $cm^{-3}$ are 5.6 μm and 1.6 μm, respectively, as shown in the Fig. 4 and Fig. 5. The back MOS-C of the SOI diode is at the maximum depletion width, and the breakdown voltage does not drop as back gate bias voltage declines.

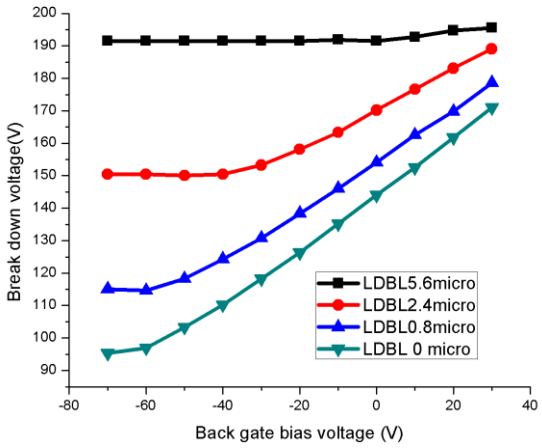


Fig 4: Effect of back gate bias voltage on breakdown voltage in SOI diode.

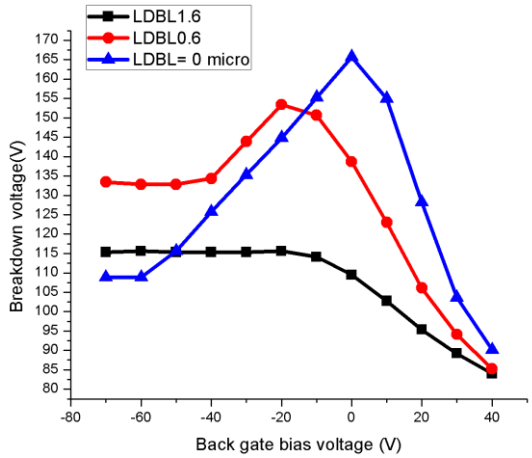


Fig 5: Effects of back gate bias voltage on breakdown voltage in SOI diode

## 4. OPTIMIZED STRUCTURE

Figure 6 shows the cross-sectional view for the proposed structure of the SOI

LDMOSFET with LDBL used in the simulation. The concentration of the n- epitaxial layer, n+ source, n+ drain, and p-body are $2\times10^{15}$ $cm^{-3}$, $1\times10^{18}$ $cm^{-3}$, $1\times10^{18}$ $cm^{-3}$, and $5\times10^{16}$ $cm^{-3}$, respectively

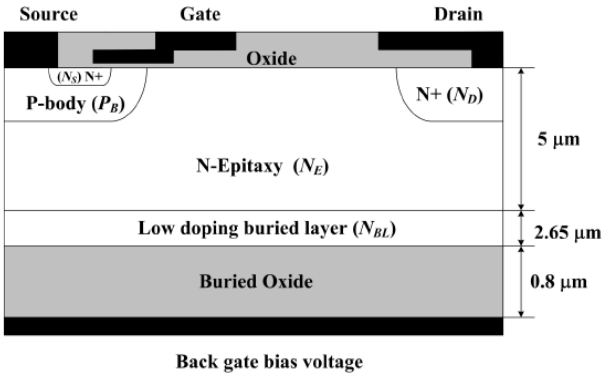


Fig-6: Cross-sectional view of the proposed structure

The structure in SILVACO window is shown in fig 7.

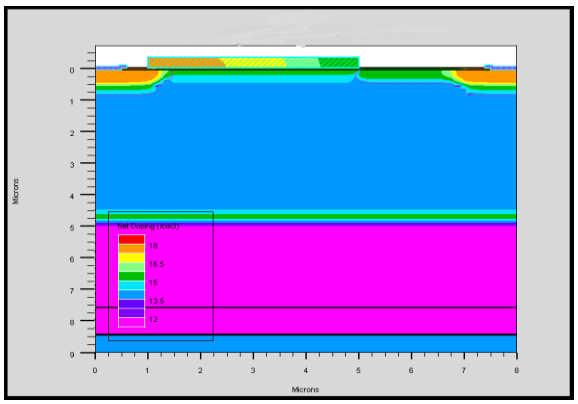

Fig-7: Structure simulated in SILVACO window

It was simulated for different thickness and concentration of LDBL. The optimal thickness of concentration $2\times10^{15}$ $cm^{-3}$ is 2.65 µm extracted. Therefore, the trend

between the n-epitaxial layer and LDBL thickness is extracted by combining the three optimal thicknesses. When the n-epitaxial layer concentration increases, the optimal thickness decreases as shown in Fig. 8.

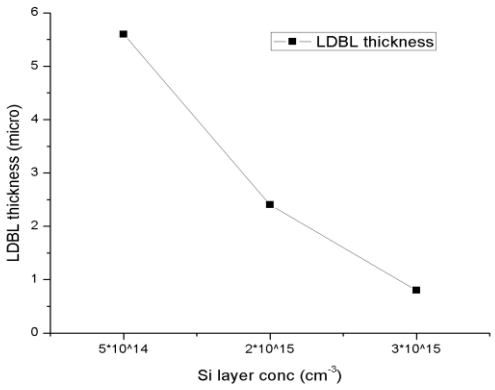


Fig. 8: Thickness of LDBL versus concentration of silicon layer.

## 5. CONCLUSION

The optimal design for eliminating the back gate bias effect of the SOI device that is characterized by an LDBL shielding layer inserted between the silicon layer and the buried oxide is predicted using SILVACO simulation tools. A comparison of the simulated results between conventional and novel structures indicates an improvement in breakdown voltage. The simple analysis presented herein in this work is useful in designing SOI power devices, such as an LDMOSFET, and lateral insulated gate bipolar transistor (LIGBT) will be adopted with LDBL.

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