Efficient Mirror Adder Design using Quantum Dot Cellular Automata

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Abstract- Quantum dot cellular automata (QCA) are a growing nano technology for the development of high performance ultra-dense low power digital circuits. QCA based numerous effective binary and decimal arithmetic circuits are implemented, however important improvements are still possible. These works determines Mirror Adder circuit design with CMOS and compare it with QCA mirror adder design. We present proportional study of mirror adder cells designed using conventional CMOS technique and mirror adder cells designed using quantum-dot cellular automata. QCA based mirror adders are superior in terms of area

1. INTRODUCTION

Quantum Dot cellular Automata (QCA) do not use transistors. QCA design addresses the concern of device density and interconnection. The elementary element of QCA is a quantum cell. Each quantum cell consumes electrons in them wherever electron diffusion take place on the columbic interaction of the electrons. QCA is an advanced research program and exertions are made to reduce the complexity of the circuits. When included size is compact to nanometers than Quantum effects such as Tunneling takes place [1].QCA circuits can be straight gained from conventional designs with addition of special clocking system. This offers very easy diffusion of predictable circuits to get transformed into QCA structures. QCA structures are designed as an array of quantum cells, where every cell has electrons in them where electrostatic interaction with its adjacent cells takes place. QCA uses a new technique for reckoning. It uses polarization upshot rather than predictable current for the transmission of information which contains the digital information. Thus a cell is accountable for the transfer of information all the way over the circuit. The basic operators used in QCA are three input majority gates and invertor. This study offers the design of different types of adders. Hence the planned design is used to reduce the area and complexity. Current transistor-based semiconductor devices are becoming resilient to scaling. For transistor circuit, the power rakishness due to leakage current is a big problem [4-7]. A possible substitute to these problems is Nanotechnology based Quantum-dot cellular automata (QCA) circuits [7-8]. The emphasis of this paper is on project of efficient Mirror adder circuit [3]. Prior to our work on mirror adder we scrutinized some prior works on adder circuits in QCA technology. J. Cocorullo, Giuseppe planned Design of Efficient BCD Adders in Quantum Dot Cellular Automata [4]. An Efficient Design of Full Adder in Quantum-Dot Cellular Automata (QCA) Technology is shown by M. Mohammadi, S. Gorgin [9]. Efficient Design of a Hybrid Adder in Quantum-Dot Cellular Automata is presented by V. Pudi and K. Sridharan [12]. M. Gladshtein

exhibited Quantum-Dot Cellular Automata Serial Decimal Adder [14]. M. Sangsefidi, M. Karimpour and M. Sarayloo proposed Efficient Design of a Coplanar Adder/Subtractor in Quantum-Dot Cellular Automata [16]. H. Cho and E. E. Swartzlander exhibited Adder and multiplier outlines in quantum-dot cell automata [17].We have exposed plan of Mirror Adder in QCA and compared these outcomes and CMOS technology. To the best of our facts, there is no earlier work that has analyzed design of Mirror Adder in QCA. Improvement in positions of area of the order of three was gained in our QCA based strategies.

2. QCA PRELIMINARIES

In this segment, the edifice unit i.e. QCA cell, general logic, and gates in QCA are explored in the directive of QCA cell, QCA wires, majority gates, inverter, AND-OR gates.

2.1 QCA Cell

The primitive cell in QCA technology, as exposed in Fig.1 (a), is a square-shaped cell. It covers four quantum dots at each crook of the cell. The quantum dot generally comprises two electrons in each cell, which lodge two dots of the cell. Due to the Coulombic repulsion amid the electrons, the electrons incline to dwell in the place which has inferior repulsion force amid them and electrons can inhabit stable states. Hence, they occupy the diagonal place within the cell. There are two means possible for the placement of electrons as shown in Fig.1 (b). Therefore, two divisions are possible. If the electrons lodge the situation as shown in Fig.1 (b) then it resembles to polarization "1" i.e. logic 1 and if is settled as shown in Fig.1(c) then it is in polarization "-1" i.e. logic 0 states. These 2 extra moveable electrons can quantum mechanically tunnel amid dots, but not cells. Hence unlike conformist digital circuits in which information is passed by the flow of electric current, QCA operates by the Columbic collaboration that joins the state of one cell to its fellow cell state.

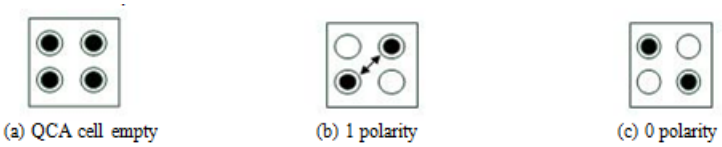


Fig.1 QCA cell

2.2 QCA wire and types

In order to transmit the information from one cell to another, a QCA wire is needed. The wire consists of a chain of cells where the cells are also coupled to each other. The logic values are delivered from one cell to the next cell due to the coulomb interaction. The polarization of the input cell is voyaged down the wire. As a result, the agreed system attempt to settle down to a ground state. Due to electron dislike if the polarization of one cell variations, it imposes its end-to-end cells to change its formal as shown in Fig.2.

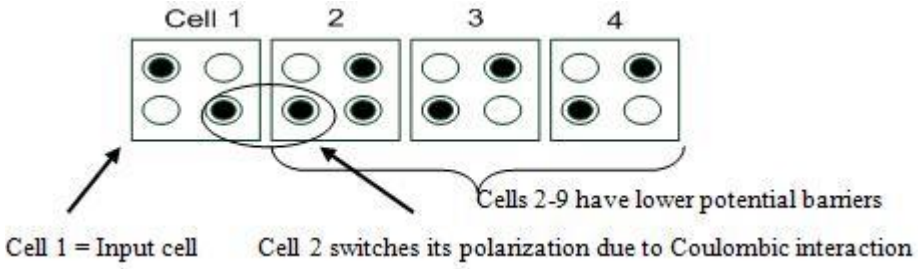
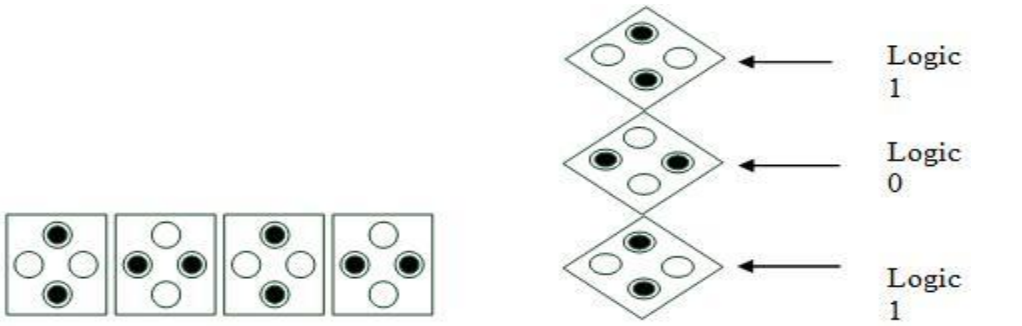


Fig.2 QCA Wire



(a) 90° wire (b) 45° Wire

Fig.3 QCA wire types

The technique of introduction quantum dots in the square cell kinds it possible to have two types of alignment. The first one is called as 90° wire and the alternative is 45° as shown in Fig.3(a) and 3(b) in which each other cell with contradictory split is put organized.

2.3 Majority gate

Majority gate is one of the important gates of QCA. It is shown in Fig.4 which is a 3-input majority function. The output is merely the majority of the 3 inputs useful. Presumptuous the inputs is A, B, and C, the Boolean function of the majority gate is,

$$M(A, B, C) = AB+AC+BC \quad (1)$$

Now if we fix the polarization of one input to logic "0", say B, then equation (1) can be likened as follows:

$$M(A, 0, C) = A.0+AC+0 = AC \quad (2)$$

Hence equation (2) is basically the AND operation between A and C input. Similarly if we placed the input B value equals to "1" then,

$$M(A, 1, C) = A.1+AC+1.C = A+C+AC = A(1+C)+C = A+C \quad (3)$$

Equation (3) is an OR operation among A and C. Thus by variable the cost of any of the input, the 3-input majority gate can role as AND gate and OR gate.

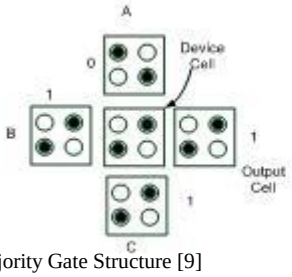


Fig.4 Majority Gate Structure [9]

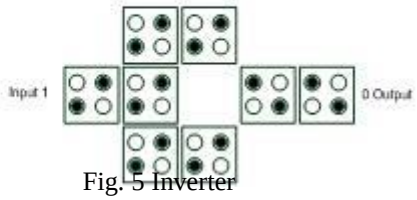
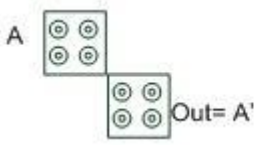


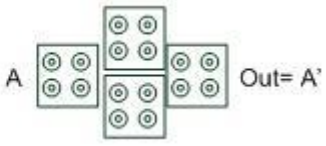
Fig. 5 Inverter

2.4 Inverter gate

There are numerous ways to do it in the QCA prototype that one is shown in Fig.5.In fig. (a), the signal derives from the left, splits into two corresponding wires, and is inverted at the point of junction [1]. The other procedure used to style inverter hawser as shown in Fig.5 (b) and 5 (c).



(b)



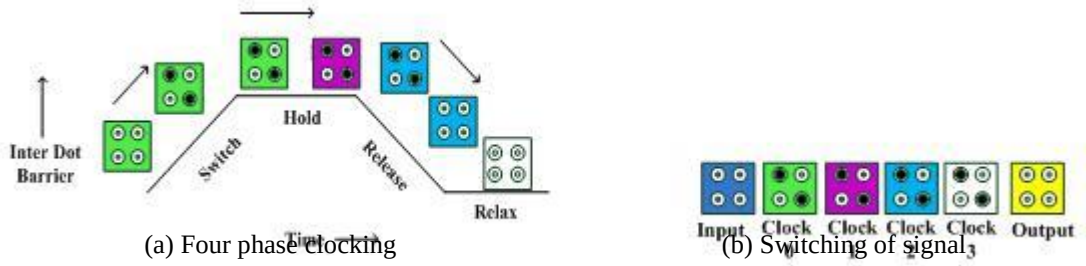
(c)

Fig.5 (a), (b), (c) Three different way to make inverter in QCA

However, settlement of two cells such that they slant via only one bend hints to switch from -1 logic to +1 logic or vice versa as shown in Fig.5(b).

2.5 QCA clocking scheme

In VLSI design, the utility is well-ordered by a clock signal which is natural to the technology used. In difference to this, QCA reveal clocking order as the most ultimate concept to cognize. As we know there is no run of any modern signal in the transmission of facts in QCA, this does not actually means that power dissipation requisite be zero. Clocking in QCA not only advise control of information run but also true influence gain in QCA [7]. The signal energy sacrificed to the surroundings is returned by the clock secondhand. Clocking in QCA is expert by two types of switching methods for its task: abrupt switching and adiabatic switching. In abrupt switching, the inputs changes speedily and the circuit can be in some excited state; accordingly, the QCA circuit is relaxed to ground state by dispelling energy to the situation [11]. This rigid easing is ungoverned and the QCA circuit may etch a metastable state that is assumed by a local, rather than a universal energy ground state. Therefore, adiabatic switching is usually chosen; in adiabatic switching, the system is continuously kept in its rapid ground state [11]. After applying the clock signal, the electrons may either strapped to the four corner dots or pull them into the two middle dots. When the electrons are in the middle dots, the cell is thought to be in the "null" state and when the electrons are in the four corner dots, the cell is in an dynamic state. The cell in an active state is used to embodies binary "0" and "1" values as shown in fig.1. This clocking scheme (which was suggested in [7] consists of four phases: Switch, Hold, Release, and Relax, as shown in Fig.6 (a).



(a) Four phase clocking (b) Switching of signal

Fig.6 Clocking in QCA

All cells in a zone are measured by the same clock signal. Cells in each zone perform a precise calculation. During the Relax phase, the electrons are pulled into the internal dots, and the cell is in "null" state. During the Switch phase, the inter dot barricade is leisurely raised and pushes the electrons into the corner dots, so the cell attains a absolute polarity under the domination of its neighbors (which are in the Hold phase). The operation of fig.6 (b) is summarized below:

- Through the first clock phase, the switch phase, the inter-dot potential barriers are short. The barriers are then higher during this phase and the QCA cells become opposed allowing to the state of their driver (i.e. their input cell).It is in this clock phase that the actual reckoning occurs. By the end of this clock phase, barriers are high enough to defeat any electron tunneling and cell states are fixed.
- During the second clock phase, the hold phase, barricades are seized high so the outputs of the sub-array can be used as inputs to the succeeding stage.
- In the third clock phase, the release phase, barricades are lowered and cells are allowed to diminish to an un polarized state.

Finally, during the fourth clock stage, the relax phase, cell barriers remain dropped and cells continue in an un polarized state

3. PROPOSED CIRCUIT AND PRESENTATION

3.1. Adders Circuits

In this section, we deliberate for planning full adder Circuits by QCA. Since the mirror adder is one of the approximately utilized reasonable implementations of the full adder in CMOS technology, we use it as our source for suggesting full adder circuits using QCA [3].

3.2. Conventional mirror adder

Table 1. Truth Table of full adder circuit Inputs Outputs

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 5 shows the transistor level schematic and figure 6 shows the layout [3] of a conservative Mirror Adder (using CMOS Technology). It consists of a total of 24 transistors.

$$Sum = ABCin + A^{-} B^{-} Cin + A^{-} BC^{-}in + AB^{-}Cin$$

$$Cout = AB + A^{-} BCin + AB^{-} Cin.$$

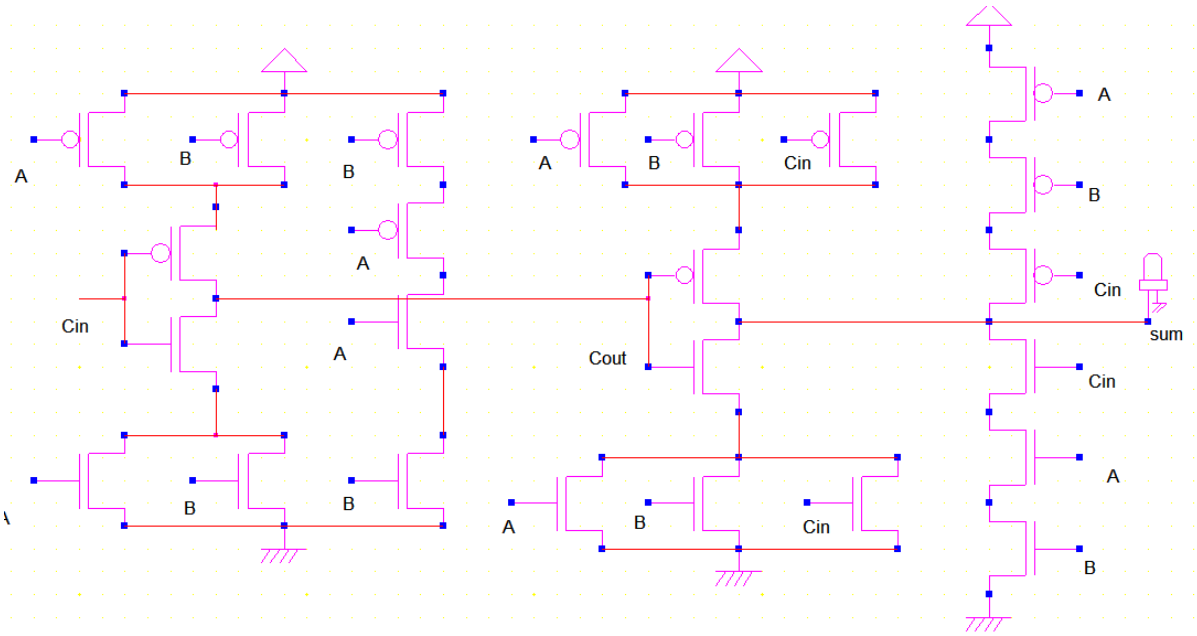


Fig.7 Transistor Level schematic of Mirror Adder [3]

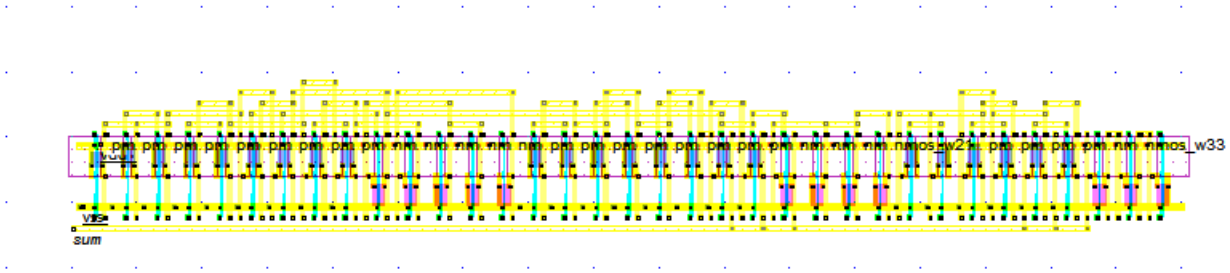


Fig.8 Layout of Mirror adder using CMOS Technology[3]

3.3 Mirror adder using QCA

In this fragment, we show layout got from QCA Designer and the simulation results for Mirror Adder. Cells for our design are assumed to have a dimension of 18*18 nm while the quantum dots have a

Figure 7 shows the QCA Designer layout of Mirror Adder while figure 8 gives the corresponding

SIMULATION RESULTS.

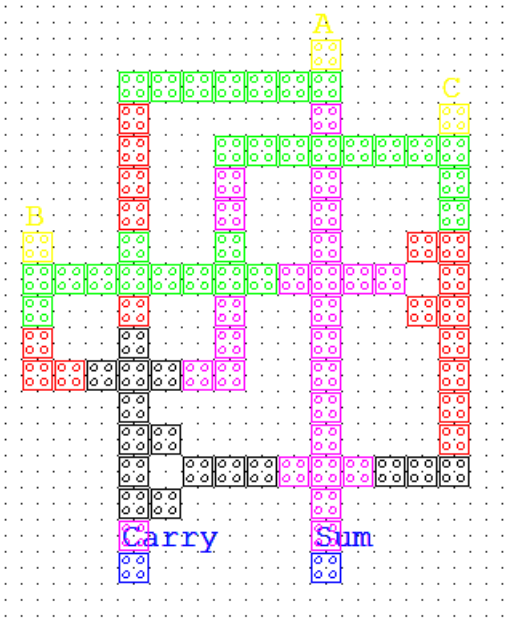


Fig. 9. Layout of Mirror Adder using QCA

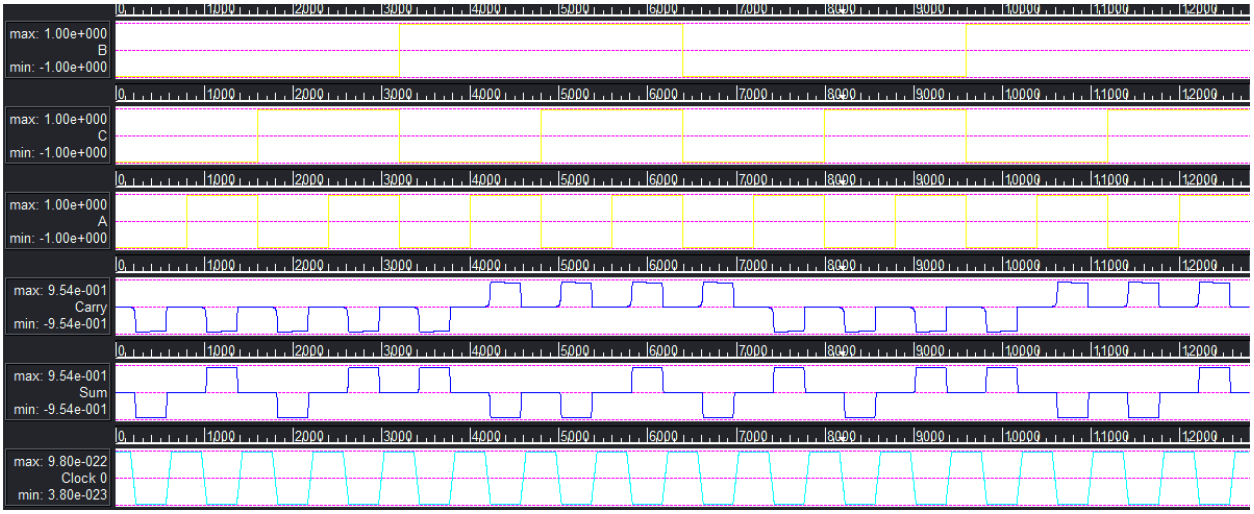


Fig.10. Simulation Output of Mirror Adder

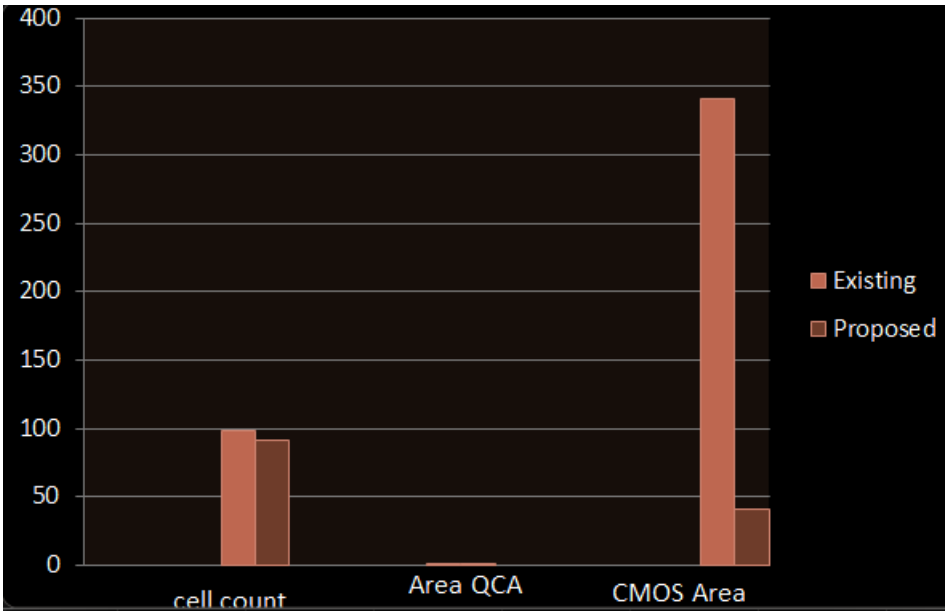


Fig.11 Layout area and number of cell comparison between QCA and conventional CMOS mirror adder

4. CONCLUSION

With respect to table 3, we observe that the no. of cells and area, for QCA Mirror Adder is less as Compared to conventional Mirror Adder. Our comparison results are based on Mirror based on 90-nm CMOS technology and Mirror Adder with QCA technology. A quantum dot cellular automaton is a future nanotechnology architecture for computing, best alternative for CMOS technology. QCA offers a new method of reckoning and information alteration. We have examined a several aspect of QCA method with their working methodology. These designs give better outcomes when contrasted with the CMOS technology as far as small area, fast speed, and low power overindulgence. Now in this paper, we obligate presented efficient Mirror Adder Design using QCA. The designs are based on new concepts concerning majority logic gate. Comparisons with conventional Mirror Adder and QCA Mirror Adder[11] are presented. Detailed simulation results are also given.

ACKNOWLEDGEMENT

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