Design of Coplanar Full Adder in Quantum-Dot Cellular Automata

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Abstract- Quantum-dot cellular automata are one of the most significant developing technologies for designing nano-electronic circuits. One of the important functions in arithmetic circuits is the one-bit full-adder cell. Moreover, in QCA field coplanar buildings are very essential because using this approach; we can shorten the employment of this function. A single layer full-adder cell is presented based on difference phase request. We have attained momentous perfections in terms of complexity, area. Predominantly simulation results show 35 % decrease in complexity and area. We have also proposed a coplanar 2-input XOR gate founded on the proposed full-adder cell. Even though, the main idea in this is just comparing and appraising the CMOS adder to the QCA adder in expressions of area and number of cells.

1. INTRODUCTION

QCA (Quantum-Dot Cellular Automata) is one of the six encouraging technologies for nano-scale computing registered in the International Technology Roadmap for Semiconductors (ITRS) 2004 [2]. The essential idea for QCA operation is to encode evidence using the charge conformation of a set of dots. This is an important disruption with the transistor example. A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells restraining free electrons. Each cell has four quantum dots which can retain a single electron per dot. The four dots are situated in the corners of a square structure. The cell can be charged by two free electrons which can tunnel concluded to neighboring dots. By the clocking

mechanism, the electrons tunnel done to the proper position during the clock conversion. Unlike CMOS, in QCA the

transmission media and logical elements are together included of the same basic block - the cell[4]. As such, QCA has been named “processing-in-wire.” The interconnects intended with QCA would be faster and would work practically up to the speed of the processing device which would extremely enhance the system performance. Quantum cellular automata technology would be jumble-sale in the future for evolving a high speed mainframes and ASICS that would be used for together general resolution and task-specific computing necessities. QCA has significant benefits in terms of speed and area over CMOS technology, for instance. On the other hand, QCA has fascinated much more attention for the reason that it has many advantages, such as ultra-low-energy depletion, fast operation and high device compactness. Normally, the QCA is distributed into 4 types; Metal-Island, Semiconductor, Magnetic and Molecular where Metal-Island as well as, semiconductor types are centered on silicon. In order to contrivance molecular types, one founded on graphene has attracted courtesy. Our proposed work is appropriate for using in Semiconductor and Metal Island types. Subsequently in these types, their cell instructors are in square shape, but further types of QCA such as Magnetic and Molecular in overall tool thru a rectangular shape. In addition, QCA Designer tool works based on Semiconductor type. So we just can simulate this category. With the use of QCA cell, we are able to encode binary statistics, so this construction is suitable for binary reckoning because in every cell there are 4 quantum dots which can provide two types of coding. The adder cell is an indispensable element in the design of arithmetic circuits based on QCA technology. In further words, operative design of the new adder cell can be functional most meritoriously for the entire system. One can achieve many improvements in poles apart parameters. In addition, as in VLSI circuits speed, area and power are the most significant routine evaluation parameters. In order to provide a widespread analysis, in this study, energy dissipation analysis is also calculated. In this study, we recommend an area and energy efficient one-bit coplanar full-adder cell. The modified design delivers many advantages counting single layer execution, lower energy dissipation, lower number of cells and smaller area. The residue of this paper is prepared as follows: The QCA fundamentals and the related works are revised in the Sections 2 and 3, respectively. Section 4 provides definitions of the proposed method. Simulation results and comparisons are accessible in Section 5. Finally, Section 6 concludes the paper.

2. QCA PRELIMINARIES

In this segment, the erection unit i.e. QCA cell, general logic, and gates in QCA are scrutinized in the order of QCA cell, QCA wires, majority gates, inverter, AND-OR gates.

2.1 QCA Cell

The embryonic cell in QCA technology, as shown in Fig.1 (a), is a square-shaped cell. It comprises four quantum dots at every corner of the cell. The quantum dot generally contains two electrons in each cell, which vacate two dots of the cell. Due to the Coulombic repulsion between the electrons, the electrons tend to reside in the position which has lower revulsion force between them and electrons can occupy steady states. Hence, they inhabit the diagonal location within the cell. There are two methods possible for the assignment of electrons as shown in Fig.1 (b). Therefore, two divergences are possible. If the electrons inhabit the position as shown in Fig.1 (b) then it resembles to polarization "1" i.e. logic 1 and if is organized as shown in Fig.1(c) then it is in polarization "-1" i.e. logic 0 states. These 2 extra mobile electrons can quantum instinctively tunnel between dots, but not cells. Hence unlike conservative digital circuits in which information is approved by the flow of electric current, QCA functions by the Coulombic interaction that joins the state of one cell to its neighbor cell state.

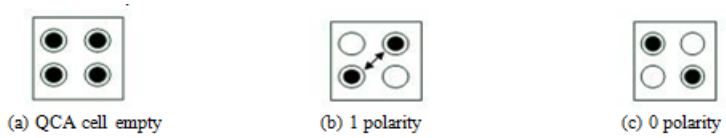


Fig.1 QCA cell

2.2 QCA wire and types

In order to communicate the information from one cell to another, a QCA wire is desirable. The wire contains of a chain of cells where the cells are also attached to each other. The polarization of the input cell is moved down the wire. As a result, the agreed system effort to settle down to a ground state. Due to electron revulsion if the polarization of one cell changes, it imposes its adjacent cells to change its state as shown in Fig.2.

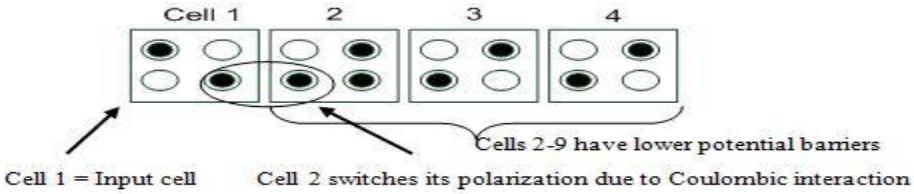
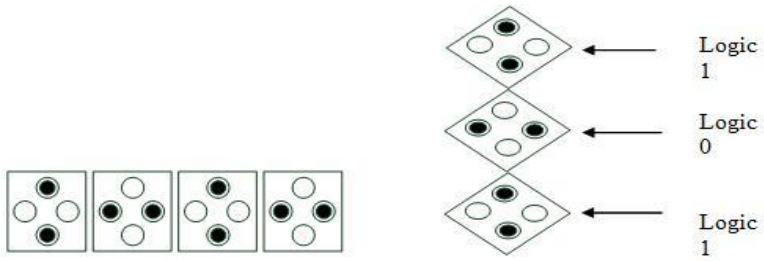


Fig.2 QCA Wire



(a) 90° wire (b) 45° Wire

Fig.3 QCA wire types

The technique of employing quantum dots in the square cell makes it conceivable to have two types of alignment. The first one is called as 90° wire and the second is 45° as shown in Fig.3(a) and 3(b) in which every other cell with conflicting polarity is put together.

2.3 Majority gate

Majority gate is single of the essential gates of QCA. It is shown in Fig.4 which is a 3-input majority purpose. The output is just the majority of the 3 inputs pragmatic. Supposing the inputs is A, B, and C, the Boolean function of the majority gate is,

$$M(A, B, C) = AB+AC+BC \quad (1)$$

Currently if we hit the divergence of one input to logic "0", say B, then equation (1) can be equated as trails:

$$M(A, 0, C) = A.0 + A.C + 0 = AC \quad (2)$$

Henceforward equation (2) is just the AND operation between A and C input. Correspondingly if we put the input B value equivalents to "1" then,

$$M(A, 1, C) = A.1+AC+1.C = A+C+AC = A(1+C)+C = A+C \quad (3)$$

Equation (3) is an OR operation amid A and C. Thus by altering the value of any of the input, the 3-input majority gate can purpose as AND gate and OR gate.

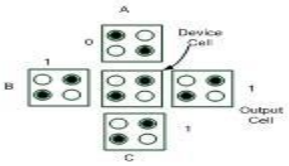


Fig.4 Majority Gate Structure [9]

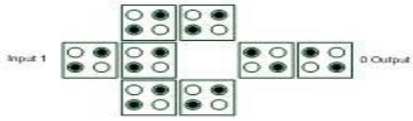
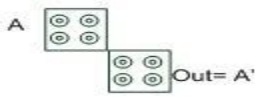


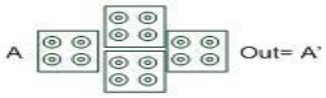
Fig. 5 (a) Inverter

2.4 Inverter gate

There are multiple methods to do it in the QCA prototype that one is shown in Fig.5.In fig. (a), the signal originates from the left, ruptures into two parallel wires, and is overturned at the point of junction [1]. The other arrangement used to mark inverter chain as shown in Fig.5 (b) and 5 (c).



(b)



(c)

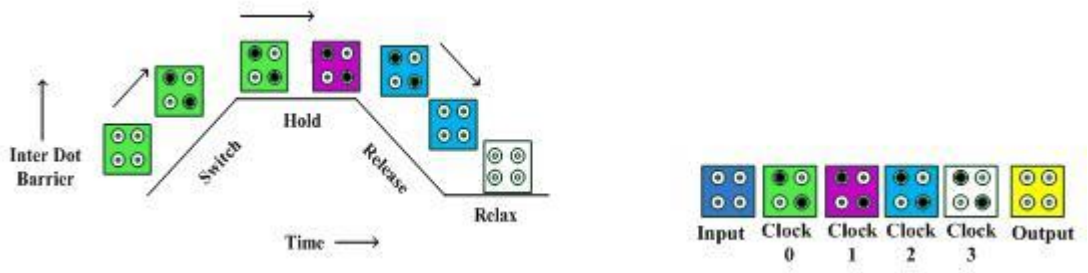
Fig.5 (a), (b), (c) Three various way to make inverter in QCA

Conversely, placement of two cells such that they method via only one corner indications to shift from -1 logic to +1 logic or vice versa as shown in Fig.5(b).

2.5 QCA clocking scheme

In VLSI design, the purpose is precise by a clock signal which is essential to the technology used. In contrast to this, QCA demo clocking system as the most fundamental perception to comprehend. As we know there is no stream of

any prevailing signal in the propagation of information in QCA, this does not essentially means that power dissipation need be zero. Clocking in QCA not only converse controller of information flow but also true power gain in QCA [7]. The signal energy be deprived of to the environment is renovated by the clock used. Clocking in QCA is consummate by two types of switching methods for its operation: abrupt switching and adiabatic switching. In abrupt switching, the inputs fluctuations unexpectedly and the circuit can be in some excited state; therefore, the QCA circuit is comfortable to ground state by dissipating energy to the environment [11]. This unbendable relaxation is ungoverned and the QCA circuit may engrave a metastable state that is comprehended by a local, rather than a global energy ground state. Therefore, adiabatic switching is typically preferred; in adiabatic switching, the system is continuously kept in its instantaneous ground state [11]. After applying the clock signal, the electrons may either lacking to the four corner dots or pull them into the two middle dots. When the electrons are in the middle dots, the cell is said to be in the "null" state and when the electrons are in the four corner dots, the cell is in a vigorous state. The cell in an active state is used to embodies binary "0" and "1" values as shown in fig.1. This clocking structure (which was recommended in [7] consists of four phases: Switch, Hold, Release, and Relax, as shown in Fig.6 (a).



(a) Four phase clocking (b) Switching of signal

Fig.6 Clocking in QCA

Entirely cells in a zone are controlled by the same clock signal. Cells in each zone perform a particular calculation. During the Relax phase, the electrons are dragged into the middle dots, and the cell is in "null" state. During the Switch phase, the inter dot fence is unhurried raised and pushes the electrons into the corner dots, so the cell gets a conclusive polarity below the dominance of that one neighbors (which are in the Hold phase). The operation of fig.6 (b) is abridged below:

(i) During the first clock phase, the switch phase, the inter-dot potential barricades are low. The barriers are then raised up during this phase and the QCA cells converted polarized according to the state of their driver (i.e. their input cell).It is in this clock phase that the genuine reckoning occurs. By the end of this

clock phase, barriers are high sufficient to suppress any electron tunneling and cell states are stationary.

(ii) Throughout the second clock phase, the hold phase, barriers are held high so the outputs of the sub-array can be secondhand as inputs to the next stage.

(iii) In the third clock phase, the release phase, barriers are lowered and cells are allowable to diminish to an un polarized state.

Finally, during the fourth clock phase, the relax phase, cell barriers endure dropped and cells persist in an un polarized state

3. PROPOSED CIRCUIT AND PRESENTATION

3.1. Adders Circuits

In this segment, we discourse for designing full adder Circuits by QCA. Since the mirror adder is one of the largely exploited inexpensive implementations of the full adder in CMOS technology, we use it as our basis for suggesting full adder circuits using QCA [3].

3.2. Conventional mirror adder

Table 1. Truth Table of full adder circuit Inputs Outputs

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 5 shows the transistor level diagram and figure 6 demonstrations the layout [3] of a conventional Mirror Adder (using CMOS Technology). It consists of a total of 24 transistors.

$$Sum = ABCin + A^{-} B^{-} Cin + A^{-} BC^{-}in + AB^{-}Cin$$

$$Cout = AB + A^{-} BCin + AB^{-} Cin.$$

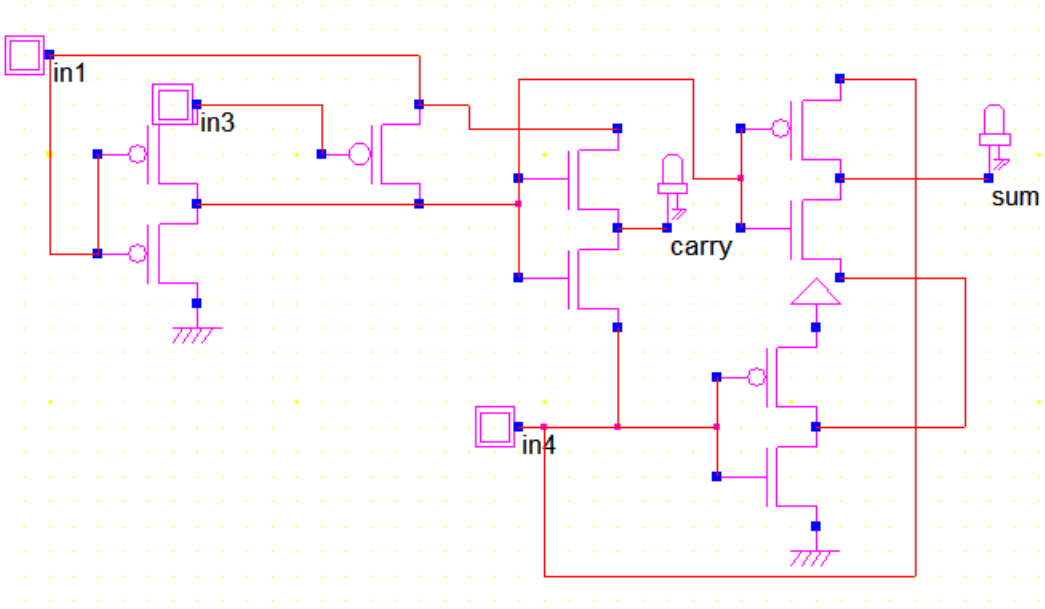


Fig.7. Circuit of 1 bit CMOS Coplanar Full Adder

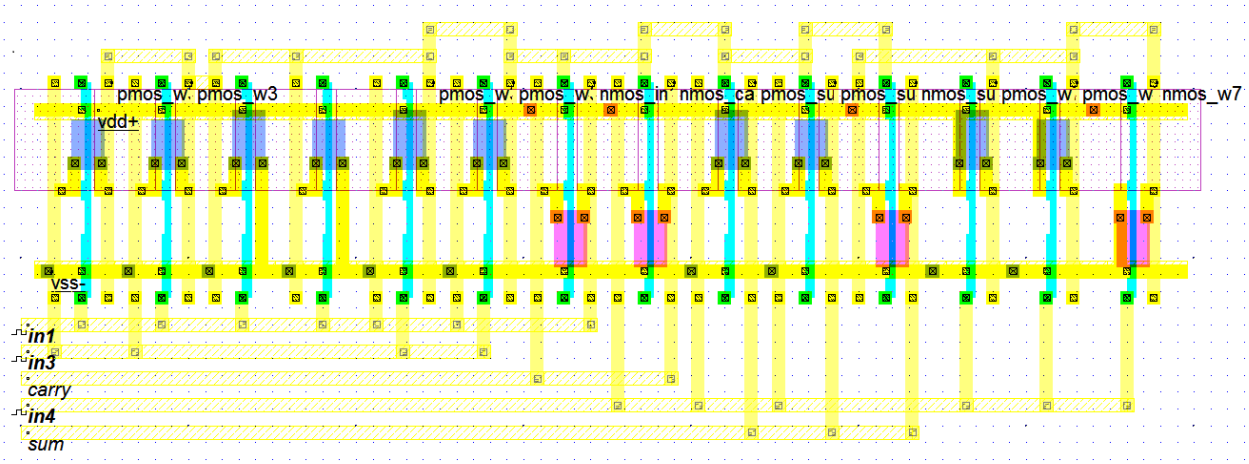


Fig.8. Layout of 1 Bit CMOS Coplanar Full Adder

3.3 Proposed XOR Gate

XOR is a digital logic gate. It gives a low output (0), if both inputs are low or both are in height. If one, and only one, of the inputs to the gate are high, the output will be correct (1). In these work two various QCA based XOR gates have been planned to develop an efficient construction. In order to proposal two inputs XOR gate, different constructions are proposed, but most of the scholar's designers are based on three stages: "AND" stage, "NAND" stage and "OR" stage. Where, "a" and "b" are the inputs, "Out" is the output signal as shown in Fig. 9. "Out".

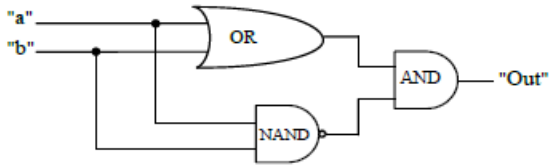


Fig.9 Schematic of XOR Gate

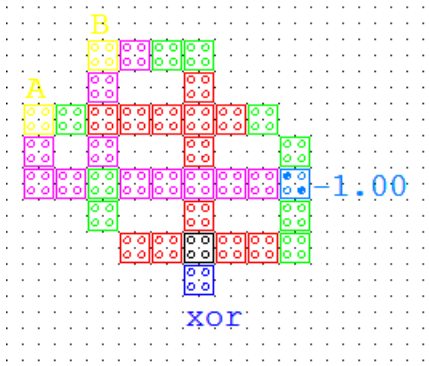


Fig.10. Proposed QCA XOR Gate

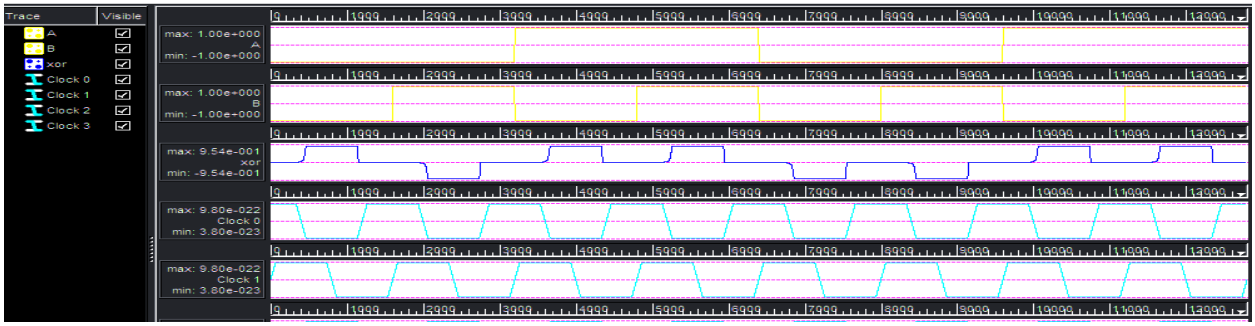


Fig.11. Output of Proposed XOR Gate

3.4 Proposed Full Adder

The existing adder is unavailable by the paper G. Singh et al[4] in this design there is 47 cells are using for 1 bit full adder designing and planned adder encompasses 37 cell for full adder operation.

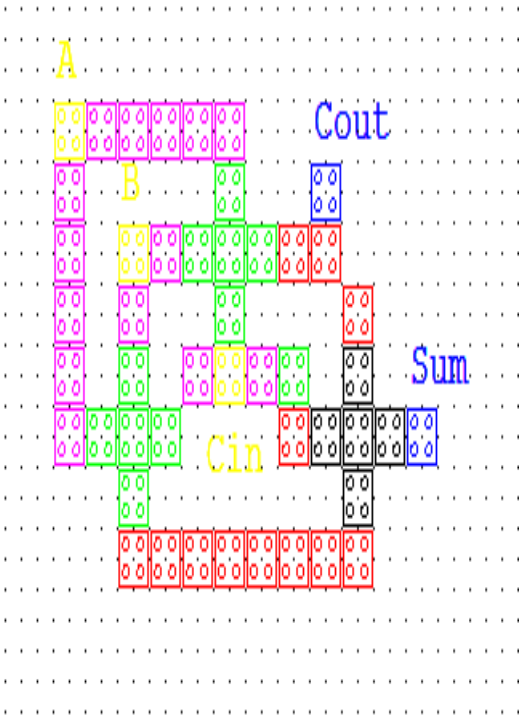


Fig.12. Existing Full Adder[4]

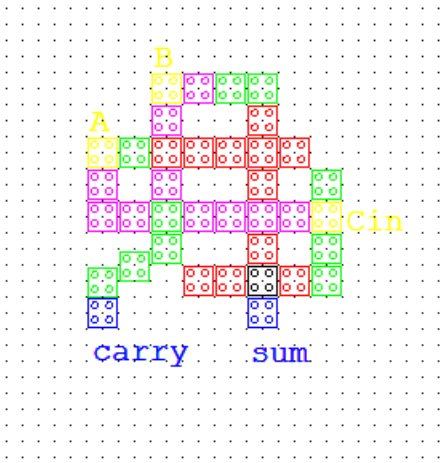


Fig.13. Proposed 1 bit coplanar full adder

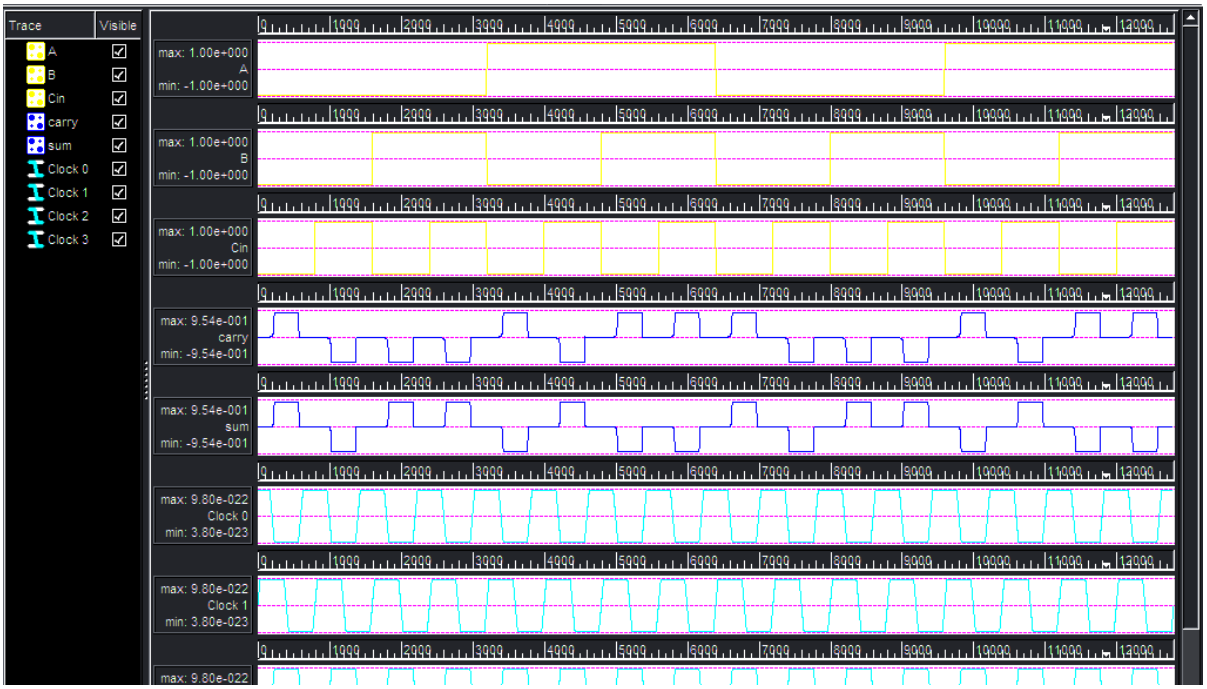
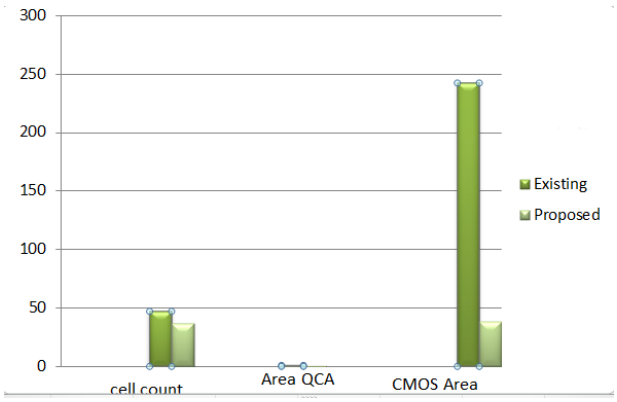


Fig.14 Output of Proposed 1 bit Co-planar adder



CONCLUSION

In this learning, energy effectual with compact area solitary layer full-adder cell in quantum-dot cellular automata was obtainable. This structure can be used for designing a QCA circuit using one single layer having low energy dissipation. Moreover, the location of all input and output cells are positioned on the outsides; thus, an improved physical supervision can be performed. In comparison to the best-published outcomes, the planned design improved in expressions of intricacy area and power consumption. The simulation results accomplished using QCA Designer specify the dominance of the proposed designs in terms of performance, area and energy dissipation. In conclusion, a new coplanar 2-input XOR gate grounded on the planned full adder cell was obtainable.

ACKNOWLEDGEMENT

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