Sub Threshold Analysis of Ultra-Low Power, Highly Reliable, and Nonvolatile Hybrid CMOS

P. Kavya
M.Tech Scholar, Department of ECE
Baba Institute of Technology and Sciences, Visakhapatnam.
puttakavya18@gmail.com
Pradeep Kondapalli
Associate Professor, Department of ECE
Baba Institute of Technology and Sciences, Visakhapatnam.
pradeepbitsvizag@gmail.com

Abstract- Very large-scale integrated circuit (VLSI) design, created on today's CMOS technologies, are frontingnumerous challenges. Sinking transistor dimensions, reduction in threshold voltage, and dropping power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design trials, hybrid MTJ/CMOS based design can determination the matter of leakage power and bring the gain of non-volatility. However, radiation-induced spineless error is still a subject in such new designs as they need outlying CMOS components. As a result, these magnetic-based circuits are tranquil susceptive to radiation things. This workoffers a radiation tough and low power magnetic full-adder (MFA) for progressive microprocessors. Associating with the previous work, the anticipateddesign is capable of abiding any particle strike nevertheless of the tempted charge. Besides, our circuit offers lesser energy consumption in write operation as compared with previous matching part. One of the most essentialstructures for the electronic system is vitality. Adders are the commonly used devices for the handy electronic systems such as for the DSP operations and processor based applications. In this paper we are executing the full Adder design using hybrid-CMOS logic style by isolating it in modules so that it can be optimized at several levels. The adder circuit which we are executing is hybrid CMOS logic based full adder. Planned full adder will be designed by merging three modules. Here we will not represent those three modules as a schematic. The proposed design area wise compact and with reduced power consumption.

1. INTRODUCTION

As we know the major apprehension in VLSI is about area, speed and power. But essentially there is no much rank given to the power when likened to the speed and area in VLSI circuits. But as per the current upward technology, power has become placing a major role to decrease the power consumption of the electronic circuits. In these applications, average power ingesting is a grave design concern. In the lack of low-power design systems then, current and future transportable devices will agonize from either very short battery life or very hefty battery pack.

To lessens this power consumption and for good battery life we are recommending a Hybrid-CMOS [1] logic design of the Full adder. Full adder is a simple block for several arithmetic circuits such as multipliers, compressors, comparators etc. The power consumption, prerequisite and output delay of arithmetic circuits is assuredly depending upon the power constraint and delay of the full adder circuits. So for crafty the high performance arithmetic circuits, minimization of the delay and power of the full adder circuit is compulsory.

Along with the diminution in CMOS dimension as well as supply voltage, sympathy to fallout effects is increasing [1-2]. Moreover, further trials such as developmentdeviation and leakage power are becoming more and more about [2-4]. Diminution in threshold voltage results in leakage power surge [5-8]. When an energetic subdivisionattacks an off-state transistor in an SRAM cell, it could modify the kept logic value. This soft error is named single event upset (SEU) [1-2]. SEU is a soft error for sequential logic and can gross place more easily due to the CMOS scaling down [2, 8]. Magnetic-based logics can be ansubstitute choice for dealing with the declared challenges of the CMOS logics [4].

Hybrid MTJ/CMOS memory and logic design offers some illustrious features such as very low power ingesting, no volatility, high resolution, and an easy 3D addition with CMOS technology [6-9]. Heretofore, a number of MTJ/CMOS-based logic and memory circuits are recommended in the literature [11-17]. In [11], a magnetic latch (mlatch) (shown in Fig.2) is proposed. This circuit includes a CMOS sequential logic for interpretation the state of MTJs (the sense amplifier), a CMOS combinational logic for reconfiguring the MTJs (the write circuit) and also two MTJ cells. The proposed mlatch circuit suggestions lower power feeding and also nonvolatility in assessment with the CMOS latches [16]. Though, the plannedmlatch is susceptive to radiation-induced SEUs. In [12], another mlatchhealthy against radiation is planned. This mlatch uses four MTJs instead of two and therefore, suffers from a high energy consumption for write operation. As conversed in [13-14], at least 90% of total energy consumption in magnetic-based memory/logic circuits is rummage-sale for the write operation to reconfigure the MTJs. Extra radiation hardened (rad-hard) mlatches are planned in [11-12]. In [5-6], simple unprotected magnetic flip-flops (MFF) are proposed. In [17], a rad-hard version of MFF offering an SEU-tolerance capability in addition to the advantages of MFFs suggested in [15-16] is proposed. Magnetic full-adder (MFA) circuits are also suggested in literature [6-7]. The planned MFA circuits offer an almost zero leakage current in reserve mode. However, as we show in section II, these MFA circuits cannot assurance a fault free operation in the company of radiation effects. This paper proposes a rad-hard MFA (the so-called RH-MFA) that is capable of acceptance particle strikes with any quantity of energy level. Over the previous work, the planned RH-MFA uses only single reconfigurable MTJ and devours a lower write-energy. We also, suggested a serial rad-hard and also a full-nonvolatile rad-hard MFA based on the proposed RH-MFA.

2. RELATED WORK

One of the main streams of VLSI Design is CMOS Technology. Dynamic or switching power is unique of the major mechanisms of total power consumption in 0.18μ technology and overhead. But static or Leakage power rules the dynamic power when technology topographies size specialists below 0.13μ technology. Several methods to decrease the leakage power have been planned by the designers [12]. The methods planned by V.Elamaran et al.[1] is a

judgment study of a one-bit adder using different methods to decrease static power dissipation in digital circuits such as lethargic, load, sleepy stack and sleepy keeper slants but in all methods the area unavailable, delay and also the static power feasting is more. Pushpa Saini et al.[2] proposed new methods such as Sleep Transistor approach with NMOS, Sleep forced NMOS load, Variable body biasing through bypass for the reduction of leakage power in 90nm technology. The designed methods were associated with the previous leakage reduction methods. The sleep technique is combined with the supplementary techniques as sleep is state negativemethod and hence these methods dwell inextra area An ultra low power non-volatile CMOS full adder by RaminRajaei et al.[5] is a low power Magnetic Full Adder (MFA) that can be secondhand in advanced microprocessors, the MFA that is calculated is talented of tolerating Single Event Upset (SEU) which is triggered by particle assault without considering the tempted charge when linked with the previous work. In the above proposed method the first MFA circuit changes the state when a particle attack and the circuit proposed to stunned this problem is complex circuits with increased number of transistors.

To reduce the leakage power Shashank Gautam [14] planned techniques like MT CMOS, power gating, dual stack, galeor and lector. A Full Adder has been measured using these techniques and power dissipation is considered and is associated with general CMOS logic of Full Adder. The lector and galeor techniques are actual when associated to other methods. Amit Kumar et al.[17] proposed a power effectualFulladder with body biasing. The Body-biasing system is discard to vary the threshold voltage to grind this adder at higher speed by sanctioning the faster gate switching. The offered design is having delay and power virtues. Erya Deng et al.[8] suggested a magnetic full-adder (MFA) design that is novel and which is based on STTMRAM with upright magnetic anisotropy (PMA). When linked with customary CMOS only full adder arrange forexpedient power efficiency and die area. This architecture sanctions scaling depressed the die area sinking energy consumption, as there is nearly zero backup power. But the MFA is more prone to fallout errors. Robust Magnetic Full-Adder with Voltage Sensing 2T/2MTJ Cell proposed by Guillaume Prenatet al.[9] is a unique symbol of Magnetic Full Adder (MFA) where all input signals are saved in non-volatile elements. Input data cin is stowed in MFA through the MTJs that are fixed, while two voltage sensing 2T/2MTJ cells stores other two input data A and B. MFA is confirmed and its low feasting, great robustness and huge speed performance merits are proved. And also the sensing error for sum and carry was zero when the size of the transistors was tripled. But a unlike read and write circuitry is used to sense and runrecords inputs to MFA.

3. IMPLEMENTATION

In order to accelerate the device routine along with the supply voltage, scaling of threshold voltage should also be done. This results in sub-threshold current to escalation exponentially, thereby increasing the static power indulgence. Fig.1 shows our planned rad-hard MFA (RH-MFA) circuit including two sub-circuits for SUM and output Carry (Co). Like to other magnetic logic circuits [11], this circuit is collected of three machineriesas well as a CMOS sense amplifier (SA) circuit, a CMOS logic tree (LT), and a nonvolatile MTJ component through a peripheral CMOS write circuit (for reconfiguration of the MTJs). As above-mentioned, among the stated CMOS components, the sequential SA circuit is susceptible to be artificial by radiation effects [8].

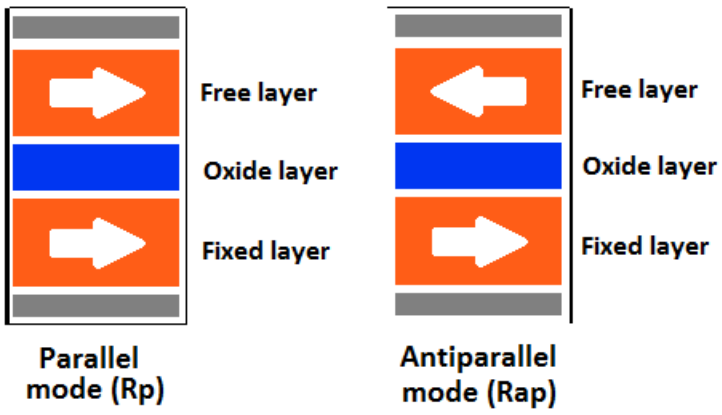


Fig.1. Metal Tunnel Junction Structure Modes

Magnetic Full Adder is recycled in supercomputers to build low power high-density arithmetic or logic unit. The MFA circuit in replacement mode offers roughly zeros leakage current. However, in the occurrence of radiation effects, these Magnetic Full Adder circuits cannot guarantee a fault-free operation [5]. The other CMOS components are combinational logic and there is no SEU apprehension for them [8]. It has been shown that, the current induced by particle assaults cannot change the formation of MTJs [13] and therefore, the MTJ cells are supposed as radiation lenient [14]. As cited earlier, the previous MFA circuits [6-7] agonize from radiation-induced easyfaults, due to their CMOS read module. To show this issue, we pretend the circuit planned recently in [7] (shown in Fig.3). All the simulations in this paper are achieved based on the simulation setup comprehensive in next section.

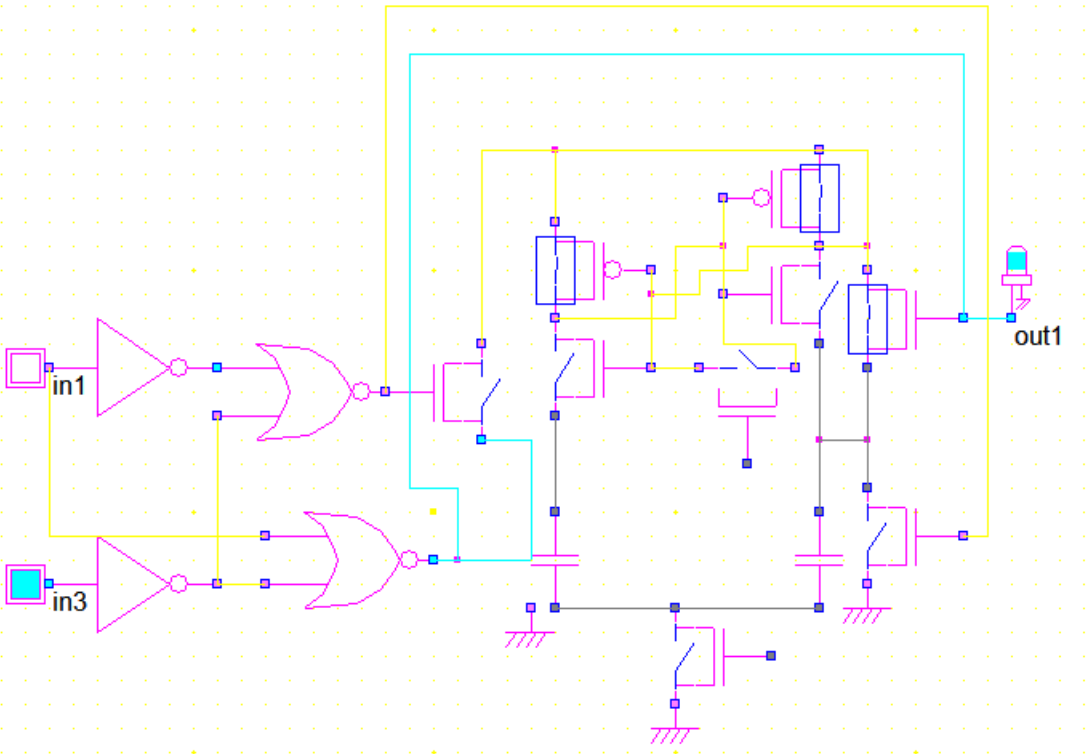


Fig.2. Unprotected magnetic latch: a complete circuit with the all CMOS and MTJ components

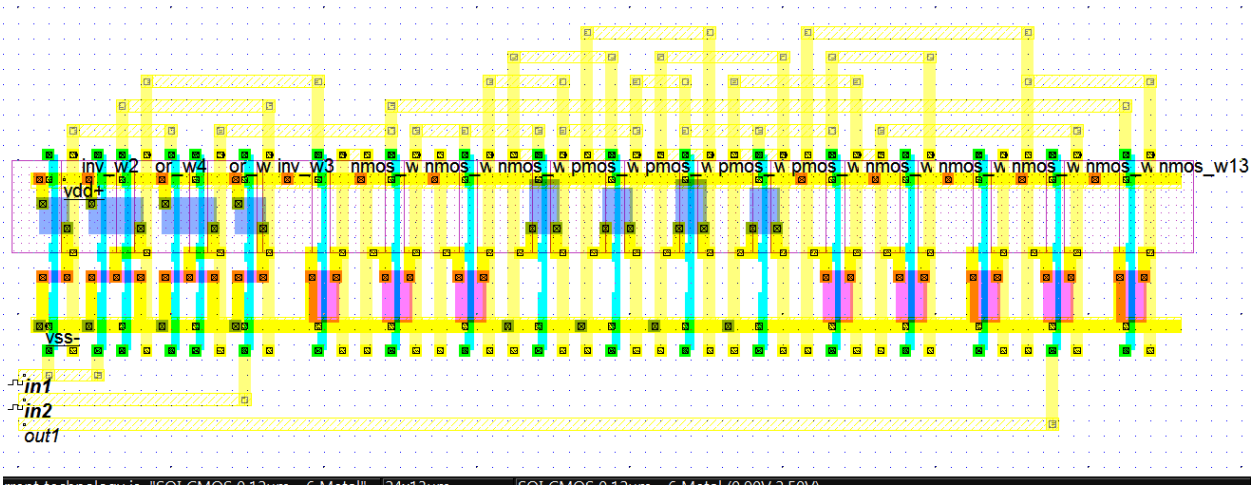


Fig. 3. Layout of UML

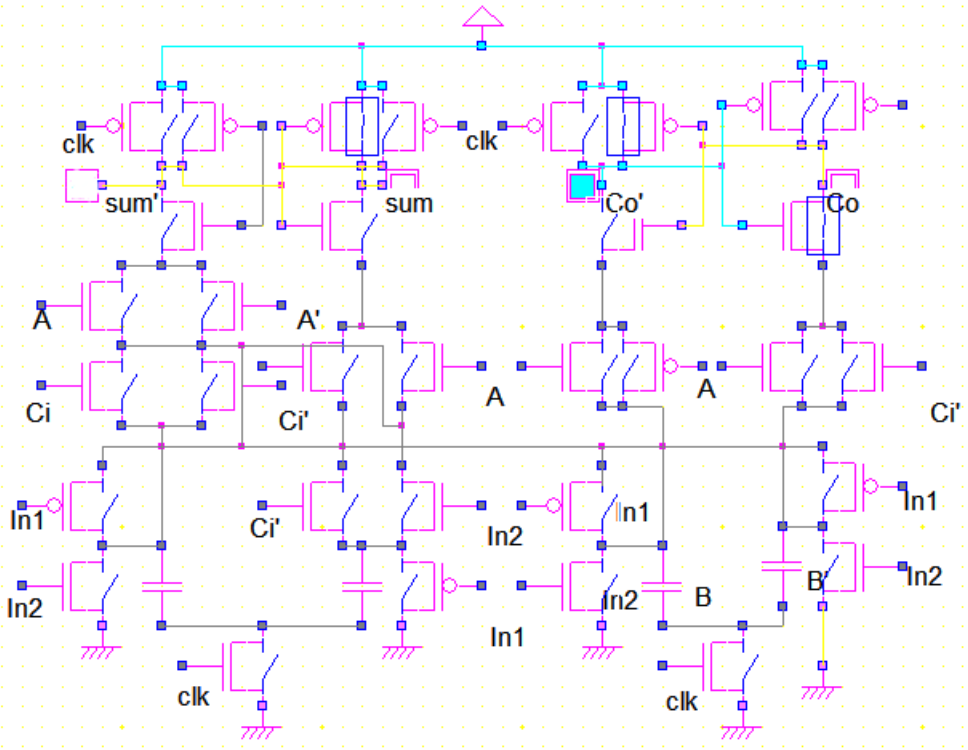


Fig.4. Proposed MFA circuit

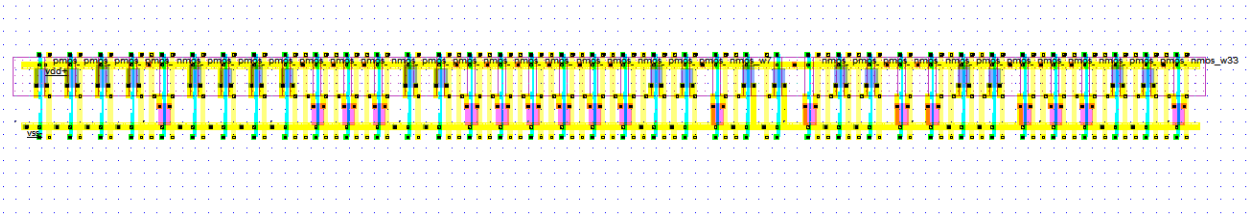


Fig.5. Proposed Layout of proposed MFA

As an alternative of the 6-transistor susceptive SA circuit active in Fig.3, we used a rad-hard SA circuit counting 12 transistors to gain SEU broad-mindedness. Also, instead of two reconfigurable MTJs per each sub-circuit (totally 4 MTJs for a 1-bit FA), we used one configurable MTJ (the so-called free MTJ) along with aimmovable one (the reference MTJ) for both the SUM and Co sub-circuits. In other words, we reduced the number of configurable MTJs from 4 to only 1 in a 1-bit full-adder circuit to obtain substantial energy effectiveness. The resistance of the configurable MTJ (the free MTJ) could be altered using the employed write circuit while the position MTJ always has a secure resistance.

4. A rad-hard and low power serial magnetic binary adder based on the proposed RH-MFA (SRH-MBA)

A sequential binary adder is a digital circuit that achieves binary addition in unremitting clock signals. As shown in Fig.7, this circuit employs a full-adder as well as a flip-flop [20]. The full-adder has two direct inputs and a carry-in bit that is the preceding calculated carry-out output. This circuit offers two output bits as the SUM and carry-out bits by addition inputs A and B (Fig.7), in a clock cycle. The conservative serial binary adder (shown in Fig.7) suffers from radiation-induced SEUs in the employed flip-flop. This circuit also has in height power consumption due to its data storage technique. We employed our proposed RH-MFA circuit to design a serial and rad-hard magnetic adder circuit (shown in Fig.8). Our planned serial magnetic binary adder uses only two reconfigurable MTJs to bar the resulted carry-out (Co) output as the next carry-in (Ci) input. MTJs are fundamentally robust against particle strikes. Also, our sense amplifier circuit is radiation hardened. Therefore, the planned serial magnetic binary adder is robust against SEUs. Also, due to the presence of MTJs in all the paths between the supply voltage and the ground, the matter of leakage current is not regarding. In this circuit, the saved value in each clock signal pulse as the carry-in (Ci), will be bring back in by the SA circuit at the next clock rise. In fact, when the clock signal is high, one of the reconfigurable MTJs employed (M1 or M2) is being sensed by the SA circuits and the other one (M2 of M1) is being reconfigured by the write circuit.

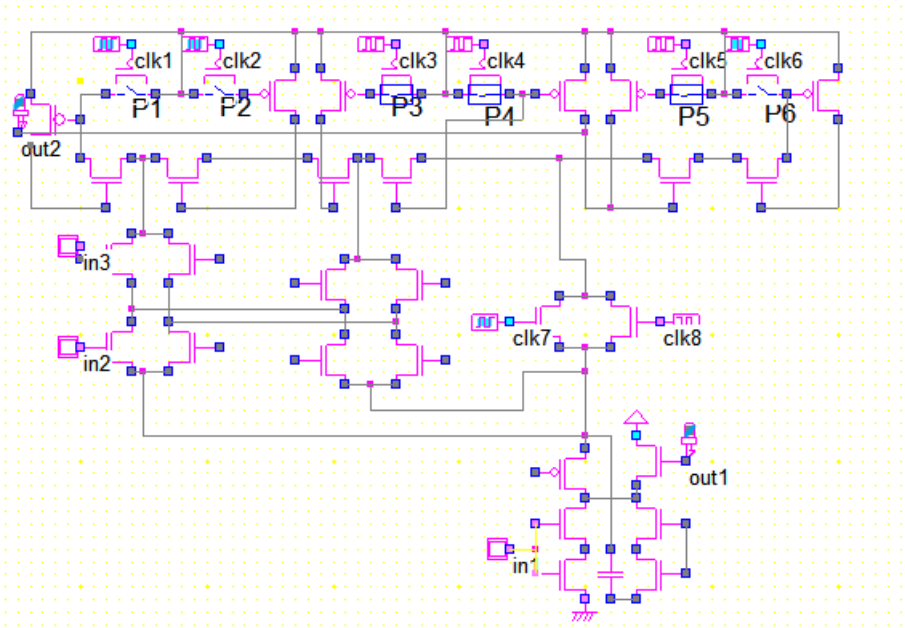


Fig.6. Proposed RH-MFA Circuit

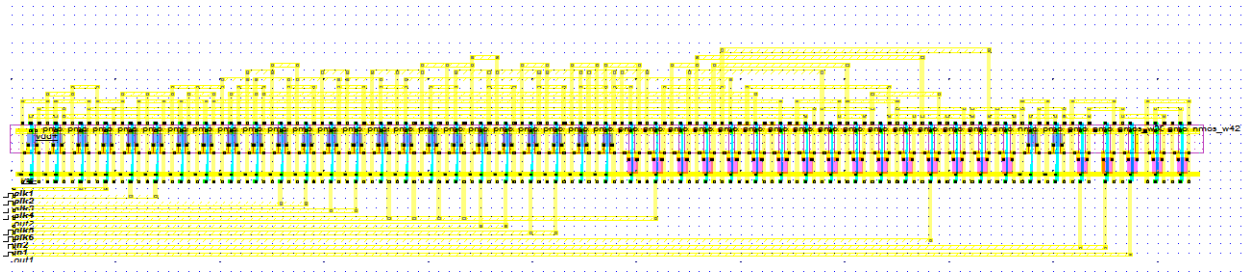


Fig.7. Layout of Proposed RH-MFA Circuit

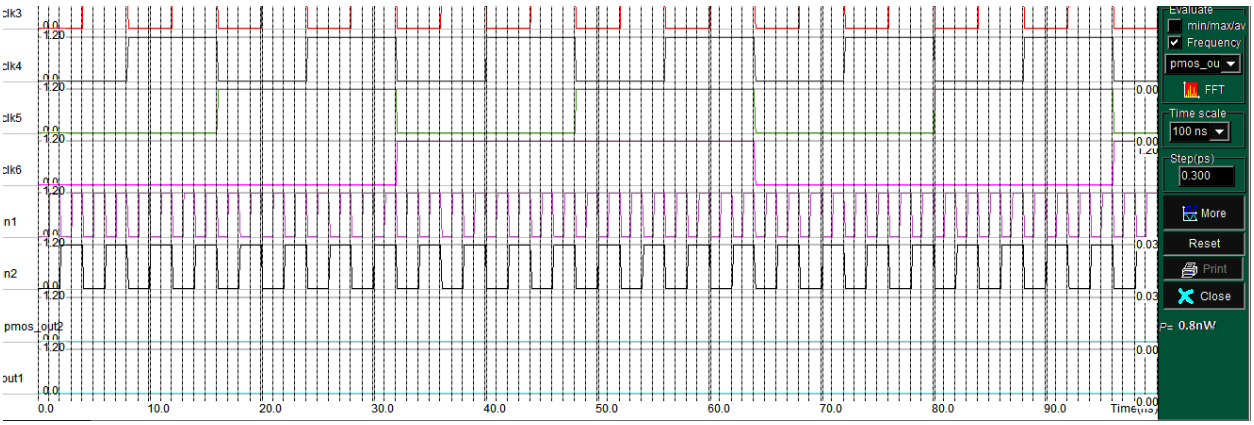


Fig.8 Output of Proposed RH-MFA Circuit

The fig. 8 shows the power dissipationsphysical appearance of the RH-MFA Fig. 7 and 8 shows the relationship between I_{ds} vs V_{ds} and I_{ds} vs V_{gs}respectively. Yielding to the DC characteristic it can be reasoned that the MOS is not biased from its standard operation and the subthreshold effect is also negligible so the low power process is required.

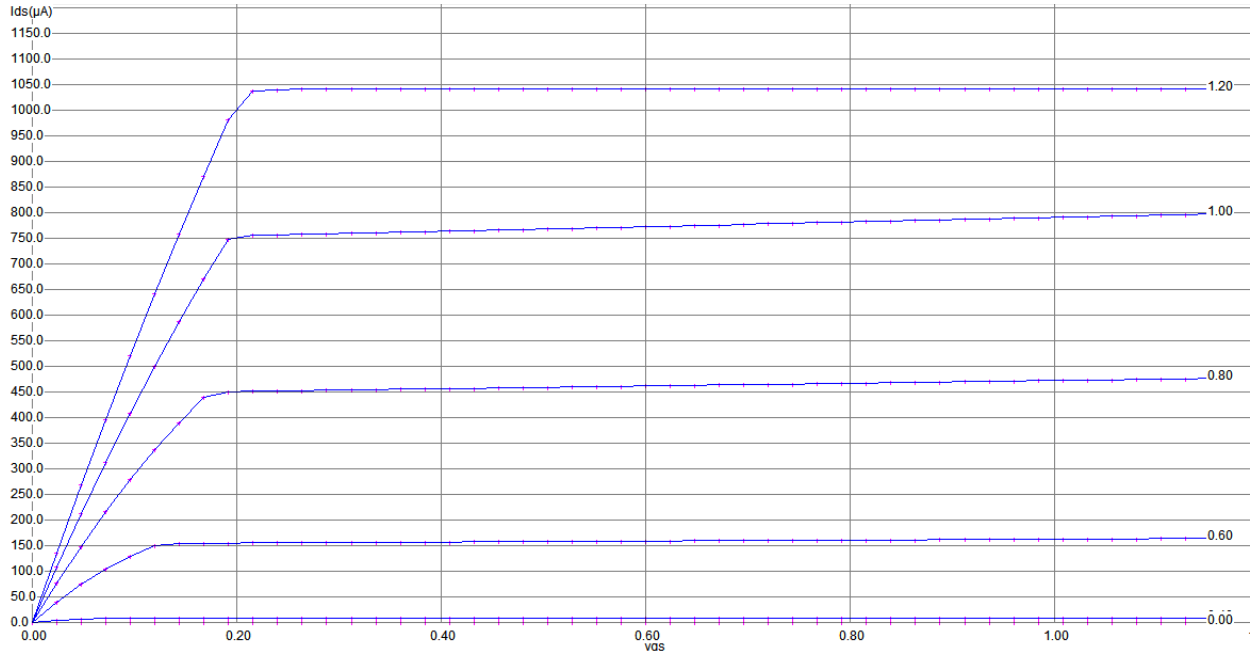


Fig.9. I_{ds} vs V_{ds} Curve

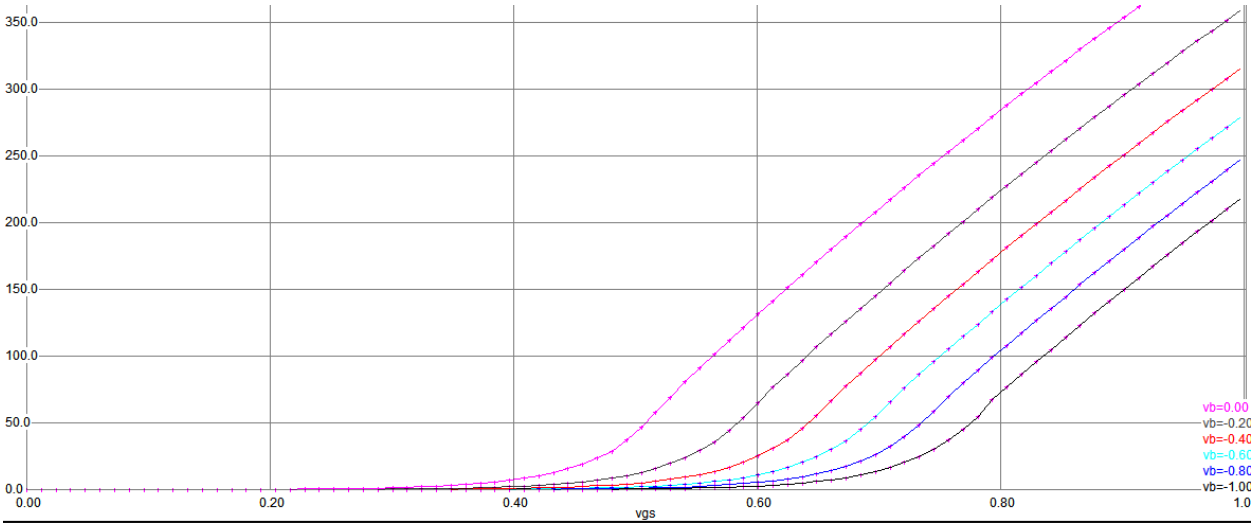


Fig.10.I_{gs} vs V_{gs} Plot

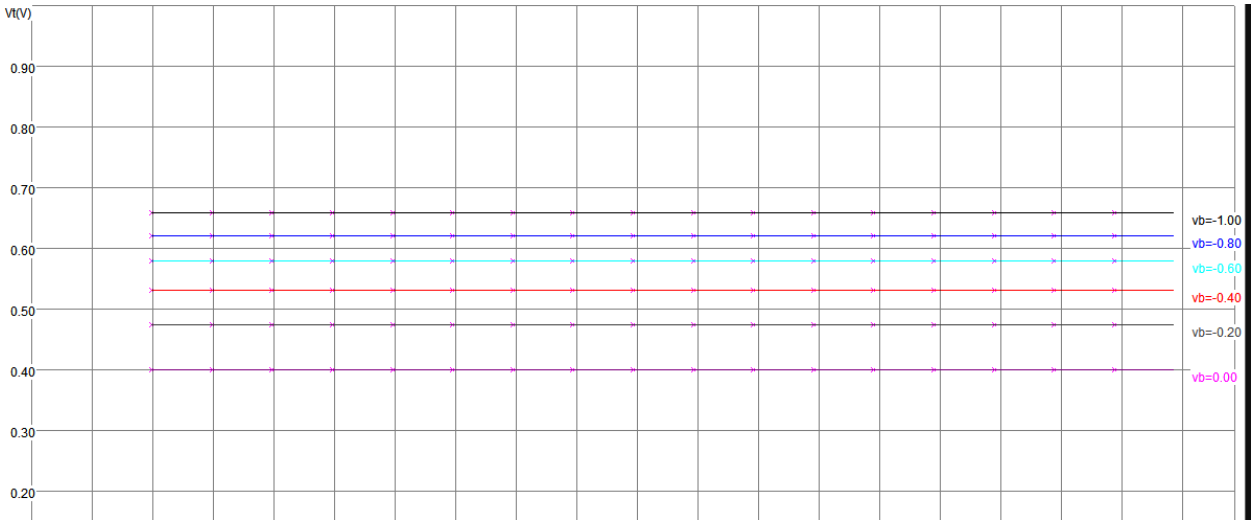
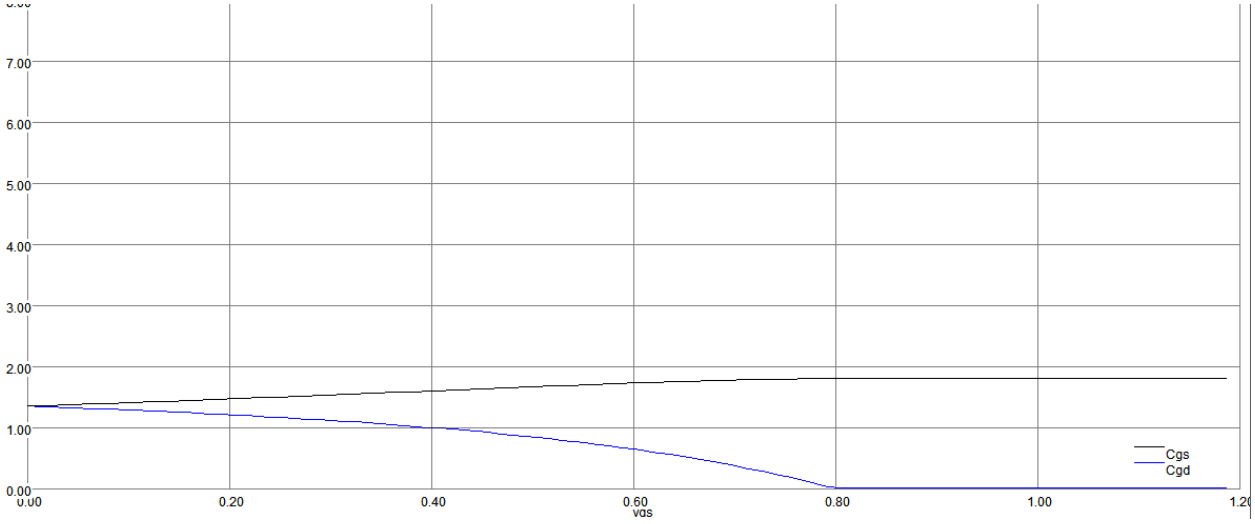


Fig.11. Threshold Analysis of Proposed Design

Fig.9 shows the relationship between channel length and the threshold voltage, after a certain limit is turned over for short channel the threshold roll off is well determined from the graph which will serve in the deciding the proper channel length of the device and it improves the, device operation. Capacitances are optimized in such a fashion that it will not affect the circuit performance. The final optimized simulation comparison is shown in figure – 11.



4. CONCLUSION

This tactic has an improvement of not impacting the dynamic power and furthermore in this method; less number of transistors is used when compared to the circuit in [4]. The planned RH-MFA circuit offers tolerance. The proposed

MFA circuit ingests less power when compared to the conventional method. To summarize, we can assert that the magnetic full-adder is effective since the power dissipation in adder circuit is fewer when compared with this technique. It can be used for the power gating and consistent architectures. In conclusion, we can entitlement that the energy consumption and also robustness against radiation effects in magnetic full-adders are enhanced over the previous work.

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