A Novel Approach to Implement MDC FFT Architecture For Low Power Applications

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Abstract- The 4G AND 5G wireless communications is dominated by MIMO-OFDM which defines as multi input and multi output orthogonal frequency division multiplexing. The multiple signals over multi antennas can be send or capable through this multi input and multi output and the radio channels can be divided into largely spaced sub channels through orthogonal frequency division multiplexing. The communication system uses this data without loss in reliability. In previous time division multiple access, code division multiple access are used with a combination of MIMO. But in spite of all these MIMO with OFDM is much famous. It is because of its high data rate, high message deliver capacity, high throughput. .At wires LAN and some standard networks at mobile communications it is famous for these reasons. If the data size increases then the memory size also increases rapidly in MDC based MIMO- OFDM, but in simplest manner data flow can be controlled by using multipath delay commutator. Simplicity is the main reason for implementing MIMO based OFDM and in order to increase reliability the bigger obstacles can be eliminated, it is possible by making the user data into a closely spaced narrow sub channels.

To implement fast Fourier transform (FFT) processors for multiple input multiple output-orthogonal frequency division multiplexing (MIMO-OFDM) systems with variable length, this Project presents a multipath delay commutator (MDC)-based architecture and memory scheduling. The fft/ifft processor can be implemented based MIMO-OFDM system based on the MDC architecture. RAM, FIFO, input buffer and output sorting buffer are implemented using this design and by using XILINX ISE 12.3i the functionality verification and the synthesis are carried out and the reduced delay values are showed.

Index Terms— Orthogonal frequency division multiplexing (OFDM), memory scheduling, fast Fourier transform (FFT), multiple-input and multiple-output (MIMO), pipeline based multipath delay commutator (MDC), WiMAX, output sorting,.

1. INTRODUCTION

Orthogonal frequency division multiplexing is the popular scheme which is generally used when we require a data to be encoded at multiple frequencies. At wideband digital communication this type of scheme is famous for. Whether it may be wired or wireless such as television, broadcasting of audio, internet accessing, wireless networks and is widely used in latest technology like 4G mobile communication. When we require to carry parallel streaming of data, OFDM uses the technique of digital multi carrier modulation, when each sub-carrier undergo convolution modulation like phase shift keying or quadrature amplitude modulation then a large spaced orthogonal sub-carrier signals are used. Because it uses slowly modulated narrow band signals instead of using one highly modulated wide band signal OFDM have the capability of channel equalization. FFT can be implemented using OFDM, then their will be no loss in efficiency. By using OFDM, narrow band co channel interfacing becomes very strong. For over time synchronization errors it is very less sensitive. In WLAN under the standard of 802.11a, digital radio systems standards like DAB/ERUKA 147, Terrestrial Digital TV systems (DVB-T)and Terrestrial Digital mobile systems(DVB-T), the OFDM signals of broad range are used.

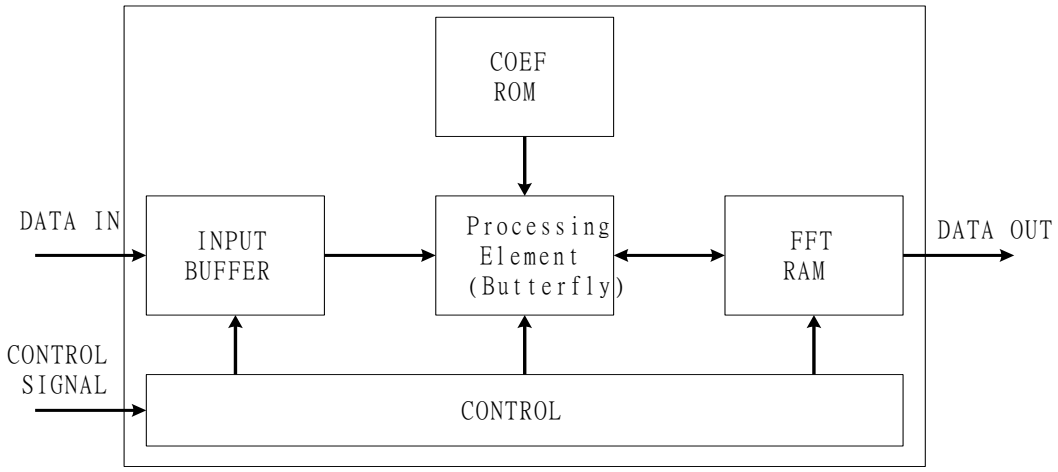
Discrete Fourier transform and also its inverse are computed using Fast Fourier transform. The signals from frequency domain to time domain and vice versa are converted by using this technique. In applications like image processing and signal processing the numeric algorithm are made as simple by using fft. FFT is used to overcome the drawback of fastness in previously existed DFT. In order to perform modulation and demodulation efficiently, Ofdm uses reverse fft and transmitter side and fft and the receiver side. In this OFDM fft frequency is cpu, intel Pentium at 1.26GHZ frequency and calculate 8 192 fft with in 576μs using FFTW, and in cpu called intel Pentium M AT 1.6 GHZ frequency and able to within 387 μs. In earlier generation cpu, a wide range of fft-ofdm based on operating frequency 3 Ghz and it is able to perform the 96 operations.

MIMO-OFDM defines multi input and multi output orthogonal frequency division multiplexing. 4G AND 5G wireless communications were dominated by multiplexing technique. Multiplexing like frequency division multiplexing and time division multiplexing. The orthogonal frequency division multiplexing communication over multi input and multi output, it defines the sending the number of possible signals communicate over multi antennas without loss in reliability . In this FFT-MIMO used to combination of time division multiple access, code division multiple access, but OFDM with MIMO technology is much famous compared to MIMO like high data rate, high throughput, high message deliver capacity. So that are have to take only familiar wires LAN and some standard networks at mobile communications. The MIMO-OFDM based MDC data size increases as well as increases memory size. But multipath delay commutator it follows the simplest technique. We controlled the data flow.

2. FFT PROCESSORS

Fast Fourier Transform and Inverse Fast Fourier Transform are the algorithms that compute the Discrete Fourier Transform (DFT) and Inverse Discrete Fourier Transform (IDFT). Fourier analysis converts the signal from

its original form time or space. Digital communication, telecommunication we were using application based FFT/IDFT. From the last decade, we were proposed so many FFT based algorithms using in communications.



Now a days, OFDM technique can be used in wireless communication: Wireless Local Area Network (WLAN), Wireless Metropolitan Area Network (WMAN), Digital Video Broadcasting (DVB), Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.) and Multi Band –OFDM Ultra Wide Band (MB–OFDM UWB). Moreover, we were proposed to be used in utilized in important wired applications like Power Line Communication (PLC) or Asymmetric Digital Subscriber Line (ADSL).

In communication system FFT/IFFT are used. In Transmitter side, IFFTs are used for modulating the signal. At the Receiver side, FFTs are used for demodulating the signal. From this we can say that FFT can be used at the transmitter side where as viterbi decoder algorithm as well as at the receiver side. FFT is the calculate the huge part at the receiver of OFDM systems. So that implementation of FFT and IFFT must be designed to achieve the required reduced area, increase speed as well as throughput. The modem OFDM transceivers lead in many cases, implementation of special–purpose hardware for the most critical parts of the transceiver. Designing of Very Large Scale Integrated (VLSI) circuit by using FFT/IFFT. The techniques are applied to IFFT can be applied to the FFT as well as. Moreover, the IFFT can be easily obtained by manipulating the output of a FFT processor. We were concentration on FFT based without loss of generality. By finding the inverse discrete Fourier transform which can be used to twiddle factor. Twiddle factor is a fast fourier transform algorithm of trigonometric constant coefficient that can be multiplied by the given data without using twiddle factor we cannot perform the FFT based algorithm. The difference between the discrete Fourier transform and fast Fourier transform is the twiddle factor division of 1/N.

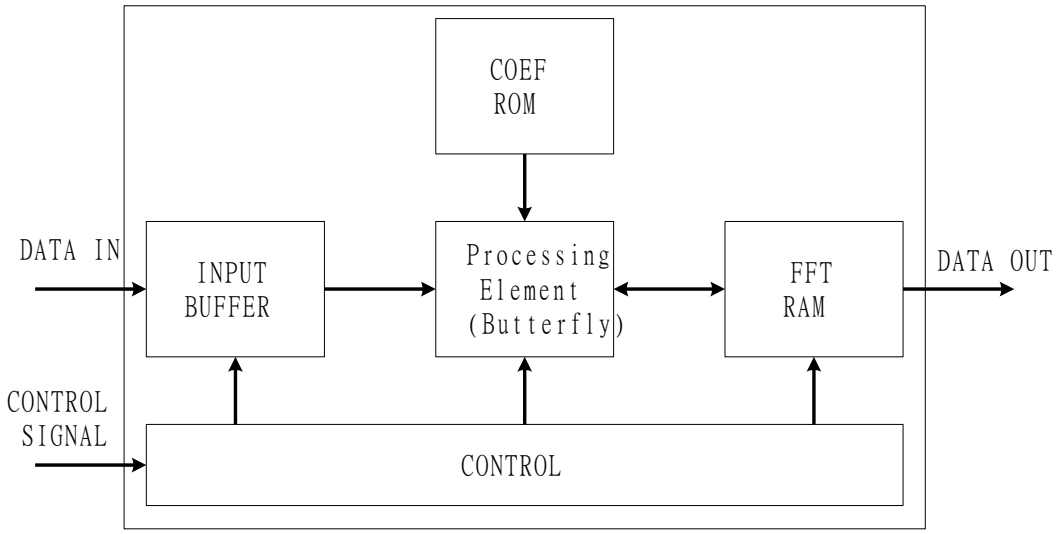


Fig1. INTERNAL ARCHITECTURE OF FFT/IFFT PROCESSORS

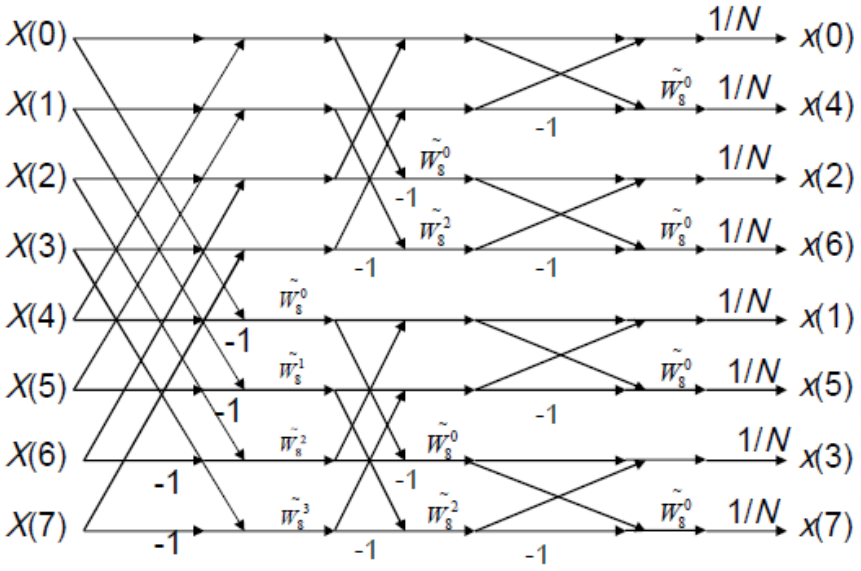


Fig.2 Inverse Fourier Transform

The evolution wireless technologies has been good contact with ships sailing in the English channel since 1894. Now a days new technologies are applicable to the new applications has been developed by hundreds and thousands of scientists and engineers through the world ever since. One of the most important communication is wireless communications can be regarded to development of wide range of applications from TV remote control to cellular phones and satellite-based TV systems. In this technology towards the people life style changes in every aspect. In last few decades growing exponentially the industrial combine radio communications with increasing rate, by the digital and RF (radio frequency) circuits design, fabrication and integration techniques and more computing power in chips. This technology is continue with an even crutial pace in the near future.

In recently radio and mobile communications advanced and development technologies have been partially helped to realize fast and reliable communicating anywhere and anytime. In mobile communications industry more experience in this wireless and wired Internet surfing and interactive multimedia messaging so on. In general how can we put high-rate data streams over radio links to satisfy our needs? we are proposed new technologies like wireless broadband techniques and wired band techniques are answer this question. So for example coming 3G (third generation) cellular networks cellular technologies provide with 2Mbps (bits per second) data service. But till now we were does not meet the data rate required by multimedia like digital communications, video conference and HDTV (high-definition television). In this techniques this performance improvement capacity increases are based on the channel state information. Channel state information plays the significant role for MIMO-OFDM systems. For this reason, it is part of my project to work on channel estimation of MIMO-OFDM systems.

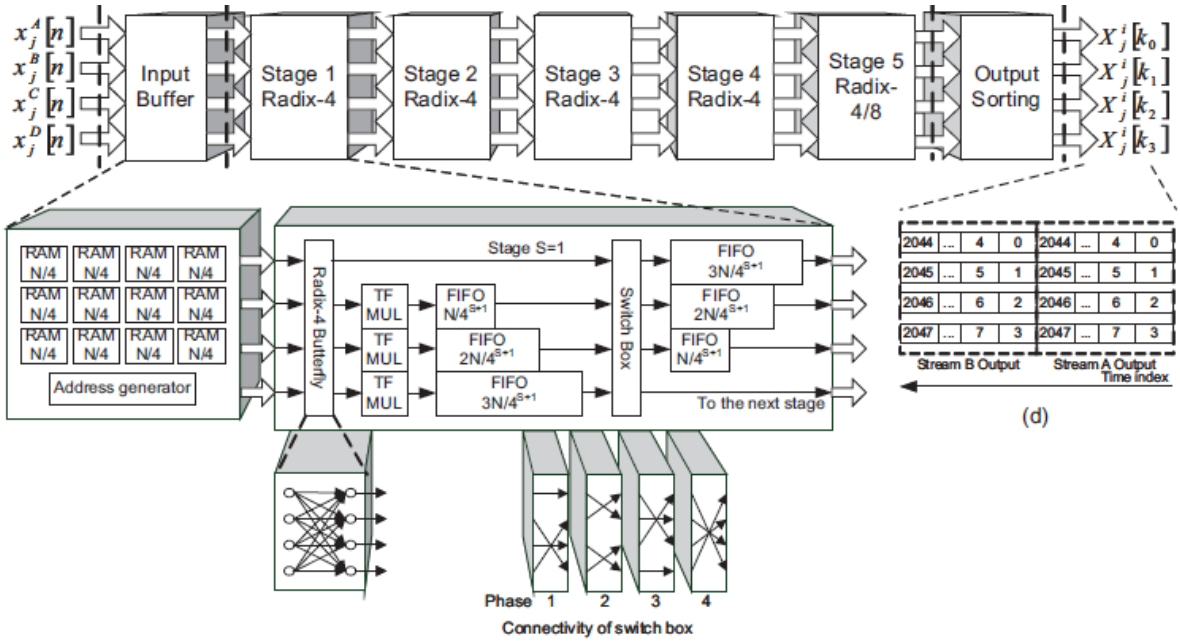


Fig 3: proposed MIMO fft/ifft processor

Multiple Input Multiple Output (MIMO) systems are devices that are used in wireless communication. These are circuits consisting of array of receivers and transmitters with FFT-OFDM devices it requires to possible

obtain high data. So far combination of MIMO and OFDM systems are provides reliability and efficient high data rate in wireless communications. IEEE 802.16 WIMAX (Worldwide Interoperability for Microwave Access) is a wireless communications standard, which can provide a data rates from 30 to 40 megabit/sec. 3GPP (3rd Generation Partnership Project) is the recent evaluation in IEEE 802.16 WiMAX. The 3rd Generation Projects evalued from neural network and AT&T Wireless networks. In this AT&T Wireless networks was operated an IS-136 (TDMA) wireless network in the United States in 1998. We were proposed memory scheduling techniques in the project RAM is changed due to DRAM to reduce the run time memory 12 memory blocks are sufficient instead of 16.Nortel Networks Wireless, which is developed till R&D center in Texas, Richardson the wireless division of Bell Northern Research developed a vision for "an all Internet Protocol (IP)" wireless network that is having the internal name "Cell Web". In the proposed design the ram is replaced by dynamic ram.

Reversible Gates are circuits in which numbers of inputs are equal to the number of outputs and there is a one to one correspondence between the vector of inputs and outputs. To getting the outputs by using Boolean algebraic equations at the side of inputs. So that the multiple outputs Boolean function X(a1; a2; :::; an) of Boolean variables are called Boolean reversible gates. With number of inputs are equal to the number of outputs and any pattern output has unique pre-image. In our project we are used reversible HNG gate can be working as reversible full adder.

If the input vector IV = A, B, Cin, 0

The output vector becomes OV = (P=A,

Q=Cin,

R=Sum,

S=Cout).

If we consider d = 0, then “S” is considered as CARRY “ R”is considered as SUM.

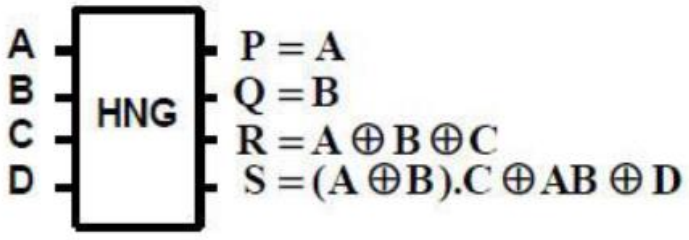


Fig 4: Block diagram of HNG gate:

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Comparing all the arithmetic operations we can implement multiplication easily by performing repeated addition, subtraction can be done by

negotiating one operand or division by performing repeated subtraction. The addition of two one bit binary numbers can be possible by using a Half Adder. For adding N-bit binary numbers and creating a logical circuit is possible by using multiple full adders. For every full adder the input given commonly is Cin, which is the Cout of the previous adder. This kind of addition operation is made by using a adder known as Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The half adder can be placed only in the first and only the first full adder. The block diagram of 4-bit Ripple Carry Adder is shown here below.

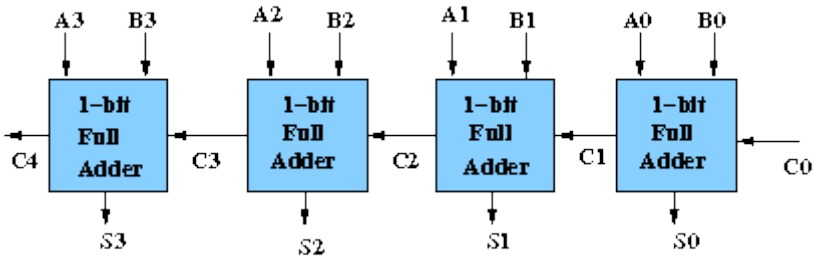


Fig 5 Ripple carry adder

3. FFT PROCESSOR METHODS

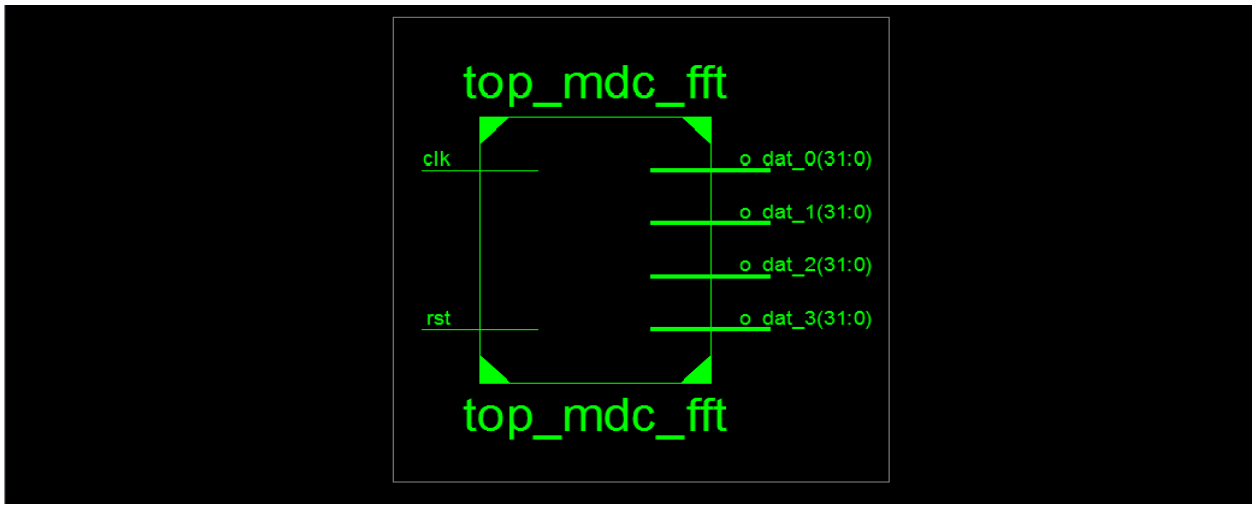
Discrete Fourier transform (DFT) is used to convert time to frequency and it also reduces the time complexity to O(N log 2N), where N denotes the size of FFT. It is computed by Fast Fourier Transform (FFT) which is an efficient algorithm. FFT is proposed by Tukey and Cooley. While implementation is considered those should be taken alternatively, the FFT/IFFT algorithm is chosen for the following parameters like flexibility, precision, execution speed and hardware complexity. However, for real time systems the main concern is execution speed. Several architectures are proposed over the last 3 decades like: single memory architecture, dual-memory architecture, cached memory architecture, array architecture, and pipelined architecture for the purpose of hardware implementation, different FFT processors are used mainly 2 types of architectures which are Memory based architecture and Pipeline based architecture. The pipeline architecture is used to overcome the disadvantages of former architecture where as the Memory based architecture cannot be alike. Pipelined architectures are distinguished non-stopping processing, real time and present smaller latency with low power consumption. These characteristics make them worthy for most application. Mainly, the pipeline FFT processors are classified in two design- architectures. They are Multiple-path delay Commutator (MDC) pipeline architecture and Single-path delay feedback (SDF) pipeline architecture.

The amount of multipliers are reduced using Single path delay feedback (SDF) but it makes difficulties in the control mechanism and also uses more memory resources whereas more area is saved using Multipath Delay Commutator,[5] and thus MDC is embrace as the hardware architecture. The feedback paths are converted into feed forward streams using switch boxes and also with memory are made feasible by using Multipath Delay Commutator (MDC). In this project, memory scheduling and Multipath Delay Commutator are used to implement fast Fourier

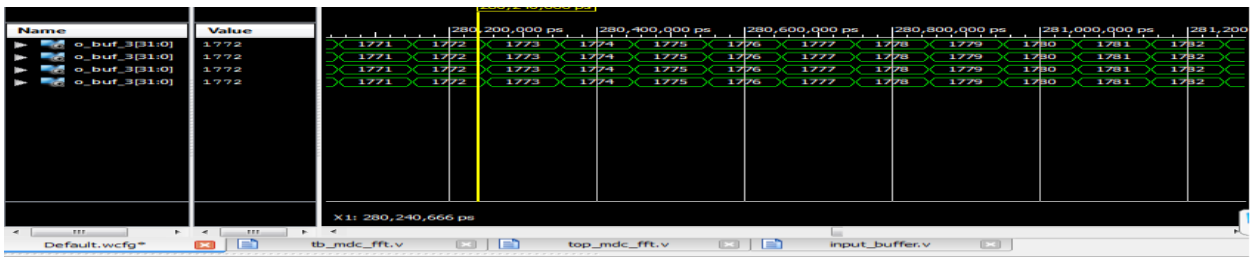
transform for multiple input multiple output orthogonal frequency division with variable length. According to the survey made in terms of memory utilization the delay feedback architecture is more advantageous or efficient than the delay commutator. To obtain the output signal of FFT computation we are used to twiddle factor to multiply with input signals whenever twiddle factor which will be increases the cost. Further a huge size of ROM is required to store the data. Thus for further improvement, ROM-less FFT/IFFT processor which eliminates ROM"s that store twiddle factor is presented. The complex multipliers are used to perform shift-and-add operations and are also used for this purpose. The processor uses a digital multiplier with 2 inputs and does not require any storage element like ROM, to store twiddle factor. The proposed architecture work we are also includes a reconfigurable complex constant multiplier to store twiddle factor instead of using ROM"s.

4. RESULTS

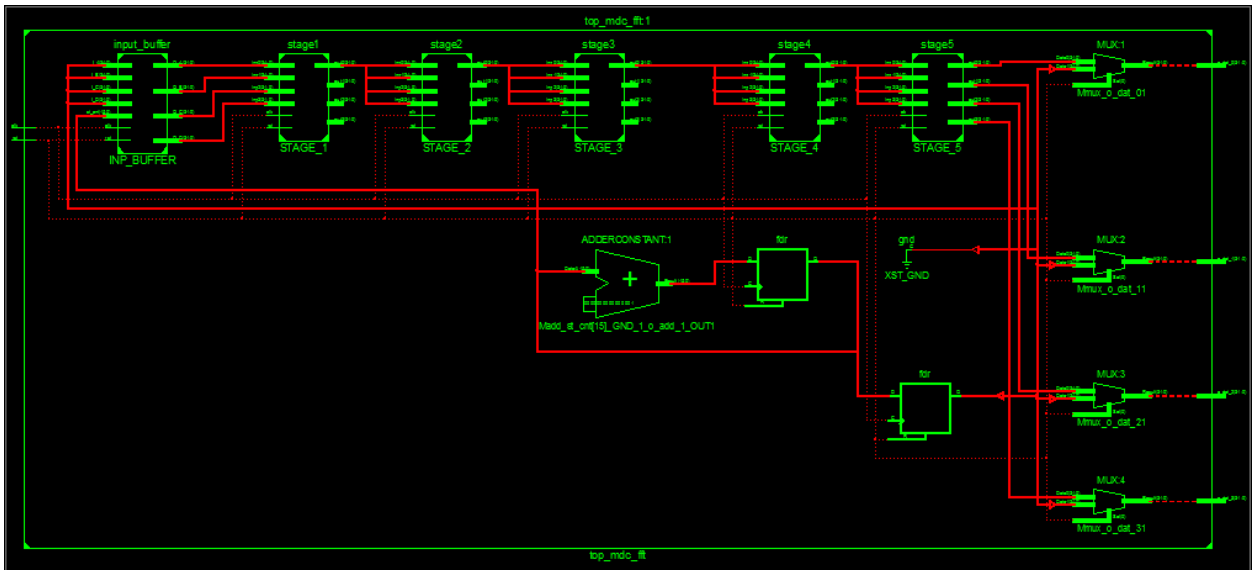
Rtl Schematic:



5. SIMULATION RESULTS:



RTL Internal Schematic:



DESIGN SUMMARY:

DEVICE USED: XC6VSX475TL-1LFF1156

PROPOSED:

NO OF LUT'S = 7850.

EXISTING:

NO OF LUT'S = 7906.

PROPOSED RESULTS:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1798	595200	0%
Number of Slice LUTs	7850	297600	2%
Number of fully used LUT-FF pairs	1308	8340	15%
Number of bonded IOBs	130	600	21%
Number of Block RAM/FIFO	6	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	228	2016	11%

EXISTING RESULTS:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1930	595200	0%
Number of Slice LUTs	7906	297600	2%
Number of fully used LUT-FF pairs	1398	8438	16%
Number of bonded IOBs	130	600	21%
Number of Block RAM/FIFO	6	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	228	2016	11%

6. CONCLUSION

In this paper, we proposed a radix-*r* based MDC MIMO FFT/IFFT processor for processing *Ns* streams of parallel inputs, where *r* = *Ns* for achieving a 100% utilization rate. The proposed approach is suitable for MIMO-OFDM baseband processor such as WiMAX or LTE applications. Where *Ns* = 4 and *N* can be configured as 2048, 512, 256, and 128. Moreover, we proposed an efficient memory scheduling to fully utilize memory. In this process we are considering decreases chip area because it dominates the chip area in an FFT processor by memory requirement. The proposed design is based on an MDC architecture, which is generally not preferred, due to its low utilization rate in memory and computational elements such as multipliers and adders.

However, by using this proposed memory scheduling of MDC architecture I was concluded which is suitable for FFT/IFFT processors in MIMO-OFDM systems, because the butterflies and multipliers and adders are capable of achieving a 100% utilization rate. Then the characteristics of simple control by MDC are maintained in the proposed design.

In this process whenever the memory reduction usage it is effect on power saving, which is important for mobile devices. For applications applying large number *Ns* of data streams such as gigabit passive optical network, *Ns* can be as high as 64. In this case, the proposed radix-*Ns* MDC scheme and memory scheduling may also be applied to achieve a 100% utilization rate with simple control mechanism. Therefore, we conclude that the proposed designs found a good balance among complexity, energy consumption, and chip area, for the MIMO-OFDM systems

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