Design Based on Digital octarate Clock and Data Recovery (CDR) Circuit

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Abstract- Digital octarate clock and data recovery (CDR) circuit are generally, plays a vital role for wired serial communication link in multi-module channel based ona system on (SoC). It uses a high range of clock frequency in terms of GHz that operate at higher clock rates in order to handle the higher data rates, which results in higher dynamic power consumption. In order to overcome, high power consumption dynamic is reducing, the proposed architecture circuit design works at the frequency of one-eighth of the received data clock rate and gift other words a novel digital octarate clock and data recovery (is a process of salvaging (retrieving) inaccessible, lost, corrupted, damaged or formatted data from) CDR circuit has an optimal solution. It is compatible with real time clock by introducing a RSG. The proposed architecture CDR circuit consists of 16 phase generators, delay line controller, an Early octarate late type phase detector and controlled digitally delay line. The purpose of FSM based digitally controller delay line is to provide a sufficient delay in digitally controlled delay line. It is observed from that group of information that the existing controller delay line is realized by using the combinational of multiple path flows delay line circuit which is not providing sufficient delay. Hence, in this project proposal we introduced a Finite State Machine (FSM) based digitally controller delay line is to provide a sufficient or required delay in input data and controls the length of the delay. In order to reduce Area, a Digital octarate CDR circuit has been realized using Xilinx ISE 14.7(extension of this work).

Keywords: Octa-rate clock and data digital recovery circuit (CDR); System-on-chip(SOC); Early Octarate late type phase detector/comparator; FSM.

1. INTRODUCTION

In a generic CDR circuit, shown in fig. 1, the phase detector compares the phase of incoming signal data to the phase of the clock frequency generated by the voltage-controlled-oscillator (VCO), Applying the XOR gate's output to a low-pass filter results in an analog voltage i.e.; proportional to the difference of the phase between the two voltage signals inputs that produce an error. This error is applied to a charge pump and its output is given to the low pass filter so it has to generate the oscillator control voltage. Depending on the control voltage the VCO generates clock signal. The clock signal drives to make a decision circuit, thereby retiming the clock data and gradually reducing its jitter. In generic CDR circuit dynamic power consumption is high. The best way to approach of reducing the dynamic power consumption is by decreasing the switching frequency of the internally generated [2] clock signal without negatively affecting the data rate.

2. PROPOSED ARCHITECHTURE

To reduce dynamic consumption power, the promising idea is to use various phases of a clock, running at a frequency less than the data rate in the operation of the PD rather than using a single high-frequency clock signal. Mohammed H. Alser et al. in [3] designed

quarter-rate CDR circuit which consists of four major blocks namely 8-phases generator, delay lines controller, early quarter-rate late type phase detector and digitally controlled line delay. The purpose of digitally controlled line delay is to provide delay under the digital control. In [3] digitally controlled line delay is designed using combinational circuits. It is experimentally found from simulation results that sufficient delay is not achieved by using combinational circuits in digitally controlled line delay of quarter rate CDR circuit. One of the main contributions in this paper is to overcome above problem by replacing the combinational circuit with a sequential circuit in FSM based digitally controlled line delay is to provide sufficient delay. On other hand the reduction of dynamic power consumption is an important aspect. So, quarter-rate CDR circuit designed which will be operate using 8 phases of a clock running at a clock or signal frequency equal to 1/4thof the data rate, as mentioned in [3], but we did not experience the one-fourth redemption in total dynamic power consumption. In this paper, we design a soc digital octarate clock and data regenerator circuit are to provide the necessary delay and power consumption. In this paper comparison of dynamic power consumption between quarter-rate and octarate CDR circuit is reported.

The circuit quarter-rate CDR has been designed by replacing the combinational circuit with a sequential circuit in FSM based digitally controlled line delay is to provide sufficient delay. With extension to Quarter- rate CDR circuit, we propose novel digital Octa-rate CDR circuit to overcome the existing problem. The proposed model mainly involves has four blocks as shown in fig. 2, namely 16-phases generator, early late PD, digitally controlled linedelay and linedelay controller.

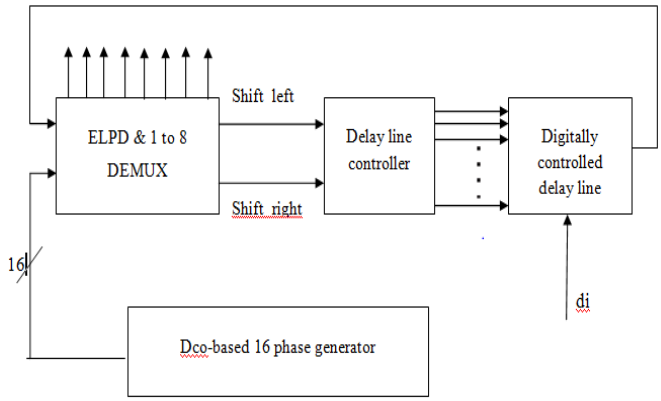

Diagram: Octa rate CDR circuit

RESULTS

The quarter-rate CDR circuit is designed, which will operate using eight phases of a clock, running at a frequency equal to one-fourth the data rate. But one-fourth redemption in dynamic power consumption was not experienced.

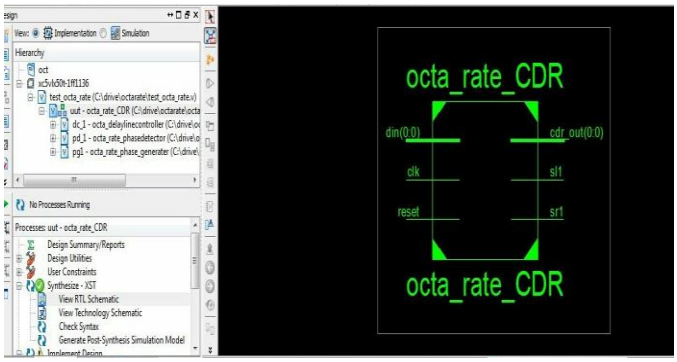

Figure1: RTL schematic top module

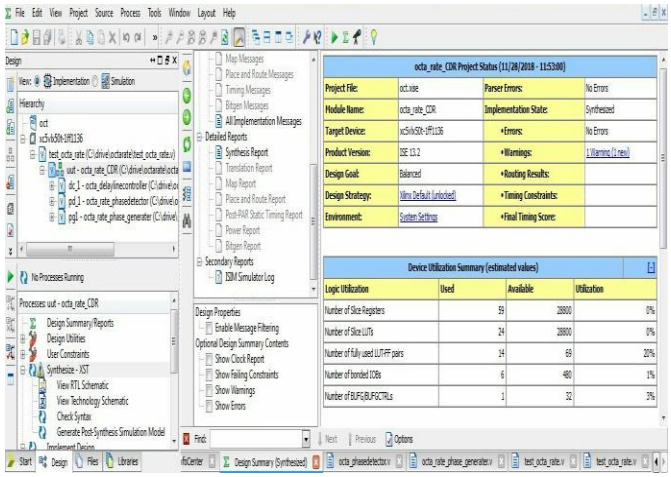

Figure2: design block diagram

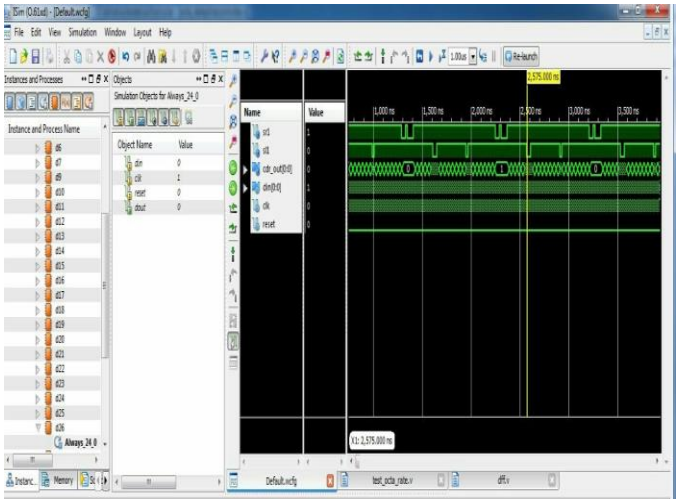

Figure3: Simulation design.

SUMMARY AND CONCLUSION:

CDR circuit is designed to provide a sufficient delay with reduced dynamic power consumption. The design of PD and line controller delay is heart of this work. To obtain sufficient delay FSM based sequential circuit is implemented in delay line controller instead of combinational circuits. The proposed architecture model can be easily classified as for different FPGA families. By comparing Octarate CDR circuit with quarter-rate CDR circuit, it is observed that 27% of dynamic power consumption is reduced. It can be therefore concluded that our novel digital octa-rate CDR circuit exhibits better performance over other realizations.

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