Innovative Design of 8-Bit Comparator using GDI Technique with efficient VLSI Design Constraints

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Abstract- Comparator has three main outputs where it can compare the weight of two words and generates three functions. GDI has the advantage of low power consumption because the total number of logic devices needed will be less and it can also operate with high speed due to affective realization of logic using minimal hardware. GDI has the disadvantage of effecting the noise margins for logic '0' and logic '1'. The problem can be solved by introducing buffers in appropriate output node where voltage levels tend to go into the unknown region. The choice of designing which two outputs and then designing the third output is always the key factor for optimized designs. We have designed the hardware for greater and lesser condition and then designed for equal condition.

I. INTRODUCTION

Optimization is the key in designing of VLSI circuits as it leads to hardware which can meet the client constraints. Comparator compares group of twin words and output the result of A=B, A>B and A<B. Comparator Designed by using adder which is a arithmetic operation with 30 Number of transistors used Xor, And, Not, Nor and Mux 2 to 1 which is a mix of Mux based design as well as arithmetic[1].Power efficient method by using GDI has proposed in by supplying less voltage where the required logic elements are more[2].High speed with CMOS Comparator

proposed in by minimizing the number of levels in hardware but with more occupancy of chip area [3].Mux based design of Comparator given in by using the least possible size of multiplexer which does realize the logic by taking minimal hardware [4]. Low Area and Low Power Design of Comparator proposed in by designing the logic block and logic carrying block [5].Hybrid Design of Comparator given in by using pass transistor logic and pseudo logic [6]. Various Logic Styles design of Comparator proposed in and their performances are analyzed[7]. Gate Diffusion input technique which is a prime factor for power consumption due to efficient design of logic using less hardware[8].

II. GDI(GATE DIFFUSION INPUT TECHNIQUE)

GDI cell consists of four terminals in which we have drain, source, gate and bulk terminal. Any GDI cell consists of two transistors , one PMOSFET and one NMOSFET. As opposed to CMOS, inputs can be applied to the gate as well as to the source but the logic levels obtained at the drain depends on which MOSFET is driving which source that is if PMOSFET drives logic'0' then there will be a loss of theshold voltage V_{tp} and the resultant voltage will be the increment of 'V_{SS}' volts and if NMOSFET drives logic'1' then there will be a loss of theshold voltage V_{tn} and the resultant voltage will be the decrement of 'V_{DD}' volts. If this degraded logic levels drive the transistors then transistors will not be turn ON or OFF completely resulting in the very bad logic levels and this may even lead to malfunctioning of the circuit. The remedy is to place non-inverting buffers in the sub-circuits where the logic levels does not fall in the logic regions of '0' and '1'.

GDI technique does require less number of transistors, with which we normally expect power and delay to be affective but degraded logic levels will not turn off the transistors completely will lead to more power consumption and since the applied voltages can be less this may lead to more delay. The overall performance of GDI depends on the number of transistors with logic level degradation

GDI in comparison with CMOS has less area, delay and power, even though GDI requires more power and more delay that is only with respect to the circuit operation and not with the circuit required to realize the logic. CMOS generally requires many number of logic devices as compared to GDI which by default leads to more power, less speed and more area.

III. COMPARATOR

Proposed equations for 8-bit comparator are mentioned below.

X0=a7b7'……1

Y0=a7'b7……2

X2=x0+y0'a6b6'……3

Y2=y0+x0'a6'b6……4

X4=x2+y2'a5b5'……5

Y4=y2+x2’a5’b5……6

X6=x4+y4’a4b4’……7

Y6=y4+x4’a4’b4……8

X8=x6+y6’a3b3’……9

Y8=y6+x6’a3’b3……...10

X10=x8+y8’a2b2’…….11

Y10=y8+x8’a2’b2…….12

X12=x10+y10’a1b1’….13

Y12=y10+x10’a1’b1….14

X14=x12+y12’a0b0’….15

Y14=y12+x12’a0’b0….16

Above equations from the X denotes logical expressions for A>B from 1-bit to 8-bit that is X0 indicates 1-bit comparator logical expression for A>B and X14 indicates 8-bit logical expression for A>B . To design for 8-bit we require 8 number of levels and in similar way N number of levels needed to design N- bit comparator. Above equations from the Y denotes logical expressions for A<B from 1-bit to 8-bit that is Y0 indicates 1-bit comparator logical expression for A<B and Y14 indicates 8-bit logical expression for A<B . To design for 8-bit we require 8 number of levels and in similar way N number of levels needed to design N- bit comparator. All the equations from 3 to 16 just require logic forward cell except with change of inputs and interchanged.

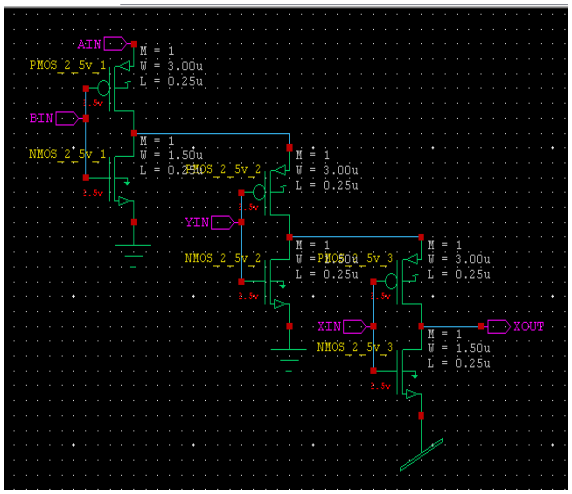

Figure1. Circuit of logic forward cell.

Fig.1 indicates there are 6 number of transistors in which XIN is the previous output of A>B and YIN is the previous output of A<B. If XIN is equal to 1 it indicates that A>B and the output should be '1' and the NMOSFET of third level will be on then XOUT will be '1'. If YIN is equal to '1' it indicates that A<B and the output should be '0' and the NMOSFET of second level will be on and the third level of PMOSFET will be on then XOUT will be '0'. If YIN is equal to '0' and XIN is equal to '0' it indicates that A=B and the output should be '0' and the first level will produce output of '0' and through PMOSFET of second level and PMOSFET of third level XOUT will be '0'.

Fig.1 can be used to generate logic block required for A<B, except operands of A and B will needed to be interchanged as well as for XIN and YIN. The same block can be forwarded to the next stage for calculation for A>B and A<B and this procedure goes on till the least significant bit

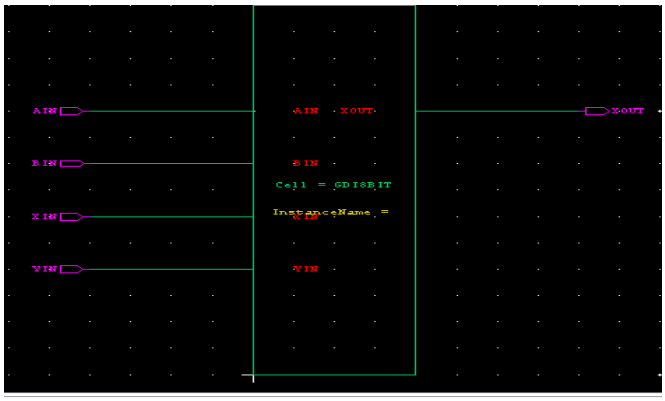

Figure2. Symbol of logic forward cell.

Fig.2 indicates that there are four inputs out of which two are the operands of A and B and remaining are previous status of A>B and A<B. The same symbol can be reused to build the entire circuit.

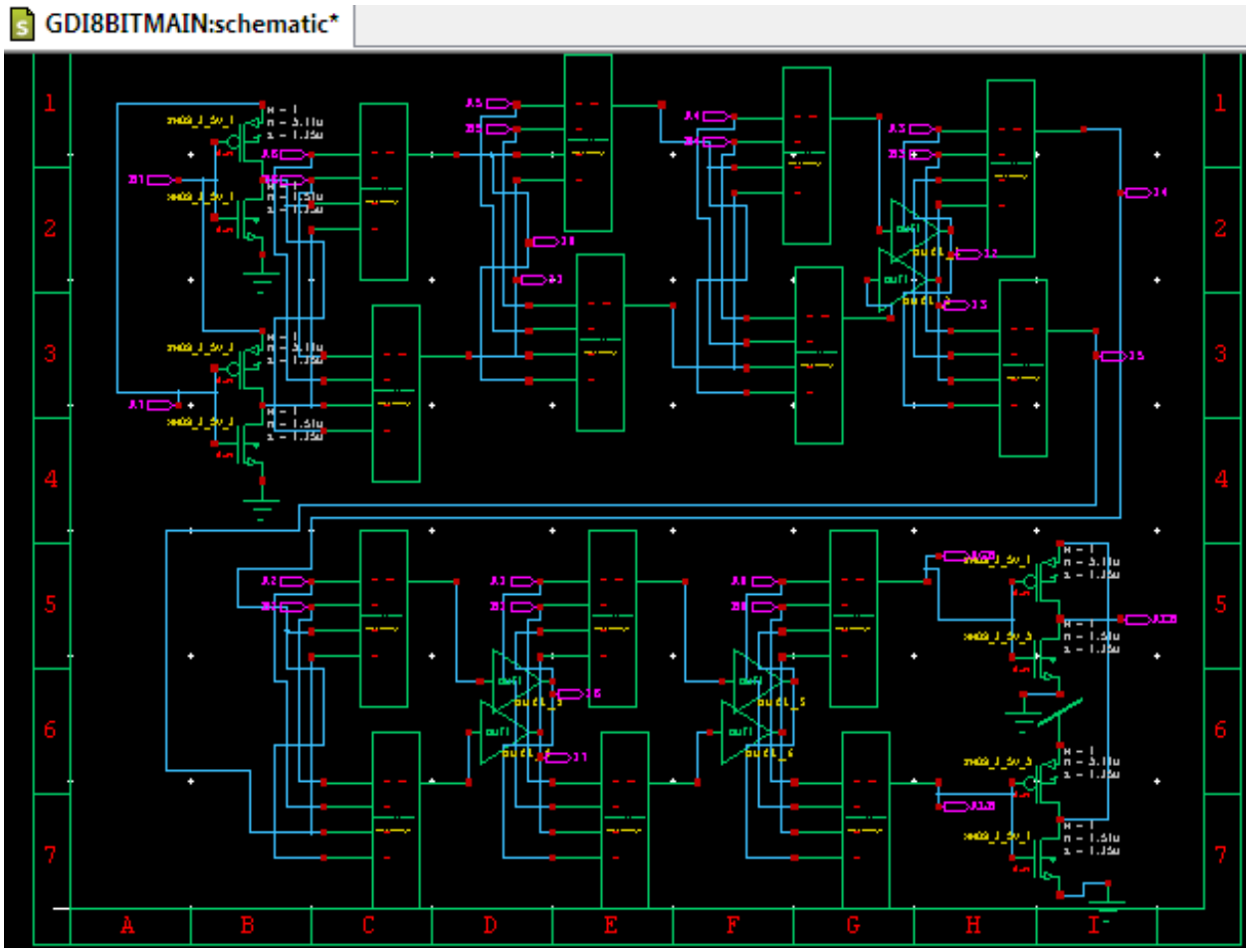

Figure3. Circuit of 8-bit Comparator.

Fig.3 indicates that Comparator required 14 number of logic forward cells and 6 non-inverting buffers and four GDI cells.Buffers were used after the 4-bit comparator because our detailed bit by bit simulation have not shown any output level reaching to undefined region, but for 5-bit comparator output levels have reached to the undefined levels where we cannot differentiate between logic '0' and logic'1' levels and there we have placed buffers to strengthen the signal to generate proper output levels at both the A>B and A<B logic forward cells. Similarly for 6-bit and 7-bit comparator buffers were needed to generate logic levels in the defined region of logic'0' and logic'1'. Nor gate was used to produce the output of A=B. Comparator requires 11 number of levels to generate the output of AGB, ALB and 12 number of levels to generate AEB.

IV.PERFORMANCE ANALYSIS

Table 1. Comparison of transistors in Two Designs

S.No	Transistor count	Design in reference 1	Proposed design
1	2 bit	30	20

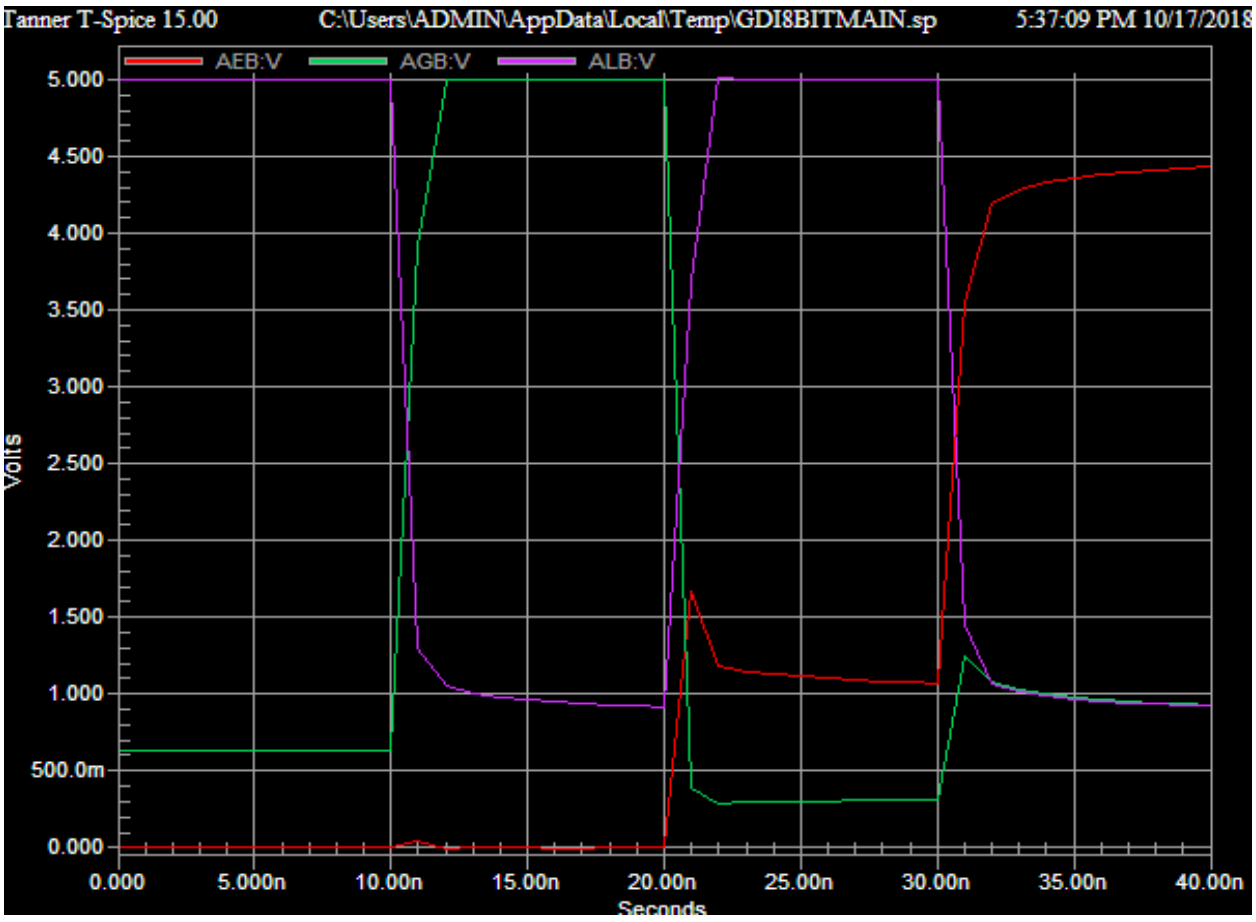

Figure 4. Waveform of 8-bit Comparator.

Above waveform has four pulses each of duration 10 ns and the first pulse and third pulse shows that ALB is true, second pulse shows that AGB is true and fourth pulse shows that AEB is true. AEB has the worst level of logic degradation 1.1 V for logic '0' and AGB has the logic level degradation of 0.9V and ALB has logic level degradation of 0.9V.

V.CONCLUSION

Designing a circuit in GDI of less number of bits has minimum modifications in the designed circuit. Design of comparator beyond 4 bit has shown us that logic levels are completely settling in the undefined region, so for that purpose we have used buffers which can strengthen the signal in the intermediate outputs and thus finally for designing 8 bits we need buffers, even though they consume more Area, Power, Delay and Cost because the circuit functionality is far more important and it is the first and foremost constraint. Proposed design needs 33% less number of transistors then the existing GDI based comparator.

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