SPEED CONTROL OF PMSM USING FPGA

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ABSTRACT: The Space Vector Pulse Width Modulation (SVPWM) is possibly the best among all the PWM techniques for three-phase voltage-source inverters (VSI) in drive applications. The RTL design of SVPWM can be incorporated with a FPGA to provide a simple and effective solution for high-performance ac drives. The SVPWM is being implemented for the speed control of permanent synchronous machine (PMSM) using Field Oriented Control (FOC) technique. The FPGA platform supports the run-time reconfiguration of control functions and algorithms directly in hardware and meets real-time performance criteria in terms of timings for PWM generation as well as reconfiguration. The range of switching frequency is 4 to 16 kHz. This paper presents a simple realization of 5-segment discontinuous SVPWM with a different approach based on FPGA, in which the judging of sectors and the calculation of the firing time to generate the SVPWM waveform is simple, and also the switching losses are low. The proposed discontinuous SVPWM has been designed using Xilinx ISE software for driving a three phase inverter system with PMSM machine as load with low current harmonic distortions.

Keywords: space vector, pulse width modulation, discontinuous SVPWM, FPGA, FOC, PMSM

I. INTRODUCTION

Today, Digital Signal Processor (DSP) and microcontroller have been widely used for PMSM control system. But global competition has brought immense pressure to the product development of PMSM control system. For the PMSM control system design, the DSP/MCU based hardware design is very time-consuming. So if the hardware of PMSM control system can be re-configurable, it will help to reduce the new PMSM control system development time and cost. FPGA, as a new re-configurable hardware platform, has been used for AC motor control system [2-5], [6-7]. VHDL is usually used for developing the FPGA based motor control system [3-9].

Employing Field Programmable Gate Array (FPGA) to realize SVPWM strategies provides advantages such as fast computation response, cost effective, simpler hardware and software design, and higher switching frequency and reconfigurable. FPGA performs the entire procedures with concurrent operation (parallel processing by means of hardware mode and not occupying) by using its reconfigurable hardware. For its powerful computation ability and flexibility, an FPGA is considered as an appropriate solution to boost system performance of a digital controller including an SVPWM algorithm [9-10].

The Space Vector Pulse Width Modulation (SVPWM) method is an advanced PWM method and it is possibly the best among all the PWM techniques for variable speed drive applications. In recent years, this method gradually obtains widespread applications in the power electronics and the electrical motor drives, because of its superior performance characteristics. Compared to the Sinusoidal Pulse Width Modulation (SPWM), SVPWM is more suitable for digital implementation and can use better DC voltage utilization ratio. Moreover, it can obtain a better voltage total harmonic distortion factor [10-11].

However, the conventional SVPWM suffers from the drawbacks like computational burden, inferior performance at high modulation indices and high switching losses of the inverter. Hence to reduce the switching losses and to improve the performance in high modulation region, several discontinuous SVPWM methods have been proposed. The comparison of PL, TJ junction IGBT, and weighted THD of the different modulation schemes are shown in Table 1 [12]. From the comparison, although the discontinuous SVPWM (or bus clamping SVPWM) gives a slightly higher of weighted THD compared with conventional SVPWM method, the result in lowest switching losses and lowest junction temperature of IGBT compared with the SPWM and conventional SVPWM. The switching loss of the discontinuous SVPWM is consistently lower than those of SPWM and SVPWM as there are fewer switching instants and that the dead-time effect is smaller since there is no switching during the DC clamped period.

The discontinuous SVPWM also provides a linear range of modulation index 0-115.4% [8]. It is, therefore, can increase the power handling capability of the converter, or its need for cooling, and increasing the converter power density. It is suitable to minimize the weight and volume of power electronics systems, as in electric vehicle and aircraft applications. Currently, the discontinuous SVPWM has become one the most promising modern PWM methods which is used in various power electronics such as motor drives, front-end converter, and active filter.

In this paper, we design and discuss implementation of a FPGA based SVPWM with a different approach, in which the judging of sectors and the calculation of the time vectors for active and null vectors to generate the SVPWM waveform is simple, and also the switching losses is low. In this paper, a novel 5-segment discontinuous SVPWM design based on the basic idea from [1] is proposed. This scheme has lower switching losses, simpler algorithm and designed using Xilinx ISE and can be implemented easily based on Spartan 3E FPGA

II.SVPWM CONTROL OF PMSM

2.1 SVPWM CONTROL

In order to control PMSM efficiently, the Field Oriented Control (FOC) is often applied. FOC is an excellent control algorithm that is used to control space vectors of magnetic flux, current and voltage. Actually, FOC relies on the SVPWM control strategy. By using SVPWM, it is possible to set up the coordinate system to decompose the vectors into a magnetic field-generating axis and a torque-generating axis. So by using SVPWM, the PMSM control is almost the same as the DC motor control, the magnetic flux and torque can be controlled separately [11].

Generally, in the PMSM control system, the SVPWM module generates the vector control signals, and then thesePWM signals are sent to the inverter in order to drive the motor. The basic diagram of SVPWM control for PMSM can be described as Fig. 1. The power switches of the inverter, shown as Fig. 2, consist of 6 IGBT switches (S1, S2, S3,S4, S5 and S6)[11].

Table 1. The Comparison of the Different Modulation Schemes [12]

Parameters	SPWM	Conventional SVPWM	Discontinuous SVPWM
P_L (per-unit of SPWM)	1.00	1.33	0.83
T_J (increase, °C)	35	45	32
Weighted THD (%)	4.0	1.8	2.9

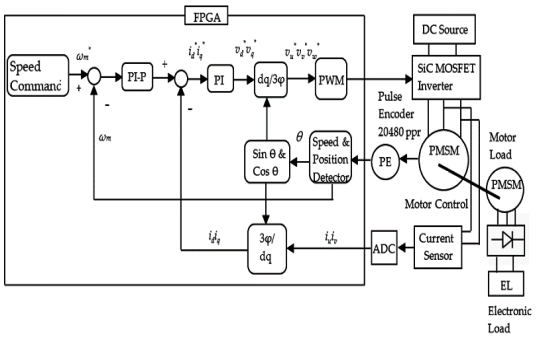

Fig. 1. The Basic Diagram of SVPWM Control for PMSM

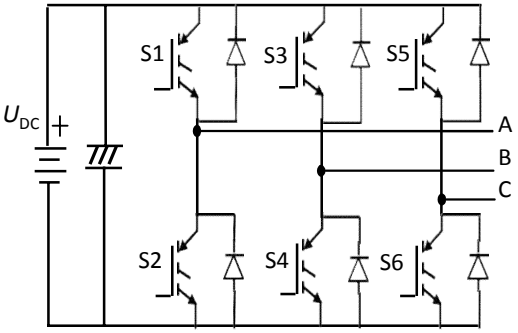

Fig. 2. Power Switches of the Inverter

The main aim of any modulation technique is to obtain variable output having a maximum fundamental component with minimum harmonics and less switching losses. The SVPWM technique is more popular than conventional technique. This technique was originally developed as a vector approach to pulse width modulation (PWM) for three phase inverter [7]. It is a more sophisticated technique for generating sinusoidal wave that provides a higher voltage to the motor with lower total harmonic distortion. It confines space vector to be applied according to the region where the output voltage vector is located. SVPWM refers to special switching scheme of the six power transistor of a three phase power converter. It is based on fact that there are only two independent variables in a 3-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase-voltage vector can be expressed as:

$$V_{ref} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (1)$$

In the SVPWM scheme, the 3-phase output voltage is represented by a reference vector which rotates at an angular speed of $\omega = 2\pi f$. The task of SVM is to use the combinations of switching states

toapproximate the reference vector, V_{ref}. To approximate the locus of V_{ref}, the eight possible switching states of the inverter are represented as 2 null vectors and 6 active vectors. The operating states and corresponding vectors are listed in Table 2.

TABLE 2: Switching State of the 2-Level Inverter

Space vector		Switching state	On switches S
Zero vector	V_7	111	1, 3, 5
	V_0	000	2, 4, 6
Active vector	V_1	100	1, 2, 4
	V_2	110	1, 3, 6
	V_3	010	2, 3, 6
	V_4	011	2, 3, 5
	V_5	001	2, 4, 5
	V_6	101	1, 4, 5

The SVPWM strategy aims to minimize harmonic distortion in the current by selecting the appropriate switching vectors and determining of their corresponding dwelling widths. The choice of the null vector determines the SVPWM scheme. There are some options: the null vector V0 only, the null vector V7 only, or a combination of null vectors. The equivalent PWM waveforms, which produce the same average flux, may consist of various combinations of the basic vectors. The characteristic of each those strategies above can be resumed as shown in Table 3.

Table 3. Comparison of SVPWM Patterns

No	Pattern SVPWM (based on sector I)	Number of segments	Number of commutation in one sampling period	THD	Easiness to implementation FPGA
1	V_0-V_1-V_2-V_7-V_2-V_1-V_0	7	6	low	quiet-difficult
2	V_7-V_2-V_1-V_0-V_1-V_2-V_7	7	6	low	quiet-difficult
3	**V_1-V_2-V_7-V_2-V_1**	**5**	**4**	**almost low**	**easy**
4	**V_0-V_1-V_2-V_1-V_0**	**5**	**4**	**almost low**	**easy**
5	V_0-V_1-V_2-V_7	4	3	almost significant	not-easy
6	V_0-V_2-V_1-V_7	4	3	almost significant	not-easy
7	V_1-V_2-V_7 and V_2-V_1-V_7 alternately	3	2 and 3 alternately	higher significant	not-easy

2.2 PROPOSED SVPWM SWITCHING PATTERN (5 - SEGMENT DISCONTINUOUS DISCONTINUOUS SWITCHING SEQUENCE)

There has been reported many discontinuous SVPWM pattern. However, not all those patterns have lower switching losses, simpler algorithm and can be implemented based on FPGA easily. In this paper, a novel symmetric 5-segment discontinuous SVPWM design refer to the basic idea from [1] is proposed. It is known has lower switching losses, simpler algorithm and can be implemented easily. Therefore, this paper proposes to implement this pattern based on FPGA in order to boost system performance of SVPWM. In this pattern, there is always a channel staying constant for the entire PWM period. The state sequence in this pattern is X-Y-Z-Y-X, where Z=1 in sector I, III and V, and Z=0 in the remaining sector. So the number of switching time for this pattern is less than the conventional pattern. The obvious result of this is reduced.

2.3 PROPOSED IDENTIFICATION OF THE SECTOR

Several methods have been introduced to judge the sector where the reference space voltage vector lies. Zhi-pu [14] compared the reference space vector's angle with 0^0, 60^0, 120^0, 180^0, 240^0, 300^0 ,360^0 to achieve the number of the sector in which V_{ref} lies as shown in figure 3.

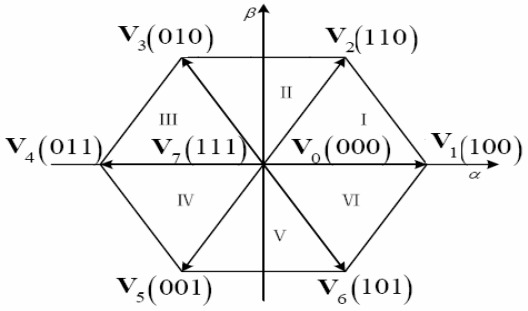

Fig. 3.Vector Plane Frame of Space Voltage Vectors

Table 4: Criterion of the Sector Identification

Sector	Vector Angle	V_α,V_βConditions
I	$(0^0, 60^0)$	$0 \le V_\beta \le \sqrt{3}V_\alpha$
II	$(60^0, 120^0)$	$V_\beta \ge \sqrt{3}V\alpha \; and \; V_\alpha \ge 0 \, , or$ $V_\beta \ge -\sqrt{3}V_\alpha \; and \; V_\alpha < 0$
III	$(120^0, 180^0)$	$0 \le V_\beta \le -\sqrt{3}V_\alpha$
IV	$(180^0, 240^0)$	$\sqrt{3}V_\alpha < V_\beta \le 0$
V	$(240^0, 300^0)$	$V_\beta \ge \sqrt{3}V\alpha \; and \; V_\alpha \ge 0 \, , or$ $V_\beta \ge -\sqrt{3}V_\alpha \; and \; V_\alpha < 0$
VI	$(300^0, 360^0)$	$-\sqrt{3}V_\alpha \le V_\beta \le 0$

2.4. DETERMINATION OF THE DURATION OF ACTIVE VECTORS

The calculation of the durations of the base vectors is described based on Figure 4.

Supposing the reference voltage space vector us falls between two adjacent base vectors, u1 and u2 , the reference vector us can be represented with the combination of the two vectors, u1 and u2 :

$$\underline{u}_s = \underline{u}_1 r_1 + \underline{u}_2 r_2 \quad (2)$$

where, r_1 and r_2 are coefficients.
Using the basic trigonometric relations we get:

$$\begin{cases} r_1 u_1 = u_s cos\theta - BC = u_s cos\theta - DC.tan30^\circ \\ \quad = u_s cos\theta - u_s sin\theta.tan30^\circ \\ = u_s\left(cos\theta - \frac{1}{\sqrt{3}}sin\theta\right) = \frac{2}{\sqrt{3}}u_s(sin60^\circ cos\theta - cos60^\circ sin\theta) \\ \quad = \frac{2}{\sqrt{3}}u_s sin(60^\circ - \theta). \\ r_2 u_2 = \frac{AO}{cos30^\circ} = \frac{u_s sin\theta}{\sqrt{3}/2} = \frac{2}{\sqrt{3}}u_s sin\theta. \end{cases} \quad (3)$$

where, u_1 and u_2 are the length of the two vectors with the value $\frac{2}{3}U_{dc}$, and u_s is the length of vector $\underline{u}_s$. To summarize we get :

$$\begin{cases} r_1 = \sqrt{3}\frac{u_s}{U_{dc}} sin(60^\circ - \theta) \\ r_2 = \sqrt{3}\frac{u_s}{U_{dc}} sin\theta \end{cases} \quad (4)$$

For θ between 0 and 60°, r_1 and r_2 are within the range [0, 1]. They take the maximal value 1 when $\underline{u}_s$ coincides with $\underline{u}_1$ or $\underline{u}_2$, respectively. $r_1 + r_2 = 1$ when $\underline{u}_s$ reaches the dashed line between the arrow peaks of $\underline{u}_1$ and $\underline{u}_2$.

This equation means that one should combine r_1 part of $\underline{u}_1$ and r_2 part of $\underline{u}_2$ to obtain the reference voltage $\underline{u}_s$. Since it is not possible to change the magnitude of the base vectors, $\underline{u}_1$ and $\underline{u}_2$, the combination is realized (approximated) using time division, as shown in Figure 4. If $\underline{u}_s$ doesn't touch the dashed edge of the triangle, the sum of r_1 and r_2 is less than 1. Therefore, the rest time is filled with zero vectors.

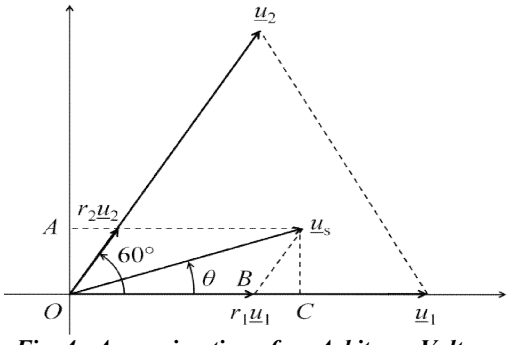

Fig. 4. Approximation of an Arbitrary Voltage Space Vector Using Base Vectors

The three time durations are defined as

$$\begin{cases} T_0 = (1 - r_1 - r_2)T \\ T_1 = r_1 T \\ T_2 = r_2 T \end{cases} \quad (5)$$

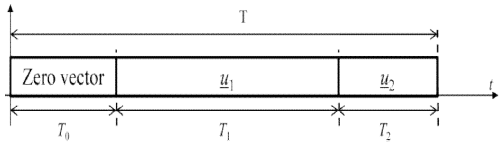

Fig. 5. Combination of Vectors Using Time Division

where T is the PWM period, T_0 is the duration for zero vector, and T_1 and T_2 the durations for vector $\underline{u}_1$ and $\underline{u}_2$, respectively.

These equations mean that an arbitrary space vector within the triangle defined by the two adjacent base vectors, between which the expected vector is located, can be represented by the sum of these two vectors. This is realized by timely activating the two vectors combined with zero vectors sequentially. If the switching process is fast enough, meaning the period T is short, the approximation can precisely represent the reference vector.

III. A SIMPLE REALIZATION METHOD OF SVPWMALGORITHM

3.1 PROPOSED IDENTIFICATION OF THE SECTOR

There are many kinds of methods to judge the sector that the reference space voltage vector lies in. Zhi-pu [14]compares the reference space vector's angle with 0^0, 60^0, 120^0, 180^0, 240^0, and $300^0$to obtain the number of the sector that the V_{ref} in. To determine the sector, they calculate the projections V_a, V_b and V_c of $V_\alpha$and $V_\beta$in (a,b,c) plane by using inverse Clark transformation, as follow:

$$\begin{cases} V_a = V_\beta \\ V_b = \frac{\sqrt{3}V_\alpha - V_\beta}{2} \\ V_b = \frac{-\sqrt{3}V_\alpha - V_\beta}{2} \end{cases} \quad (6)$$

Then, based on equation (6), they calculate N=sign(Va) + 2*sign(Vb) + 4*sign(Vc). Map N to the actual sector of the output voltage reference by referring to Table 5 below.

Table 5: Map N to the Actual Sector of the Output Voltage Reference

N	1	2	3	4	5	6
Sector	2	6	1	4	3	5

3.2. THE PROPOSED CALCULATION OF THE DURATION OF ACTIVE VECTORS

In this work, based on the analysis performed in [1], a new set of equations to calculate the duration of active vectors for each sector has beenrearranged in order to construct an easier implementation based on FPGA.

The equations associated with each sector are shown in Table 6.

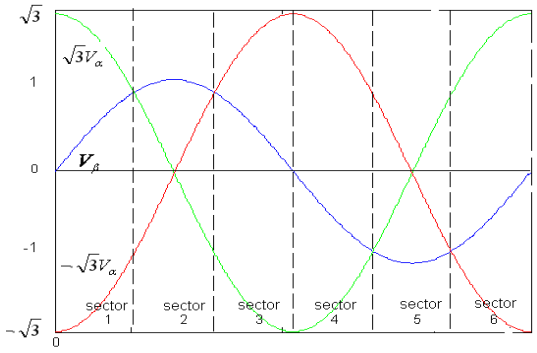

Fig.6. Plotting of $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ wave

Table 6: The Switching Time of the Active Vector for Each Sector

Sector	T_a	T_b	T_a+T_b
I	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
II	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
III	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
IV	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}+\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
V	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
VI	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}}-\frac{V_\beta}{\sqrt{3}V_{dc}}\right)$

3.3 PROPOSED SVPWM SWITCHING SEQUENCE GENERATING METHOD BASED ON CALCULATION OF THE DURATION OF ACTIVE VECTORS

In this paper, with refer to equation $y=\frac{2m}{T}x$in Figure 7, the PWM generating for odd sector are realized through comparison between triangle and T_a, and between triangle and T_a+$T_b$with other switching is set equal to 1; while for even sector, the PWM generating are realized through complement of comparison between triangle and T_a, and complement of comparison between triangle and T_a+$T_b$with other switching is set equal to 0. For example, in sector I if $x=T_a=\frac{T_0}{2}$ then $y=\frac{2m}{T}(T_0/2)$and if $x=T_b=\frac{T_1}{2}$ then $y=\frac{2m}{T}(T_1/2)$.

For more simplicity of circuit design, in this paper the Term $\frac{2m}{T}$ is set equal to 1, so if $x=\frac{T_0}{2}=T_a$ then$y=\frac{T_0}{2}=T_a$, and if $x=\frac{T_1}{2}$ then y=$\frac{T_1}{2}=T_b$. Obviously if $x=\frac{T_0}{2}+\frac{T_1}{2}=T_a+T_b$ then $y=\frac{T_0}{2}+\frac{T_1}{2}=T_a+T_b$. Therefore, the PWM generating for S_b and S_c channels in sector I can be obtained through comparison between triangle and T_a , and between triangle and T_a + T_b respectively and S_a Channel is set equal to 1. Moreover, the PWM generating in other sectors can be obtained in the similar way.

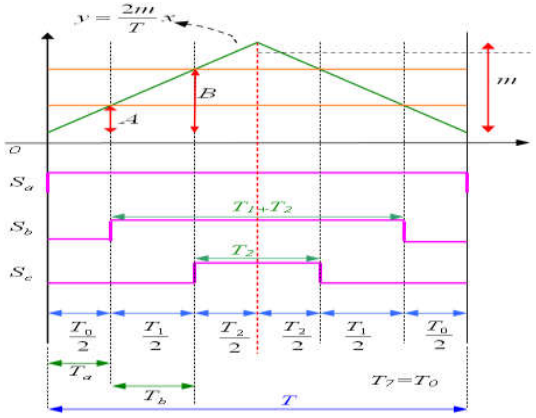

Fig.7. Proposed SVPWM Switching Sequence Generating Method

IV. FPGA IMPLEMENTATION OF A PROPOSED SVPWM

In previous section, the principle of SVPWM is analyzed. In this section FPGA implementation of a proposed novel SVPWM will be presented. Overall of the proposed SVPWM design is shown in Figure 8. This top module can be sub divided into 5 sub modules, namely ajust_freq, Vbeta_Valfa, find_sector, SVM_generator and deadtime_sytem module.

4.1. FIRST MODULE: ajust_freq

From Figure 8, the function of ajust_freq is to generate a suitable clocking frequency. In the proposed SVM design, this module functions as a frequency divider by generating a carrier frequency of 20 kHz and a fundamental frequency of 50 Hz from the FPGA board, which have a clocking signal of 33.33 Mhz. Since the triangle signal generator in this design is sampled to be 32 times per period, in order to get a carrier frequency of 20 kHz, the main clock generator from the FPGA board was divided by 13 (33.33 MHz: (13 * 32)= 20 kHz).

4.2. SECOND MODULE: Vbeta_Valfa

In the proposed method, Valfa and Vbeta are generated based on sine and cosine functions through the look-up table (LUT) with a memory mapping of 360 addresses. There are three lines, categorized as lower, base, and upper, into 9 unsigned bits. With the memory mapping of 360 addresses, the counter mod-360 will used to count the LUT of Valfa and Vbeta. The RTL design for this is shown in figure 9.

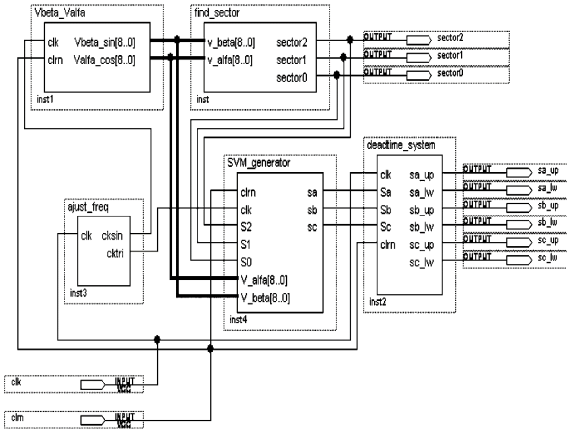

Fig. 8. Overall of the proposed SVM design

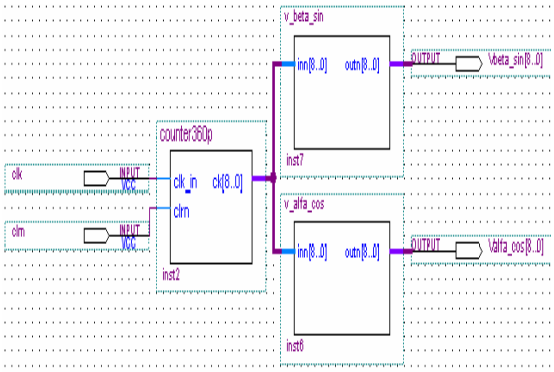

Fig.9. Vα and Vβ Module

4.3. THIRD MODULE: find_sector

Due to the different switching time equations, a reference voltage sector is necessary. The sector finder (SF) module shown in figure 10, in this design is used to judge the reference vector sector by referring to Table 4. This module determines the number of sectors and simplifies the truth table by comparing the above-mentioned results.

4.4. FOURTH MODULE: SVM_generator

This module was divided into four sub-modules, namely Triangle, Duration_Ta, Duration_TaTb, and SVM pattern modules. The Triangle module functions as a triangle signal generator for carrier signal. In the proposed SVM design, one period of triangle signal generation is sampled 32 times. The Duration_Ta and Duration_TaTb modules are realized using Table6. Finally, the SVM pattern module is used to generate the SVM sequence as shown in figure 11.

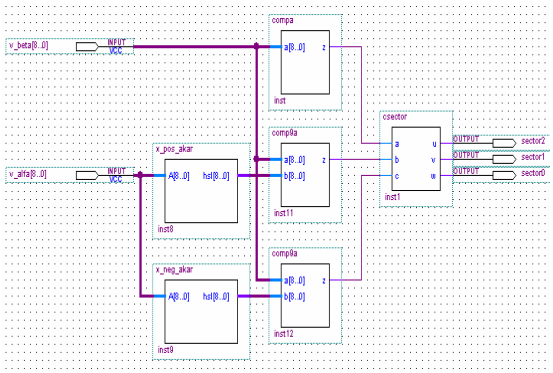

Fig.10. Sector Finder (SF) Module

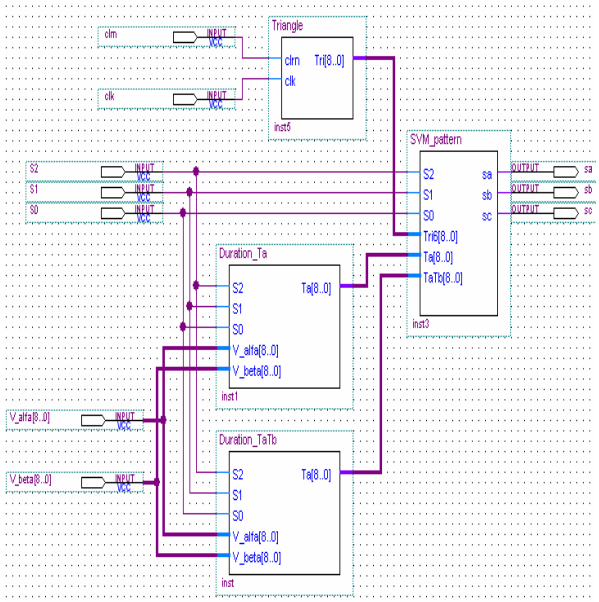

Fig.11. Three Phase SVPWM Signal Generator Module

4.5. FIFTH MODULE: deadtime_system

A dead-time of at least 2 µs is required to avoid short circuit within a leg. A combinationof a 16-bit counter and a 16-bit comparator is used to construct the dead-time generator for each leg.

V. CONCLUSION

In this paper, a new FPGA based PMSM control system and the Top-Down design is proposed, method based on FPGA is presented. The PMSM

control system is programmed in VHDL, and then is implemented in the FPGA system. The RTL design of SVPWM has been designed with its various module such as sector identification, Valfa & Vbeta module, and three phase SVPWM signal generator in VHDL using Xilinx. The hardware/software co-design of PMSM control system can be realized easily using this new SVPWM approach.

A theoretical study concerning the SVPWM control strategy on the voltage inverter based on FPGA is presented. This aims on the one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction. SVPWM is among the best solution to achieve good voltage transfer and reduced harmonic distortion in the output of an inverter

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