Design of PLC Receiver Using Clock Gating for DFT

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Abstract: Smart Grids are becoming a reality all over the world. Nowadays, the research efforts for the introduction and deployment of these grids are mainly focused on the development of the field of Smart Metering. This emerging application requires the use of technologies to access the significant number of points of supply (PoS) existing in the grid, covering the Low Voltage (LV) segment with the lowest possible costs. Power Line Communications (PLC) have been extensively used in electricity grids for a variety of purposes and, of late, have been the focus of renewed interest. PLC are really well suited for quick and inexpensive pervasive deployments. However, no LV grid is the same in any electricity company (utility), and the particularities of each grid evolution, architecture, circumstances and materials, makes it a challenge to deploy Smart Metering networks with PLC technologies, with the Smart Grid as an ultimate goal. This paper covers the evolution of Smart Metering networks, together with the evolution of PLC technologies until both worlds have converged to project PLC-enabled Smart Metering networks towards Smart Grid. This paper develops guidelines over a set of strategic aspects of PLC Smart Metering network deployment based on the knowledge gathered on real field; and introduces the future challenges of these networks in their evolution towards the Smart Grid.

Keywords— Design-for-testability (DFT), PLC at ICs, PLC receiver, power line communications (PLCs).

I. Introduction

The Smart Grid is recognized today as a revolutionary concept that, even with some of the problems associated to the lack of consensus over a unique and closed definition, is in the process of being implemented in many electricity grids all over the world. Within the aspects that may be highlighted as standing within the consensus of the utility community in the Smart Grid definition, we find the addition of recent advances of electronics, and information and communications technologies (ICTs) applied on the distribution grid electricity assets, to get a better energy supply based on remote monitoring and metering of the existing assets, a better adjustment between energy production and consumption, the optimization of operation reaction times, and the improvement in the grid technical losses. Smart Metering is the application that is experiencing greater support both from the industry and utilities, that find in the deployment of smart meters an opportunity to build the foundations for a larger scope Smart Grid, while obtaining some immediate advantages derived from the savings and commercial opportunities based on the real time access to customers' smart meters. PLC is a telecommunications technology with a long history and tradition in electricity companies, with a wide scope of applications, varieties and implementations. The confluence of the Smart Metering and PLC technologies has been highlighted from the very first conception of PLC systems, and increasingly in the last decades. The projection of PLC into the Smart Grid is a matter

that has been specifically addressed recognizing in PLC "an excellent and mature technology that can support a wide variety of applications from the transmission side to the distribution side and also to and within the home". From a purely academic perspective, the evolution of the subjects focusing the attention of researchers on PLC has followed the historical path of industry interest (high voltage (HV)-lines propagation, metering and control, medium voltage (MV)-environment, broadband (BB) access, and in-home communications). Of late, Smart Grids have focused much of the attention of both industry and academic world, through an evolution in which Smart Metering has been the core of the interest. The PLC literature is mainly composed of academic papers focused on low level specific details of PLC technology. Noise, channel characteristics, modulation schemes, MAC architectures, etc. are extensively covered by academic researchers. With all this information, PLC technology has managed to progress and evolve into different system specifications that have subsequently been applied on real field to provide real services. However, the application of any PLC technology to the electricity grid is not straightforward. The so-called "PLC learning curve" might not be easy for an electricity company that needs to make use of PLC to deploy a service-oriented PLC system. Electricity grid specific details are not often found in the conventional scientific literature and even in the electricity industry related associations (e.g., [11]). Thus the deployment of PLC solutions is often a field in which utilities cannot be easily assisted, as not many general public technical references can be found. It is the opinion of the authors that this circumstance is the main reason of the slow and unequal adoption rate of PLC technologies in the different utilities. The causes for these non-existing standard deployment guidelines include reasons such as application of the technology on real grids being far from academics, electricity grid being a transmission media that needs skilled technicians to be handled and that is not accessible to the general public (with the exception of the in-home segment), and PLC technology not being a conventional transmission media for telecommunication specialists. This paper will contribute to solve these aspects, providing guidelines for the deployment of Smart Metering systems.

Power line communications (PLCs)

Power lines were originally devised to transmit electric power from a small number of sources (the generators) to a large number of sinks (the consumers) in the frequency range of 50-60 Hz. It is a fact that power transmission towers and lines are some of the most robust structures ever built. Historically, the PLC technology has very limited applications but now we are witnessing the possibility of it being acclaimed universally as a prime mode of long-haul data communication. With the inevitable arrival of broadband access, the demand for sending digital voice, video and Internet data within the home increases continuously. While retrofitting the houses and neighborhoods with special wires is one option, it is expensive and time consuming. PLC Technology allows the use of the existing and widespread power distribution infrastructure to provide high speed networking capabilities along with many other benefits.

Block diagram of PLCs

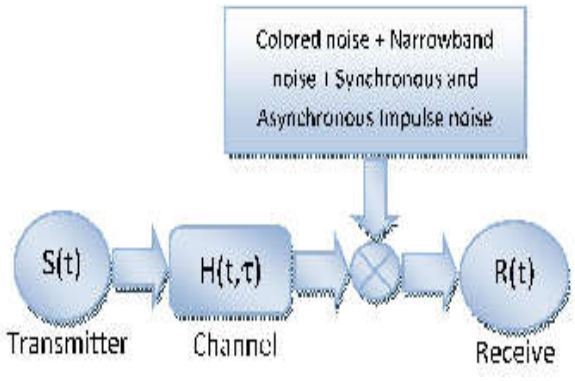


Figure.1: Block diagram for PLC systems.

II. Literature Survey

In recent years, the advancement in broadband over power line technology and its perceived potential has lead to several studies been performed to determine its feasibility for use for communications in several systems, such as airplanes, cars, airport lighting systems, ships and space shuttles, that have pre-existing power cables. Our group proposed PLC in ICs to reduce the pin count, size, and hence the cost of a chip initially and later to increase the channel capacity for the multiple parallel scan design. To follow up the proposal, we investigated several relevant topics for PLC in ICs, and reviewed them briefly as follows. We measured the propagation loss from a core power supply pin to an on-chip node of a PDN of a cold Pentium 4 die (65 nm version). The largest pass band was observed ~2 GHz over a 200-MHz band, and the path loss increases above 40 dB beyond 2.5 GHz. Other measurements were carried out on three different samples of cold 45-nm Core 2 Duo processors and two randomly picked locations on the PDNs. The averaged transfer function shows narrow sporadic pass bands, where about 5%~7% of the input signal passes through the PDN. We observed that there is little correlation between the pass bands of the 65 nm Pentium 4 and that for the 45-nm Core 2 Duo processors. We suggested the use of ultra wideband (UWB) and direct-sequence code division multiple access (DS-CDMA) communication technologies to circumvent the blocking of data signals in low frequencies at packages and PDNs and increase the SNR. Compared with the traditional narrow-band communication systems UWB signaling has several advantages, such as high data rate, low average power, and simple RF circuitry. Shannon's theorem states that the channel capacity is given as B×log2 (1+SNR), where B is the bandwidth. As the bandwidth is much larger (on the order of several gigahertz) for UWB than a narrow-band signal, the SNR can be much smaller for UWB to achieve the same data rate. The DS-CDMA technology assigns a codeword to each bit of information called spreading, and orthogonal code words are assigned to different users or power pins for the PLC in ICs to support multiple channels. The spreading operation represents 1 bit of data as a series of binary pulses spread over a codeword, which increases the pulse repetition frequency. The benefit of spreading is the processing gain, which is 10 × logs (spreading_ factor) in decibel. For example, the spreading factor for 4-bit code words is 4, which yields a processing gain of 6 dB, or increases the SNR by 6 dB. We also investigated the modeling of I/O pads and PDNs, and estimated the performance of the proposed PLC systems.

Home automation, also referred to as home control, smart home, smart house, or intelligent home is actually a collection of devices, systems, and subsystems which have the ability to interact with one another or function independently. Power Line Communication (PLC) is called power-line carrier or a mains communication. PLC uses electric power lines to carry information over the power line. It is a technique used in home automation for remote control as it can use the household electrical power wiring as a transmission medium. PLC has been a very important interdisciplinary topic for power, communications, industrial, and automation engineers and researchers since the 1980s. PLC promises to be an enabling home network technology due to its ability to deliver data over existing power lines in homes. Similar to RF, the power line is a shared medium that exists in a noisy environment, although the respective noise sources differ markedly. Motors, switch-mode power supplies, fluorescent ballasts, and other impairments, which generate substantial impulse and wideband noise share power lines. Recently, with the explosive growth of the Internet and telecom technology home automation experience an accelerating growth based on

different kinds of residential network. At the present there are several kinds of transmission medium in residential network, such as coaxial-cable, radio, microwave, millimeter wave, power line and fiber optics. Compared with other kinds of transmission medium, power line has distinct advantage in setting up a network without additional line 6 installation and existing digital devices, including home appliances and information devices, at a very low cost. Many applications are operating at high speed and a fixed connection is often preferred. If the power utilities could supply communication over the power line to the customers it could make a tremendous breakthrough in communication. Every household would be connected at any time and services being provided at real time. Using the power line as a communication medium could also be a cost effective way compared to other system because it uses an existing infrastructure, wire exists to every household connected to the power line network. On the other hand, device power in home automation still can be supplied by power line itself. So PLC rapidly becomes a popular solution to set up residential network. Concerning the former, one should consider that the targets are conventional houses, adapted when users have an accident leading to disability or when they get older. Signal strength or signal attenuation in home electrical line is important for design of home automation communications circuits. PLC communication signals via main power lines are transmitted from a part of the home and received at the other side. Measurements are carried out between general divisions of a home such as kitchen, bedrooms, living room, hall, and bathroom, etc. Connectors are used to deliver power lines in the divisions of homes. Connectors are placed at the wall between two neighbor divisions at home. So power is delivered via these connectors to every division. Connectors are induced an additional attenuation. Power-line distances measured for signal attenuations given are between 6–30 m.

Design for Testability Using Scan path Techniques for Path-Delay Test and Measurement

This paper describes a novel flip-flop design which is used in performing internal path-delay test and measurement using scan path technique:. Also described is the design for a boundary-scan cell that enables input/output delays to be measured. The paper includes a real-life application example.

Conditionally Robust Two-Pattern Tests and CMOS Design for Testability

The concept of a conditionally robust two-pattern test for testing stuck-open transistor faults in CMOS gates is introduced. Such a test is conditionally hazard-free; i.e., the transition will not produce a hazardous output provided a (partial) order is imposed on the time instants at which the components of the input pattern undergo transition. Two sources of the existence of such a partial order are identified:

(i) When a set of transistors is controlled by the same logic signal, the symbolic layout (routing) information provides the knowledge of such a partial order;

(ii) Multi pattern tests, which may be necessary to test embedded CMOS gates, can be looked upon as two pattern tests with an imposed partial order. Algorithms are given to (a) determine whether a two-pattern test is conditionally hazard-free under a given partial order and (b) compute minimal Cardinality partial orders which, when imposed on a transition, make it conditionally hazard-free.

III. PROPOSED SYSTEM

The proposed on-chip PLC receiver receives the data superimposed on power lines, and the data (such as scan test data) are sent from a test instrument. Therefore, the transmitter for the PLC receiver is an external instrument rather than the one on the same chip. The receiver was designed in CMOS 0.18-μm technology with a supply voltage of 1.8 V. It consists of three

building blocks, and this section describes the design of each building block.

A. Block Diagram

A block diagram of the proposed PLC receiver is shown in Fig. 2.

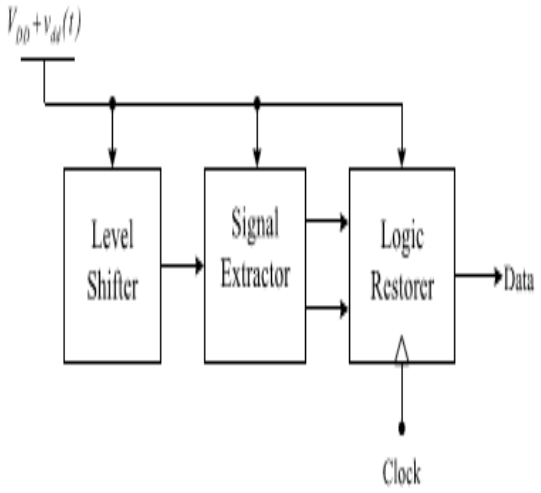


Figure.2: Block diagram of the proposed PLC receiver.

The proposed PLC receiver consists of three blocks, each sharing the same supply voltage (VDD+vdd(t)).The first block is a level shifter, which lowers the dc level of the signal superimposed on the supply voltage. The level shifted signal is processed by the subsequent block, a signal extractor, which amplifies the signal and converts it to a differential signal. The logic restorer, which is a differential Schmitt trigger, recovers logic values from the differential signal. The design and operation of each block is explained below.

B. Level Shifter

The level shifter shown in Fig. 3 can be treated as a common source amplifier with diode-connected load as, in which the amplifier input is fixed to a bias voltage Vbias.

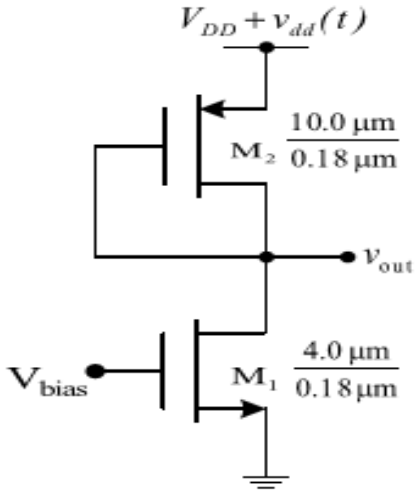


Figure.3: Level shifter.

The level shifter propagates the data signal vdd(t) imposed on the supply voltage VDD to the output while lowering the dc voltage level of the signal to 0.5VDD. To propagate the data signal superimposed on the supply voltage to the output, the output should be sensitive to supply voltage variations. In other words, contrary to a typical amplifier design, the power supply rejection ratio (PSRR) of the level shifter should be set to small. The PSRR of the common source amplifier with the gate of M1 as the input is defined as the ratio of the voltage gain from the input to the voltage gain from the supply voltage

$$\text{PSRR} = \frac{A_v}{A_{V_{DD}}} \quad \text{---}\rightarrow 1$$

Where Av is the small-signal voltage gain from the input (i.e., the gate ofM1)to the output of the amplifier, and A_{VDD} is the small-signal gain from the power supply to the output. Av is obtained as

$$A_v \approx -\frac{g_{m1}}{g_{m2}} \quad \text{---}\rightarrow 2$$

Where gm1andgm2are the transconductances ofM1 andM2, respectively. A_{VDD} is obtained as in (3) and becomes 1 ignoring the channel length modulation

$$A_{V_{DD}} = \frac{r_{o1}}{1/g_{m2} + r_{o1}} \approx 1. \quad \text{------}\rightarrow 3$$

Thus, the PSRR of a common source amplifier is expressed as

$$\text{PSRR} \approx -\frac{g_{m1}}{g_{m2}}. \quad \text{--------}\rightarrow 4$$

The transconductance of a MOS transistor is

$$g_m = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH}). \quad \text{-------}\rightarrow 5$$

By substituting (5) in (4), the PSRR becomes

$$\text{PSRR} \approx \frac{\mu_n (W/L)_1 (V_{GS} - V_{TH})_1}{\mu_n (W/L)_2 (V_{GS} - V_{TH})_2}. \quad \text{-------}\rightarrow 6$$

Equation (6) indicates that the PSRR can be lowered by setting (W/L)1 small, (W/L)2 large, the overdrive voltage of M1 small, and the overdrive voltage of M2 large. This means that the bias voltage and the W/L ratio of M1 should be set to small, while operatingM1 in saturation. Since the desired dc voltage level at the output of the sensing circuit is 0.5 VDD, the condition sets the overdrive voltage of M2. A large W/L ratio forM2increases the current ID, and so it is a compromise between low-power dissipation and low PSRR. The overdrive voltage (VGS–VTH) of M1 is set to a near minimal (=0.08 V) for the proposed level shifter and that for M2 large (=0.373 V). In addition, (W/L)1 is set relatively small (=22.2), and (W/L)2 relatively large (=55.6). The resultant PSRR for the level shifter is 1.3 (or 2.27 dB), which is small compared with a typical value of analog amplifiers ranging from 65 to 80 Db.

C. Signal Extractor

The input signal of the signal extractor is the data signal offset with 0.5 VDD, and the signal extractor amplifies the data signal while removing the dc offset voltage. The signal extractor shown in Fig. 4 is a differential amplifier, in which one input is connected to an RC low-pass filter.

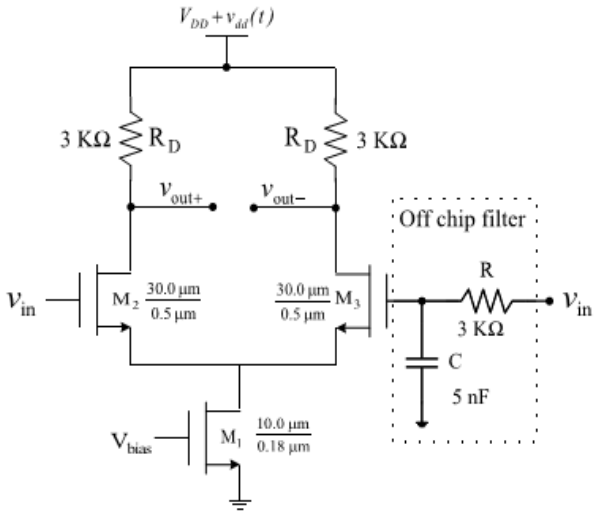


Figure.4: Signal extractor

The low-pass filter intends to extract the dc value of the signal. The differential amplifier rejects the common-mode signal of the two inputs or the dc value. It also converts a single-ended input into a differential output pair. The voltage gain of the differential amplifier is expressed as

$$A_v = -g_{m2,3} R_D \quad \text{-----}\rightarrow 7$$

Where gm2 and gm3 are equal to $\mu C_{ox}(W/L)(V_{GS}-V_{TH})$. The gain increases by increasing W/Land/or RD at the cost of a larger device size and increased parasitic capacitances. A larger RD also leads to a higher voltage drop to limit the maximum voltage swing. The transistor size, W/L, of the proposed signal extractor is set to 30/0.5 µm and RD to 3 **KΩ**, which achieves the amplifier gain of 10 dB. It should be noted that a relatively large transistor size and a large resistor minimize the input dc offset due to mismatches. The RC low-pass filter intends to pass the dc value, which can possibly vary or fluctuate, while removing the signal. The filter is off-chip for our test chip, which enables us to try different cutoff frequencies. The resistor R of the filter

issetto3Kand the capacitor 5 nF for our experiments. The−3 dB cutoff frequency of the RC filter is 10.6 KHz. Note that it is desirable for the RC-filter to be on-chip for the final design, which is possible through the increase of the data rate and hence the cutoff frequency.

D. Logic Restorer

The logic restorer translates the data in the form of an analog differential signal into logic values. It is based on the differential Schmitt trigger presented and is shown Fig. 5.

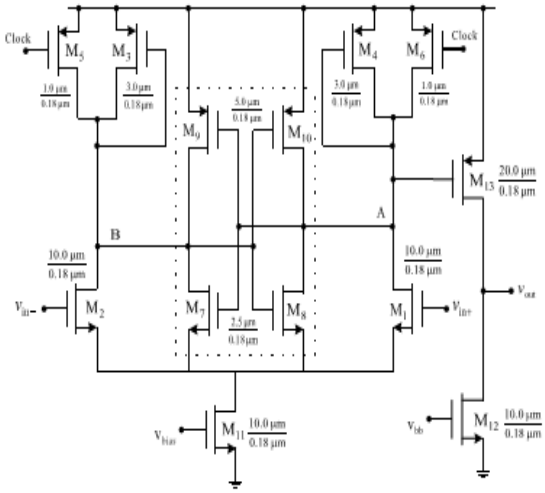


Figure.5: Differential Schmitt trigger

A key aspect of the Schmitt trigger is the hysteresis generated through the regenerative feedback circuit, specifically a cross-coupled inverter pair. When a new data signal is applied to the logic restorer, the clock is turned from low to high and turns OFFM5 and M6. It reduces the current supplied to the differential amplifier, which results in a smaller gap between the high and the low threshold voltages. The cross-coupled inverter pair settles to a high or low state, and hence the output of the logic restorer. Then, the clock signal becomes low, andM5 and M6 are turned ON. The gap between the two threshold voltages becomes wider, which increases the immunity to noise and disturbances.

E. Scalability and Location of the PLC Receiver

The level shifter is a rather unique block and specific for our PLC receiver. The level shifter has two transistors in cascode, so it can be scaled to lower supply voltages easily. Consider that the resistive load for the signal extractor is replaced by a current source. Then, both the signal extractor and the Schmitt trigger have three transistors in cascode, which are common for analog circuits. Therefore, they would scale along with other analog circuits. It should be noted that the two blocks are commonly used building blocks for analog circuits, and have been migrated to the advanced processing technologies with lower supply voltages. When compared with digital circuits, analog circuits do not scale well in the supply voltage. Therefore, the proposed PLC receiver, or its variations, may not be applicable for extremely low supply voltages such as those for low-power digital circuits operating at very low supply voltages. The physical location of a PLC receiver on the chip affects its performance. Obviously, a PLC receiver located closer to the source, i.e., the power pin through which the data signal is applied, performs better. The cost is possibly a long signal path from the receiver to the target logic block to which the data are applied. Impact on the signal quality at various locations inside a chip was investigated, and simulation results for a ball grid array package are reported.

Clock gating of PLC receiver:

Clock gating is a methodology of turning off the clock for a particular block when it is not needed and is used by most SoC designs today as an effective technique to save dynamic power.

In SoC designs clock gating may be done at two levels:

• Clock RTL gating is designed into the SoC architecture and coded as part of the RTL functionality. It stops the clocks for individual blocks when those blocks are inactive, effectively

disabling all functionality of those blocks. Because large blocks of logic are not switching for many cycles it saves substantial dynamic power. The simplest and most common form of clock gating is when a logical “AND” function is used to selectively disable the clock to individual blocks by a control signal, as illustrated in Figure 1.

• During synthesis, the tools identify groups of FFs which share a common enable control signal and use them to selectively switch off the clocks to those groups of flops.

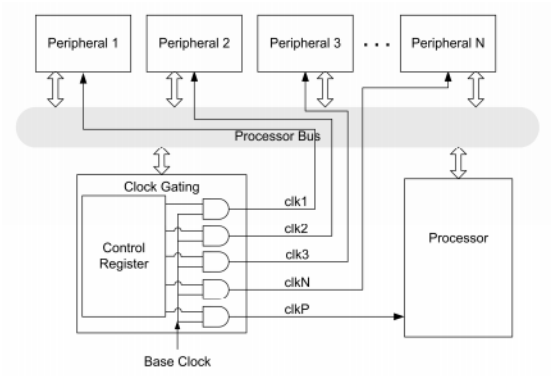


Figure.6: RTL clock gating in SoC to reduce dynamic power

Both of these clock-gating methods will eventually introduce physical gates in the clock paths which control their downstream clocks. These gates could introduce clock skew and lead to setup and hold-time violations even when mapped into the SoC, however, this is compensated for by the clock-tree synthesis and layout tools at various stages of the SoC back-end flow. Clock-tree synthesis for SoC designs balances the clock buffering, segmentation and routing between the sources and destinations to ensure timing closure, even if those paths include clock gating.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. A design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic. This clock gating logic is generally in the form of "integrated clock gating" (ICG) cells. However, the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree.

Clock gating logic can be added into a design in a variety of ways:

1. Coded into the Register Transfer Level (RTL) code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating).
2. Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific integrated clock gating (ICG) cells to gate the clocks of specific modules or registers.
3. Semi-automatically inserted into the RTL by automated clock gating tools. These tools either insert ICG cells into the RTL, or add enable conditions into the RTL code. These typically also offer sequential clock gating optimizations.

Any RTL modifications to improve clock gating will result in functional changes to the design (since the registers will now hold different values) which need to be verified.

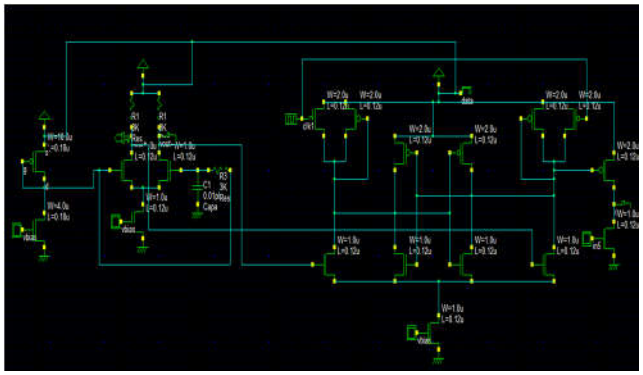
Sequential clock gating is the process of extracting/propagating the enable conditions to the upstream/downstream sequential elements, so that additional registers can be clock gated.

Although asynchronous circuits by definition do not have a "clock", the term **perfect clock gating** is used to illustrate how various clock gating techniques are simply approximations of the data-dependent behavior exhibited by asynchronous circuitry. As the granularity on which you gate the clock of a synchronous circuit approaches zero, the power consumption of that circuit approaches that of an asynchronous circuit: the circuit only generates logic transitions when it is actively computing.

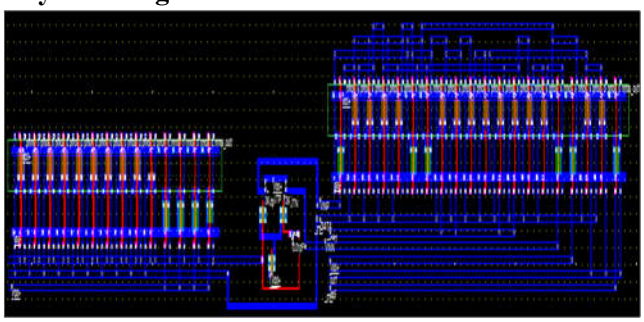
IV. RESULTS

PLC RECEIVER:

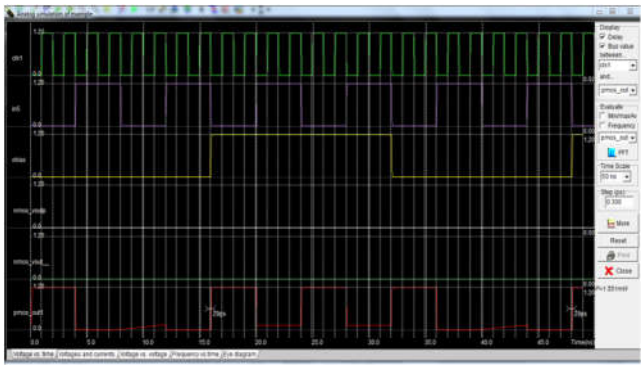
Schematic:



Layout Design:

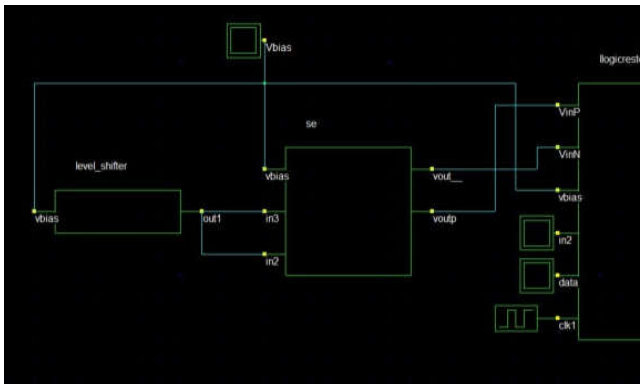


Simulation:

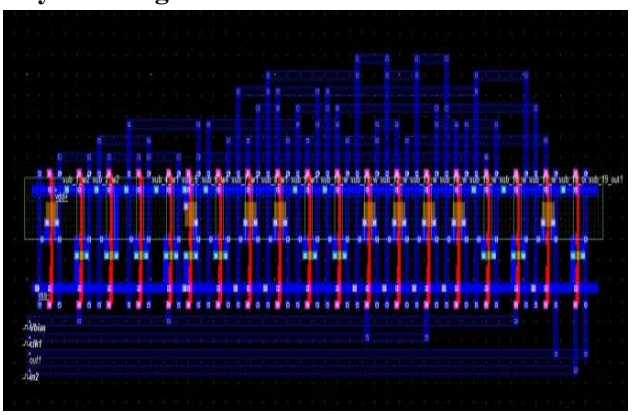


CLOCK GATING

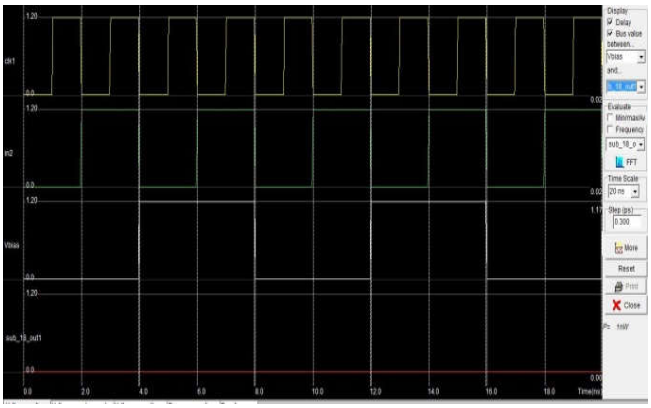
Schematic:



Layout Design:



Simulation:



V. CONCLUSION

A receiver for PLC at the IC level, which may be applicable to low data rate communications, like scan style, system debugging, and fault diagnosing, was investigated during this paper. The projected PLC system adopts a Binary raise modulation theme, and therefore the PLC receiver consists of 3 building blocks. The extent shifter shifts the dc level of the information signal to a 1/2 the provision voltage. The signal extractor supported differential electronic equipment, removes the dc voltage from the information signal with the help of a low-pass filter, that mitigates supply voltage fluctuations and droops. The logic renovator, based on a differential Schmitt trigger, extracts logic values from the information signal whereas rising the noise immunity of the receiver. The PLC receiver was designed to demonstrate the

practicability of a sturdy receiver as a signal of conception and fictional in CMOS zero.18-µm technology. The measurements show that the PLC receiver will tolerate a provide dip of zero.423 V or twenty three.5%. the ability dissipation for the receiver is three.2 mW under one.8 V supply. It needs a large scope of analysis efforts to use the potential of the PLC in ICs absolutely. To denote some, modeling of power pins, packages, and PDNs, channel characterization, modulation and multiple access schemes, SNR versus bit-error rates of a given system, design of PLC receivers and transmitters, and adverse impact of the info signals superimposed on power lines to the operation of digital circuits.

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