DESIGN OF CMOS BIO-SIGNAL AMPLIFIER USING 45 nm TECHNOLOGY

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ABSTRACT

Biomedical signals are observations of the physiological activities of various organs of the body. These signals are of extremely low amplitudes of the order of few micro volts. It is therefore inevitable that these signals need to be amplified to considerable levels so as to facilitate extraction of significant information from them. Previous work referred implements a dual-channel current reuse bio-signal amplifier dedicated for the low-power wireless body area network (WBAN) nodes using CMOS 180 nm Technology [1]. The prime requisites of any sensor node electronics are low power consumption, miniaturized nature and capability to detect biological signals like ECG, EEG, PPG, Blood flow, etc. Therefore this paper implements a low power CMOS bio-signal amplifier as in the literature, containing a pre-amplifier, programmable gain amplifier (PGA), low pass filter (LPF) and class AB amplifier but at 45 nm technology in order to attempt miniaturization and scaling.

Keywords: *CMOS, WBAN, Biomedical Signal Processing, scaling.*

INTRODUCTION

This paper discusses the design, construction and working of CMOS based bio-signal amplifier implemented in 45 nm technology. Nowadays, with an increased demand for healthcare and clinical treatment, wearable and implantable medical devices for the wireless body area network (WBAN) are of great concerned. These medical devices are useful in achieving real-time detection of bio-signals. Following figure shows a biomedical front-end system for the WBAN nodes, where the biological electrodes sense and acquire weak bio-potential signals which are amplified by bio-signal amplifier and then converted to digital signals by ADC, followed by an RF transmitter module for signal transmission. The bio-signal amplifier has a considerably vital impact on the system performance and hence an excellent design requires certain attributes such as low power consumption, low noise, high CMRR and high input impedance.

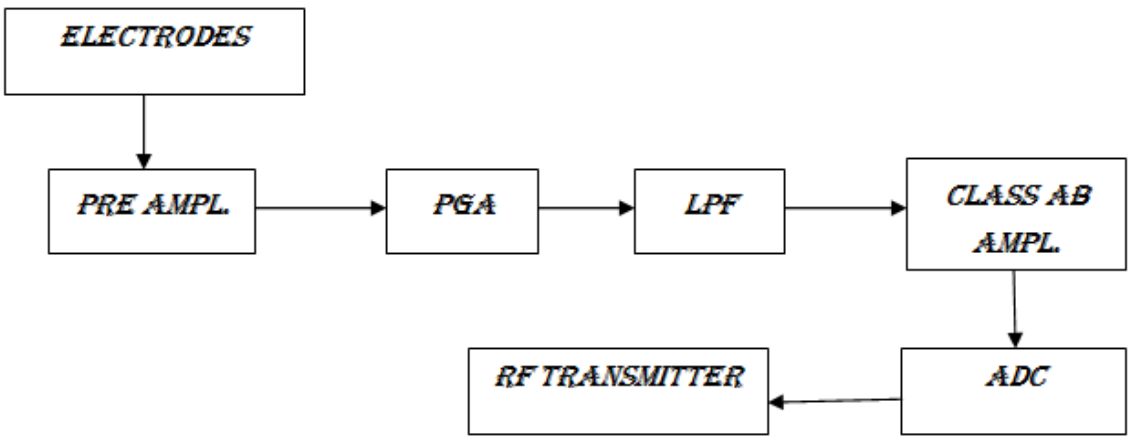

Fig.1: Block diagram of WBAN front end system

EXISTING WORK IN LITERATURE AND MODIFICATION MADE

The low-noise bio-signal amplifier presented in the literature contains a pre-amplifier, programmable gain amplifier (PGA), low pass filter (LPF) and class AB amplifier. The performance of the preamplifier is crucial which determines the signal quality and noise level. By adopting a low pass filter at the output node, high frequency ripples from the chopper modulation could be eliminated. A programmable gain amplifier and a class AB amplifier are employed to increase the gain of the system and enhance the ability to drive the load. The implementation is done in 0.18 µm CMOS technology, however considering the advantages of scaling such as; reduction in channel length increases the drive current of the device, increases the switching speed to a great extent, the same circuit is implemented using 45 nm CMOS process in this work.

.AMPLIFIER DESIGN

In this work a high gain and low-power CMOS based amplifier is presented. The main characteristics of the proposed amplifier such as gain, power consumption, CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio) and Delay are calculated and tabulated. The figure below gives the overall block diagram of the amplifier.

The various input signals fed to this circuit are described below. As shown in figure this amplifier is a dual channel circuit therefore differential sinusoidal input is fed to both channel A and B respectively of amplitude 5 mV, an offset of 0 mV at a frequency of 100 Hz. This is because the objective of the work is to design a biomedical amplifier dedicated to WBAN nodes, however incorporating external signals into VLSI workbenches are uncommon, therefore a replica of such signal is attempted to be utilized.

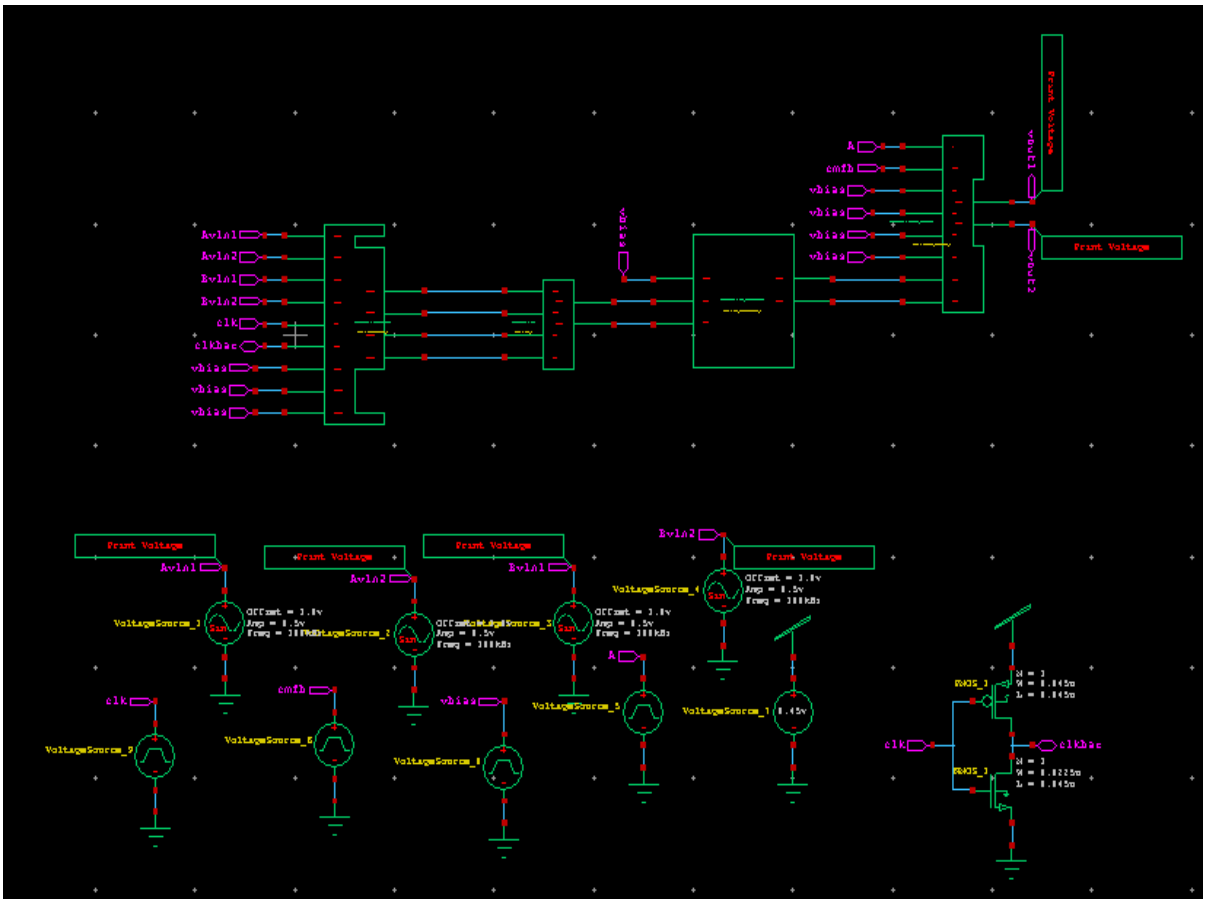

Fig. 2: Schematic of CMOS amplifier

The supply V_{dd} is a DC source of potential 0.45 V thus evaluating the circuit's performance at such a low supply voltage. Further the clock signal employed is a pulse signal of duration 50 ns, width 25 ns, amplitude of 1.0 V, raise and fall time of 5 ns. The bias potential is again a pulse signal of period 100 ns, width 45 ns, amplitude 1.0 V.

DESIGN AND SIMULATION OF PREAMPLIFIER

The proposed pre-amplifier with two parallel channels (A and B) is shown in the figure below. The dual-channel three-input current-reuse OTA is used to enhance the equivalent transconductance while CH1~CH8 denotes the chopping switches, and A1~A4 shows the voltage buffers. Moreover, the feed forward/feedback network includes the following namely feed-forward capacitors, feedback capacitors, feedback pseudo-resistors and a DC offset cancellation loop. At first the differential input signals are modulated to a higher bandwidth by the chopper switch CH2 prior to being amplified by OTA, and then demodulated back to the baseband frequency by the chopping switch CH4, while the low-frequency noise is only modulated once by CH4, therefore separating the signal spectrum from the noise spectrum. The modulated noise is eliminated by following low pass filter. Controlled by the CH1, the voltage buffer is intended to charge the feed forward capacitor of OTA directly to increase the input impedance before the chopping modulation. Both Channel A and Channel B use the same structure.

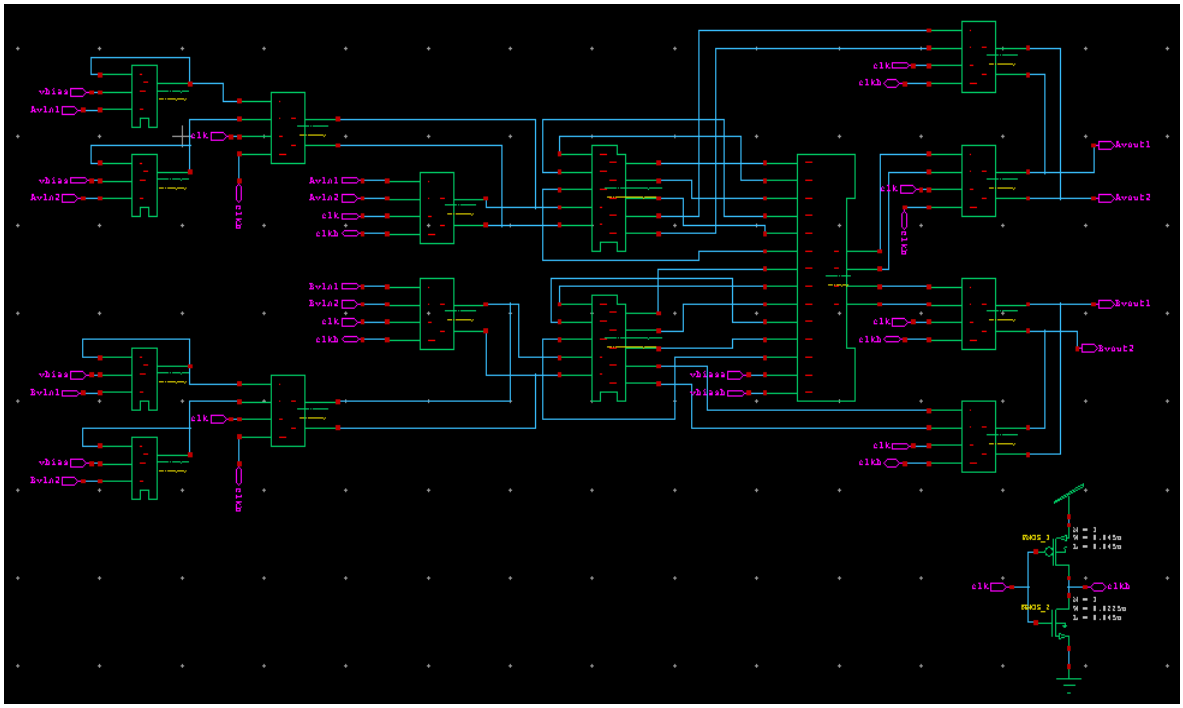

Fig. 3: CMOS Pre Amplifier schematic

VOLTAGE BUFFER

A voltage follower could also be called as a unity-gain amplifier, a buffer amplifier or an isolation amplifier. It is an op-amp circuit which has a voltage gain of 1, which means the op amp does not provide any amplification to the signal. These circuits are generally used to isolate stages from one another. Its attribute is to have a high input impedance and a low output impedance. Therefore the circuit that supplies the input signal need not provide large current but the output of the voltage follower can supply significantly more current to the next stage.

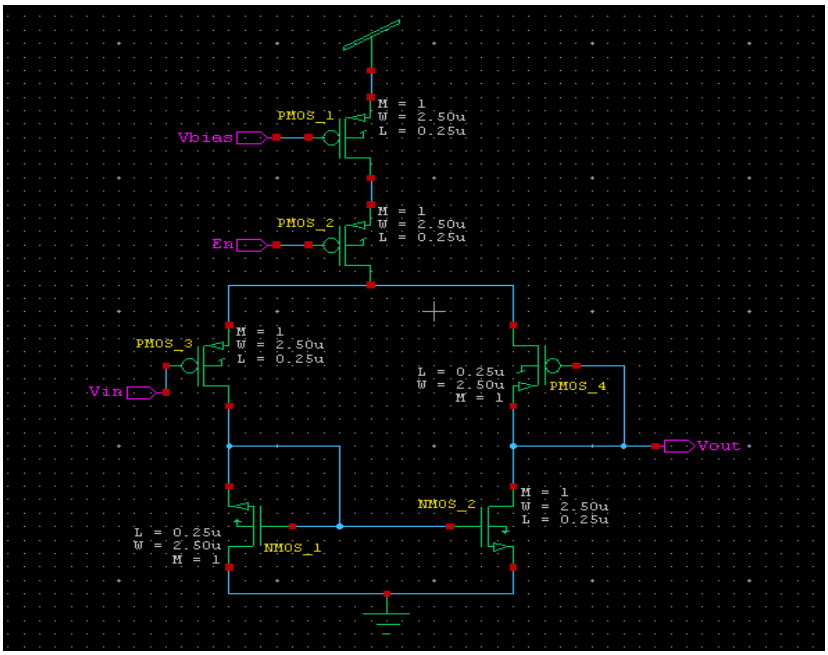

Fig. 4: CMOS voltage buffer circuit

CHOPPER SWITCH

For sensor applications, the bandwidth of interest is generally a few Hertz. In this bandwidth, offset and 1/f noise are the dominant sources of error. Chopping technique is an efficient approach to decrease the 1/f noise and low-frequency offset of CMOS amplifiers; thus, in this work, a proposed chopper circuit to tackle these problems is presented. The chopper circuit is designed using complementary CMOS switches that are optimized to achieve symmetric linear resistance in the range of input signal.

Chopping is a kind of modulation technique that reduces the effects of op-amp imperfections including DC offset voltage and noise. The chopper circuit is driven by clock at frequency f_{ch} therefore the signal is modulated at f_{ch}. Following this, the modulated signal is amplified together with its own input offset. The next chopper circuit demodulates the amplified input signal back to DC, and at the same time modulates the offset to the odd harmonics of f_{ch}, which would be filtered by the low-pass filter (LPF) stage. The result is, we get an amplified input signal without offset. The pink noise called as the reciprocal frequency noise or the 1/f noise is modulated and filtered out along with offset. Thus the chopping action is in the frequency domain. The circuit of used in this work are shown below.

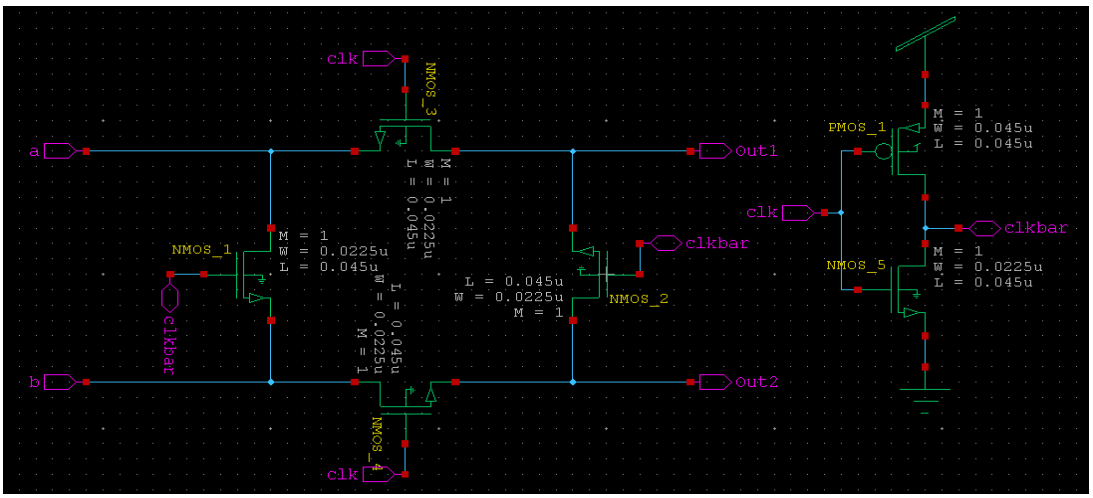

Fig. 5: CMOS chopper switch circuit

FEED FORWARD – FEEDBACK NETWORK

A feedforward network is employed as a compensation technique where a buffer is used to break the bidirectional path through the compensation capacitor. The usage of a current mirror circuit along with the feedforward technique produces a lower non dominant pole than in a folded cascode amplifier.

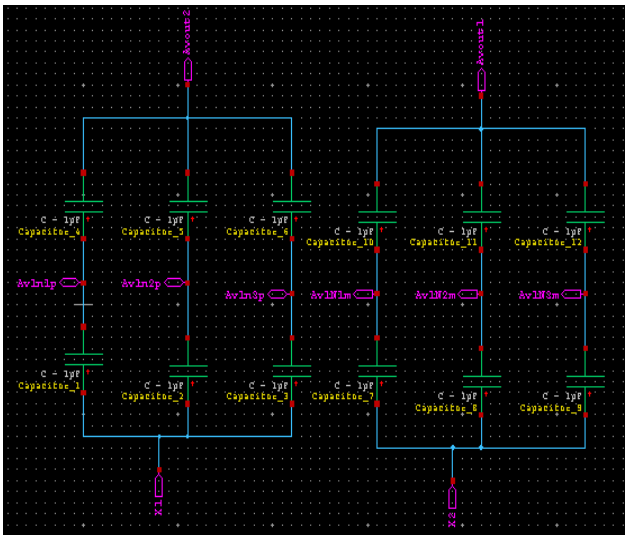

Fig. 6: CMOS feed forward/feedback circuit

The Feed-forward/feedback network consists of four components namely, the feed-forward capacitors, feedback capacitors, feedback pseudo-resistors and a DC offset cancellation loop. It is used for coupling the signals, stabilizing the DC operating points, determining the gain of the amplifier and eliminating the DC offset voltage from the input. Feed-forward capacitors C1~C6 couple the input signals and determine the AC gain. The impedance of pseudo-resistors is of the order of GΩ, which constitute the DC feedback loop to determine appropriate DC operation points of three input differential pairs. Feed-forward capacitors are used to improve the input impedance.

DUAL CHANNEL THREE INPUT CURRENT REUSE OTA

The next task ahead is elimination of the thermal noise. Increasing gm can effectively reduce thermal noise, but power consumption must be strictly limited in the low-power applications. So high current transconductance efficiency (g_m/I_D) will be critical for the low-noise and low-power design for which the transistor must be biased in the subthreshold region. Though the CMOS biased in this region has high current transconductance efficiency, it is limited for single transistor. Therefore, the current-reuse technique is used for further enhancement of g_m/I_D. The Current Reuse structure used here is a non folded cascode structure having 2 separate gain stages with a common bias current. A Cascode is nothing but a two transistor stack used to obtain high gain and high output impedances consisting of a common source configuration followed by a common gate stage. This reduces the power consumption but the linearity of the signal gets disturbed, which could be compensated by the Gm-C filter.

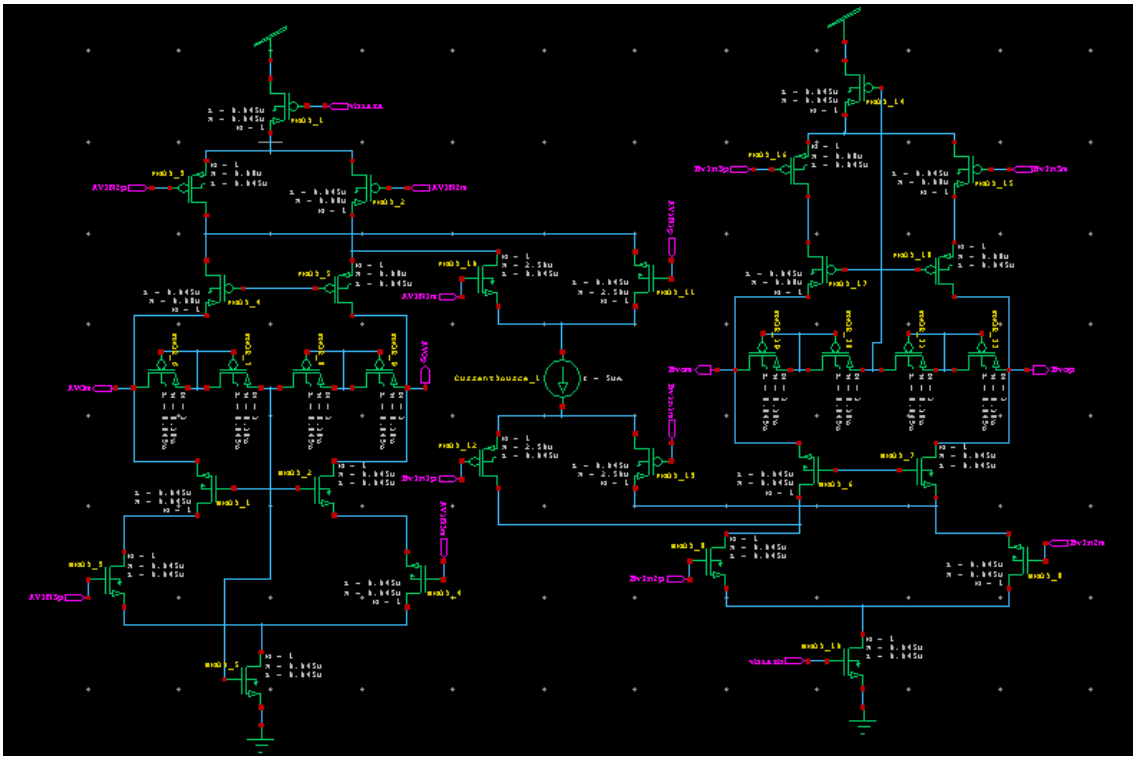

Fig.7: Operational Transconductance Amplifier circuit

DESIGN AND SIMULATION OF PROGRAMMABLE GAIN AMPLIFIER

Since the biomedical signal amplitudes change in a wide range, a programmable gain amplifier is adopted to get the expected signals amplitudes. It employs a capacitive-coupled structure in a differential mode. The closed loop gain of amplifier is adjustable according to the values of the feedback capacitors. If the feed-forward capacitor value is 8C, then the feedback capacitor is are of values C, 2C, 4C and 8C, therefore the closed loop gain of 8/4/2/1. Each capacitor is gets connected to a MOS switch in series, and the switches are in turn controlled by a 2-4 decoder.

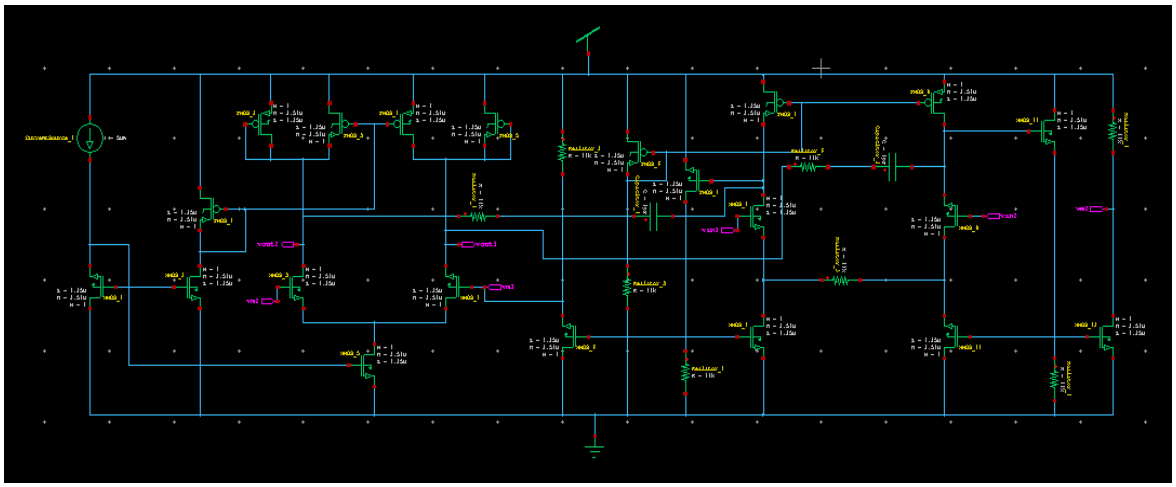

Fig.8: CMOS Programmable Gain Amplifier circuit

DESIGN AND SIMULATION OF LOW PASS Gm-C FILTER

The output of the chopper contains high frequency ripples which are caused by low frequency noise being modulated by chopper. Frequency bands of these ripples are above the chopper frequency, so they could be eliminated by the low pass filter. Since the frequency of a bio-signal is always very low, large values of capacitors and resistors are to be used to acquire cut-off frequency of about 150 Hz. Gm-C filter is an appropriate choice to reduce the chip area, which consists of basic transconductance units and capacitors. The basic transconductance unit is achieved by a low transconductance – high input

impedance amplifier. Considering the trade-off between area and power consumption, a second-order Gm-C low pass filter is chosen.

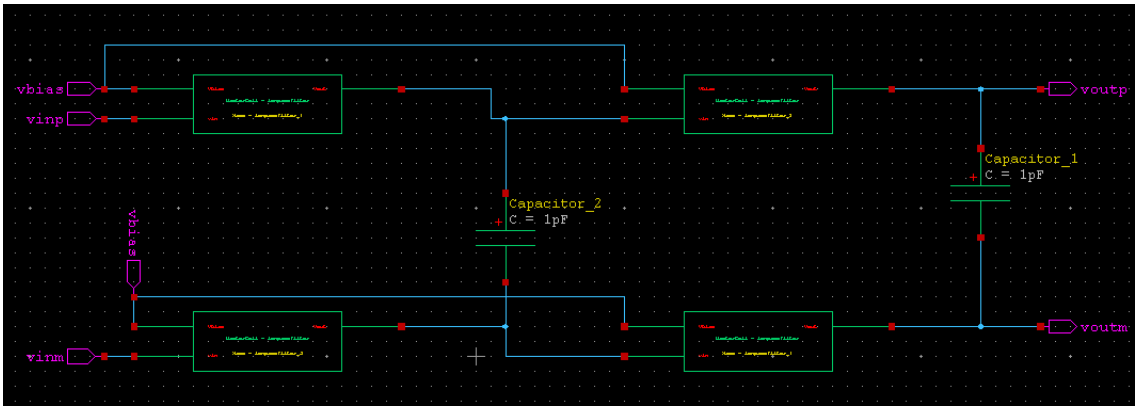

Fig.9: CMOS Low pass Gm-C filter schematic

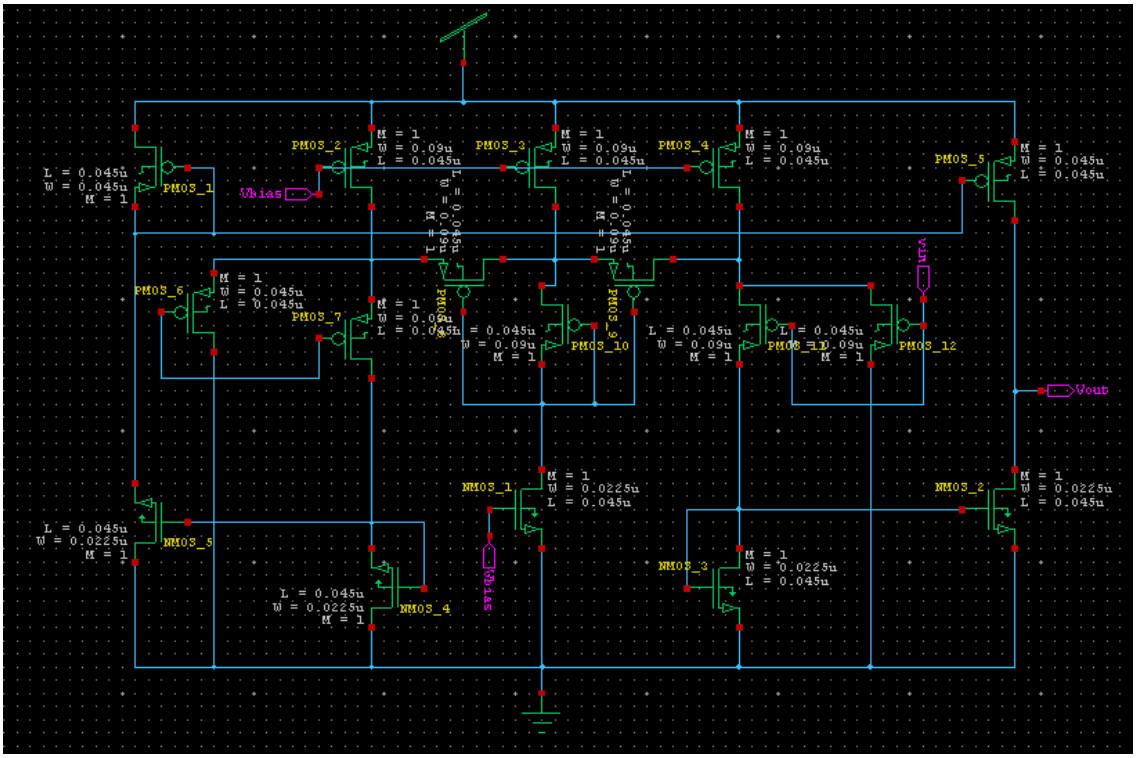

Fig.10: Transconductance block

DESIGN AND SIMULATION OF CLASS AB AMPLIFIER

As mentioned earlier, the biomedical signals are extremely weak, the closed loop gain provided by the pre-amplifier – PGA combination still remains insufficient for the amplification of the low amplitude signals. Moreover, the programmable-gain amplifier has a poor driving capability. Therefore, the class AB amplifier is employed to improve the gain and driving capability. The class AB amplifier can be divided into input stage, middle stage and output stage. The input stage and output stages are differential stages while the middle stage does partial gain contribution.

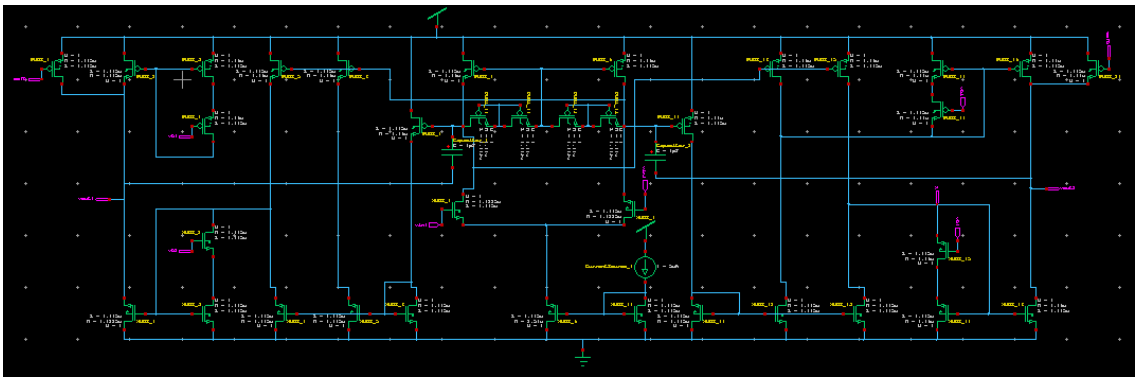

Fig.11: CMOS Class AB amplifier circuit

RESULTS AND DISCUSSION

In this work, a dual-channel low-noise amplifier based on the wireless body area network is designed and implemented in a 0.045 µm standard CMOS process. the performance parameters are evaluated and tabulated below. Also the input and output waveforms are shown. The amplifier is quite suitable for biomedical signal acquisition systems and other related applications.

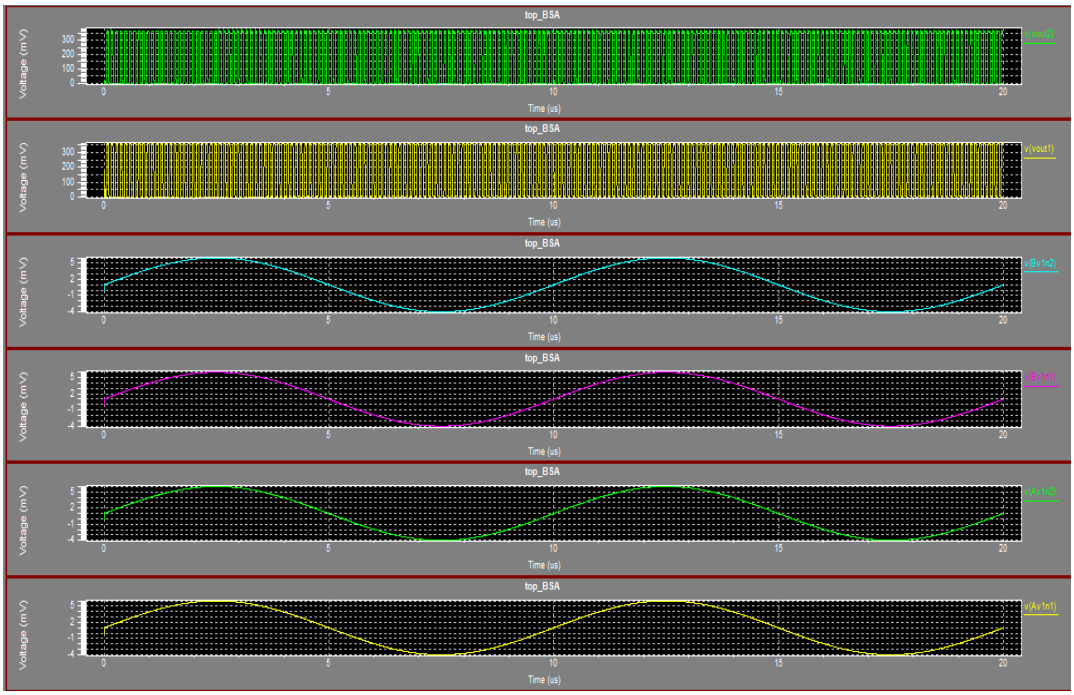

Fig.12: Overall amplifier input-output waveform

The tables shown below gives the device count and the results in terms of the performance parameters analysed.

Table1: Number of Sources, Active and Passive devices used to construct the entire CMOS amplifier circuit

DEVICE	COUNT
Active devices	233
Passive elements	38
Independent sources	12
Total devices	283

Table 2: Performance Analysis of CMOS amplifier

PARAMETER	SIMULATED RESULTS
TRANSISTOR	CMOS
TECHNOLOGY	45 nm
SUPPLY VOLTAGE	0.45 V
GAIN	37.07 dB
CMRR	114.80 dB
PSRR	89.3 dB
MAXIMUM POWER CONSUMED	17.3 µW
AVERAGE POWER CONSUMPTION	6.7 µW
TRANSIENT DELAY	47.8 ns

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