OPTIMIZATION OF 2-4, 4-16 DECODERS AND 2-BIT COMPARATOR

KUMBAM ESHWAR REDDY[1]
eshwarreddy4mail@gmail.com

DURGAM KHASIM HUSSAIN[2]
khasim427@gmail.com

[1]Assistant professor, M. Tech, Princeton College OF Engineering &Technology/ECE Department, Ranga Reddy, India
[2]Assistant professor, M. Tech, Princeton College OF Engineering &Technology /ECE Department, Ranga Reddy, India

Abstract: A mixed-logic design method for line decoders, combining transmission gate logic, pass Transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoders: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power- delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. four new 4-16 decoders are designed, by using mixed-logic 2-4 pre decoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. The proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases .comparator circuit is designed using mixed logic line decoders.

Index Terms: Line decoder, mixed-logic, power-delay optimization.

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits [1]. It consist of complementary nMOS pull down and Pmos pull up networks and present Good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced [3-6], aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. Mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM) multiplexing structures, implementation of Boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including [7-9].

II. OVERVIEW OF LINE DECODER CIRCUITS

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the m = 2n minterms of n input variables.

A. 2-4 Line Decoder:

A 2-4 line decoder generates the 4 minterms D0-3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination; one of the 4 outputs is selected and set to 1 while the others are set to 0. An inverting 2-4

decoder generates the complementary minterms I0-3, thus the selected output is set to 0 and the rest are set to 1, as shown in Table I.

TABLE I
TRUTH TABLE OF 2-4 DECODER & INV 2-4 DECODERS

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, Therefore implementing logic functions with higher efficiency. A 2-4 decoder can be implemented with 20 transistors using 2 inverters and 4 NOR gates, as shown in Fig.1 (a). The corresponding inverting decoder can also be implemented With 20 transistors using 2 inverters and 4 NAND gates, as shown in Fig.1 (b).

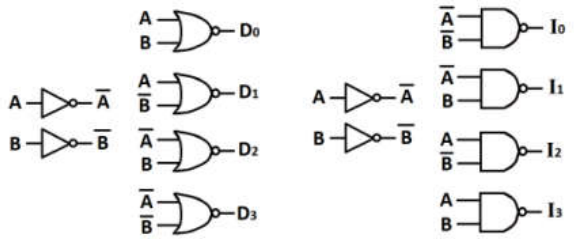


Fig. 1: 20-transistor 2-4 line decoders implemented with CMOS logic: (a) Non-inverting NOR-based decoder, (b) Inverting NAND-based decoder.

B. 4-16 Line Decoder with 2-4 Predecoders:

A 4-16 line decoder generates the 16 minterm D0-15 of 4 input variables A, B, C and D, and an inverting 4-16 line decoder generates the complementary Minterms I0-15. It require 16 4-input NOR and NAND gates. A more efficient design can be obtained using a pre decoding technique, according to which blocks of n address bits can be predecoded into 1-of-2^n predecoded lines that serve as inputs to the final stage decoder [1]. A 4-16 decoder can be implemented with two 2-4 inverting decoders and 16 2-input NOR gates (Fig. 2(a)) and an inverting one can be Implemented with two 2-4 decoders and 16 2-input NAND gates (Fig. 2(b)). In CMOS logic, these designs require 8 inverters and 24 4-input gates, yielding a total of 104 transistors each.

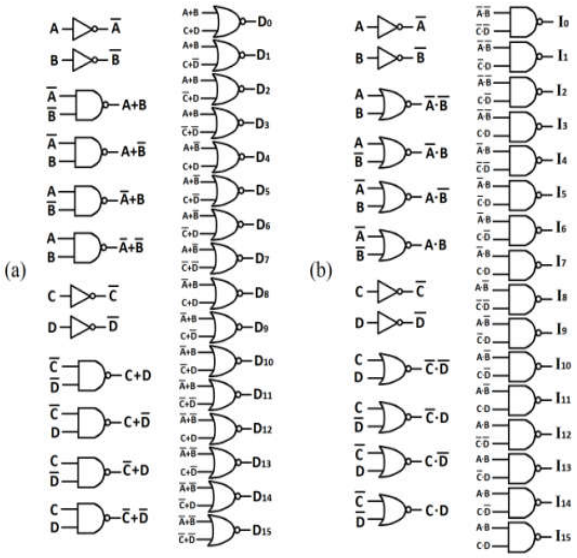


Fig.2: 104-transistor 4-16 line decoders implemented with cmos logic and predecoding.(a) Non-inverting decoder implemented with two 2-4 inverting predecoders and a NOR-based postdecoder, (b) Inverting decoder implemented with two 2-4 non-inverting predecoders and a NAND based post- decoder.

III. NEW MIXED-LOGIC DESIGNS

In combinational logic, transmission gates have mostly been used in XOR-based circuits such as full adders and as the basic switch element in multiplexers. However, we consider their use in the implementation of AND/OR logic, as demonstrated in [5], which can be efficiently applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig.3(a) and 3(b), respectively.

They are full-swinging, but not restoring for all input combinations. Regarding pass-transistor logic, there are two main circuit styles: those that use nMOS only pass-transistor circuits, like CPL [3] and those that use both nMOS and pMOS pass- transistors, like DPL [4] and DVL [6].

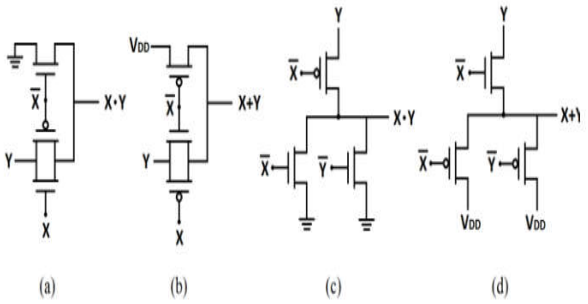


Fig. 3: The 3-transistor AND/OR gates considered in this work (a) TGL AND gate, (b) TGL OR gate, (c) DVL AND gate, (d) DVL OR gate.

The style we consider in this work is DVL, which offers an improvement on DPL, preserving its full swing operation with reduced transistor count[10]. The 2 input DVL AND/OR gates are shown in Fig. 3(c) and 3(d), respectively. Similar to the TGL gates, they are full-swinging but non-restoring. Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR gates. Decoders are high fan Out circuits, where few inverters can be used by Multiple gates, thus using the TGL/DVL gates can result to reduced transistor count.

Transmission gates have Asymmetric nature, i.e the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs X and Y. In TGL gates, input X Controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate Terminal and propagates through a pass transistor to the output. X and Y inputs as the Control signal and the propagate signal of the gate, respectively. This asymmetric feature gives a designer the flexibility to perform signal arrangement, ie .,choosing which input is used as control and which as propagate signal in each gate.

Having a Complementary input as propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A'B) or implication (A'+B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A+B) function, either choice is equally efficient. Finally, when implementing the NAND (A'+B') or NOR (A'B') function, either choice results to a complementary propagate signal, perforce.

A. The 14-transistor 2-4 Low-Power Topology:

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely A and B, we eliminate the B inverter from the circuit. The D0 minterm (A'B') is implemented with a DVL gate, where A is used as propagate signal. The D1 minterm (A'B) is implemented with a TGL gate, where B is used as propagate signal.

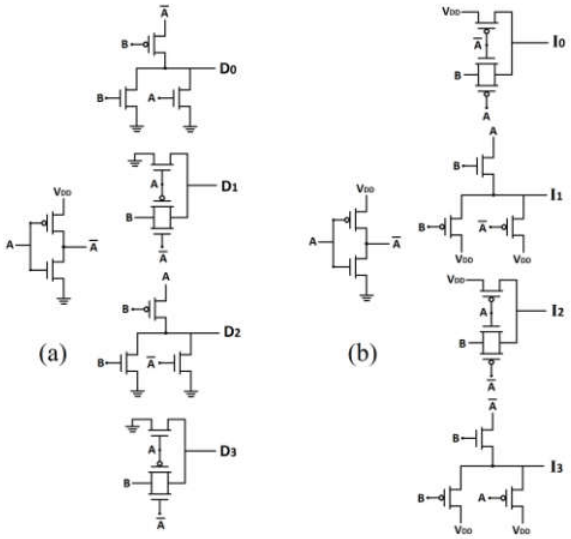


Fig. 4: New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI.

The D2 minterm (AB') is implemented with a DVL gate, where A is used as propagate signal. Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as propagate signal. These particular choices completely avert the use of the complementary B signal, therefore the B inverter can be eliminated from the circuit resulting in a 14-transistor topology (9 nMOS, 5pMOS). Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS, 9 pMOS), as well: I0, I2 are implemented with TGL(using B as a propagate signal) and I1, I3 are

implemented with DVL (using A as propagate signal). The B inverter can once again be elided.

The inverter elimination reduces transistor count, logical effort and overall switching activity of the circuits, thereby minimizing power dissipation. 14 is the minimum number of transistors required to realize a full swinging 2-4 line decoder with static (non clocked) logic. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stands f or 'low power' and 'I' for 'inverting'. Their schematics are shown in Fig. 4(a) and Fig. 4(b),respectively.

B. The 15-transistor 2-4 High-Performance Topology:

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, realizing D0 and I3 can be implemented more efficiently by using standard CMOS gates, since there is no need for complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology.

The new designs resulting from this modification mix 3 different types of logic into the same circuit and present a significant improvement in delay while only slightly increasing power dissipation. They are named '2-4HP' (9nMOS, 6 pMOS) and '2-4HPI' (6 nMOS, 9 pMOS), where 'HP' stands for 'high performance' and 'I' for 'inverting'. The reasoning behind the 'HP' designation is that these decoders present both low power and low delay characteristics, therefore achieving an overall good performance. The 2-4HP and 2-4HPI schematics are shown in Fig. 5(a) and Fig. 5(b), respectively.

C. Integration in 4-16 Line Decoders:

Circuits based on pass transistor logic Can realize logic functions with fewer transistors and improved performance compared to static CMOS. However, cascading several non-restoring circuits causes a rapid degradation in performance. A mixed topology approach, i.e., alternating restoring and no restoring Levels of logic, can potentially deliver Optimum results, combining the positive characteristics of both.

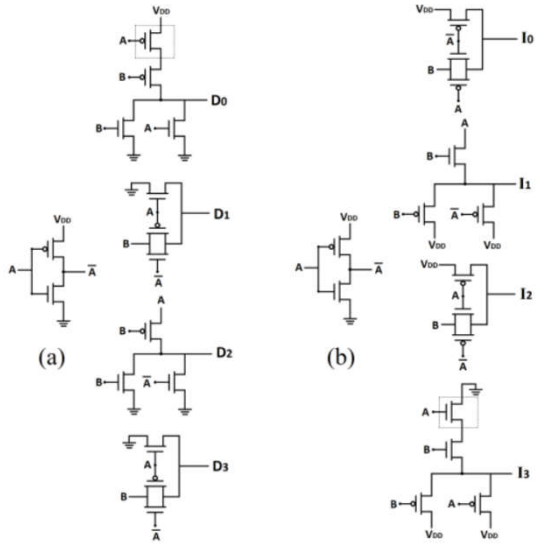


Fig. 5: New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI. Deliver optimum results, combining the positive characteristics of both.

We implemented four 4-16 decoders by using the four new 2-4 as Predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are: 4-16LP (Fig. 6(a)), which combines two 2- 4LPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 6(b)),Which combines two 2-4LP predecoders with a NAND based post-decoder,4-16HP (Fig.6(c))which combines two 2-4HPI Predecoders with a NOR based post-decoder and, finally,4-16HPI (Fig. 6(d)), which combines two 2-4HP predecoders with a NAND based predecoder.

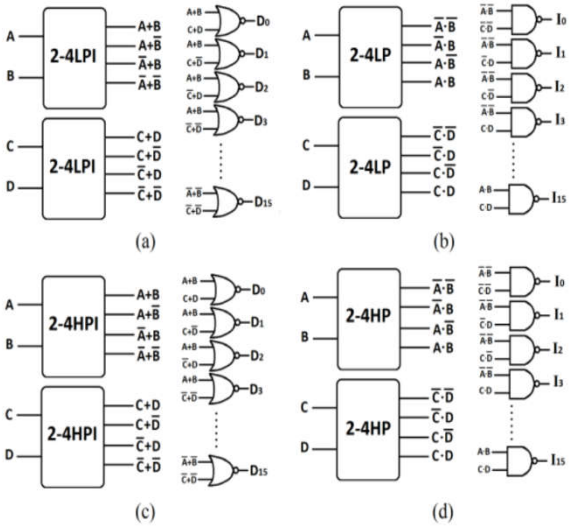


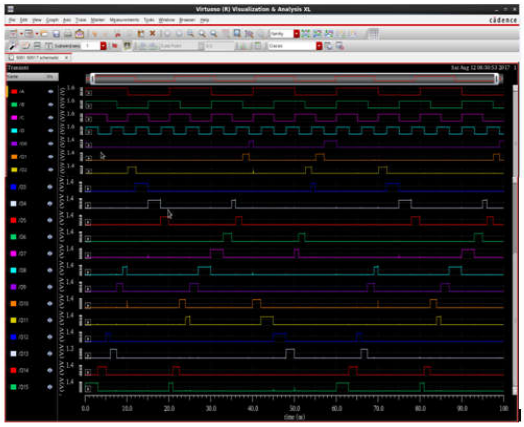
Fig. 6: New 4-16 line decoders: (a) 4-16LP, (b) 4-16LPI, (c) 4-16HP, (d) 4- 16HPI.

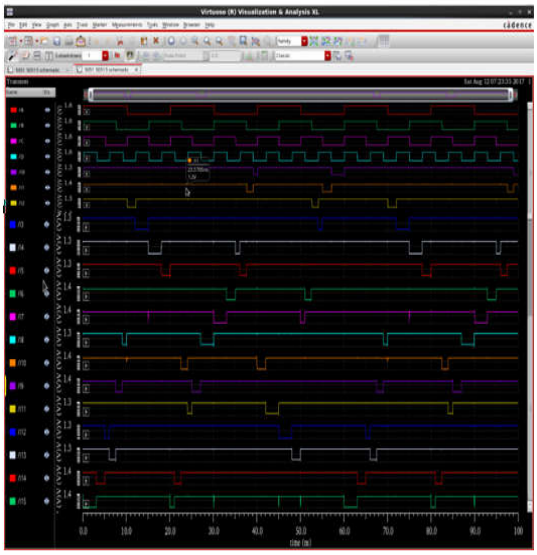
The 'LP' topologies have a total of 92 transistors, while the 'HP' ones have 94, as opposed to the 104 transistors required by the pure cmos implementation.

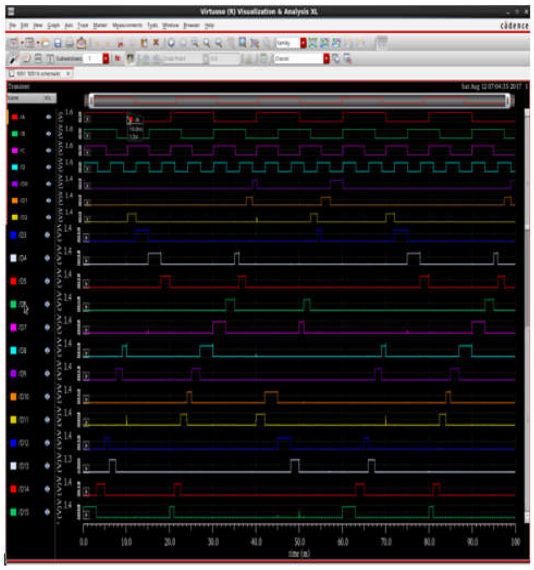
IV.SIMULATION RESULTS

All the simulations are performed on cadence tools. The main focus of this work is to meet all challenges faces in designing of Decoder circuit using mixed logic. This work develops a mixed-logic design methodology for line decoders combining gates of different logic to the same circuit in an effort to obtain improved performance compared to single style design. All the examined circuits are implemented using a 45nm technology model for low power applications.

Simulations are performed on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional cmos. The simulation results are shown below figures.







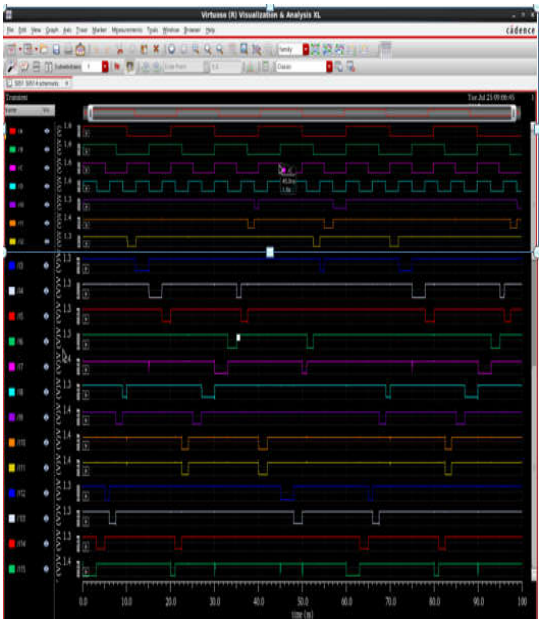


Fig.7: Input/output waveforms of proposed 4-16 decoders for all input transitions: (a) 4-16LP, (b) 4-16LPI, (c) 4-16HP, (d) 4-16HPI.

V. EXTENSION WORK

Designing of 2-bit Comparator Using mixed logic line Decoder:

It generates 3 minterms A<B, A=B, A>B of 2 input variables A and B. Its logic operation is summarized in Table II. Here Comparison done between two Variables. Whenever A<B, then the output is 1, others are set to 0.

A. DESIGN OF 2 BIT COMPARATOR:

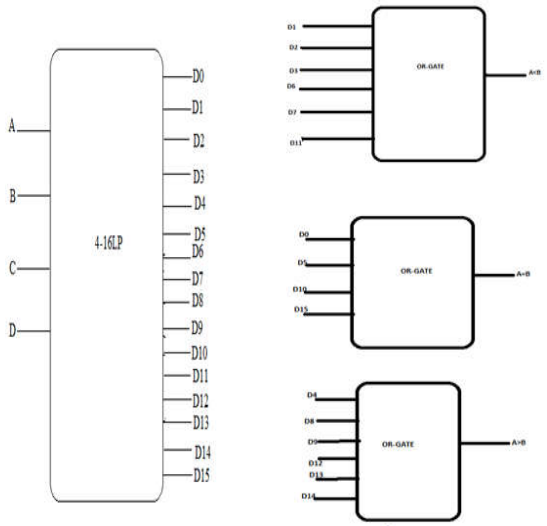


Fig.8: Design of 2 bit comparator using 4-16 decoders

Circuits based on pass transistor logic Can realize logic functions with fewer transistors and improved performance compared to static CMOS. However, cascading several non-restoring circuits causes a rapid degradation in performance. A mixed topology approach, ie., alternating restoring and no restoring Levels of logic, can potentially deliver Optimum results, combining the positive characteristics of both. Adopting this design methodology, and with respect to the theory presented on section 2 bit comparator is designed by using pass transistors instead of using cmos logic, which combines two 2-4LPI predecoders with a nor-based post decoder and with a or gates. The 2-bit comparator schematic is shown in Fig.8.

TABLE II

2-BIT COMPARATOR TRUTH TABLE

INPUTS				OUTPUTS		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Fig.9: Input/output waveforms of 2-bit Comparator for all input transitions: (a) comparator design using cmos logic (b) comparator design using transistor logic.

TABLE III

Comparison of 2-4, 4-16 and 2-bit comparator

	DELAY(ns)	AVERAGE POWER FROM CALCULATOR	HIGH PEAK POWER(μW)	LOW PEAK POWER(μW)	AVERAGE(μW)
2-4LP	10	426.9E	402.63	213.03	307.83
2-4LPI	10.03	498.7E	446.25	233.33	339.79
4-16LP	37.56	232.8E	904.94	213.19	559.07
4-16LPI	37.54	189.8E	981.945	209.485	595.71
2-4LP	10.01	359.3E	496.02	76.109	286.02
2-4LPI	10.39	311.9E	484.987	102.841	293.91
4-16LP	37.53	221.2E	803.576	209.482	506.52
4-16LPI	33.03E	147.5E	1.218(mw)	133.17	670.00
2-4HP	10.02	304.5E	418.876	92.139	255.50
2-4HPI	10.08	304.5E	451.357	112.749	281.55
4-16HP	30.03	217.0E	792.468	211.552	502.01
4-16HPI	30.56	135.2E	1.064(mw)	151.411	650.07
2 BIT COMPARATOR USING CMOS LOGIC	10.09	439.3E	837.603	218.243	527.97
2 BIT COMPARATOR USING TRANSISTOR LOGIC	10.07	327.8E	841.522	209.764	525.64

VI. CONCLUSIONS

Efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2-4 line decoder topologies, namely 2-4LP, 2-4LPI, 2-4HP and 2- 4HPI, which offer reduced transistor count (therefore potentially smaller layout area) and improved power-delay performance in relation to conventional CMOS decoders. Four new 4-16 line decoder topologies were presented, namely 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits and combining them with post decoders implemented in static CMOS logic. These designs combine the improved performance characteristics of pass transistor logic with the restoring capability of static CMOS.The 2-4LP and 4-16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2-4LPI, 2-4HP and 2-4HPI, as well as the corresponding 4-16 topologies (4-16LP, 4-16HPI, 4-16HP), proved to be viable and all-around efficient designs , thus they can effectively be used as building blocks in the design of larger decoders, multiplexers and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI design as well.

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DCST BASED REGION OF INTEREST EXTRACTION FROM REMOTE SENSING IMAGES: A REVIEW

J. MAHESWARREDDY[1], Dr. S. A. K.JILANI[2]

[1]Research Scholar, Department of ECE, Rayalaseema University, Kurnool, A.P, INDIA.

[2]Professor, Department of ECE, Madanapalle Institute of Technology & Science, INDIA.

[1]Jmaheswarreddy@gmail.com, [2]jilani_consult@yahoo.com

ABSTRACT

Saliency object detection is considered as the pre processing technique to study the features of the specific area in the satellite images.Diversity in surroundings texture and objective clutter also adds up to the complicationin the problem of localizing saliency regions in satellite images. Extraction of a feature of an image is very difficult due to having to find the appropriate image segmentation techniques and combine diverse methods to detect the Region of Interest (ROI) most efficiently. In this paper we address the problem of the region extraction in various methods and suggested a novel technique based on the discretecosine stock well transform (DCST) for the generation of saliency map and for segmentation of the required area we suggest inhomogenity active contour model in order to provide high degree of results. The results in the proposed approach may increase the detection capability of the target region.

KEYWORDS: Region of interest, Inhomogenity active contour model, DCST.

1. INTRODUCTION

As remote sensing technology is increasing rapidly in various applications there is need to extract the saliency objects for further processing of images. The saliency object detection needs to detect the image with perfect edges and of high quality. Saliency detection of remote sensing images has various applications in the fields of image segmentation, image restoration and image compression etc. It is not an easy task to extract the saliency regions in the remote sensing images with our naked eye and if possible it is not accurate and in some images it turns into problematic. So, we develop an automatic detecting algorithm based on some features and certain conditions.

Automatic detection of military targets such as oil tanks, aircrafts, artillery, etc. in high resolution satellite imagery has great significance in military applications. With the rapid development of satellite imaging and geographic information systems, a large amount of high resolution images can be acquired effortlessly from Google Earth. The non-hyper spectral image data has been used in many civil and military applications. Various techniques and features have been proposed so far for automatic target detection in satellite imagery.

Target detection is an important aspect in many defence applications. A target generally means an object or a region of interest and importance, such as urban areas, roads, railway tracks, shipyards, etc. The task in target detection is to locate and label a particular target among non-

targets in a scene. This task has been extensively studied in computer vision where the main steps are classification of the scene into regions of interest, looking for potential structures, making geometric analysis of these structures and finally confirming the presence or absence of a target using proper knowledge base. But, its application in remote sensing had been limited because of the inadequate ground resolution of the image available in the past. However, with resolution better than 30-40 m provided by the current remote sensing technology, it is now possible to a great extent to identify even smaller targets, like bridges, runways and buildings. Consequently, the scope of application of remotely-sensed imagery in defence has considerably widened.

2. SALIENCY OBJECT DETECTION TECHNIQUES IN SATELLITE IMAGES:

Wang Xiangyangt Hu Fengli Yang Hongying [2006] proposed a method based on the multiple features of the satellite image. In this method the area of interest is segmented based on the K-means clustering algorithm and gather color features from dominant color and its percentage and acquire shape feature from the pixel distribution and based on the these features and segmented region the saliency object is extracted [1]-[3]. But this method is applicable only for the simple background regions.

Hui-Zhong Chen, Ning Jing, Jun Wang, Yong-Guang Chen, and Luo Chen [2014] inferred that the saliency objects can be detected based on the SURF features of the image. In this work, two regions of the image are considered. They are highlight regions and the shadow regions for whichthe speed up robust features are calculated. A feature vector is generated for the region of interest, depending on this vector SVM classifier classifies the saliency regions are extracted from false detected and inconspious ones [4]-[6]. But the satellite image must contain both highlight and shadow regions clearly.

Libao Zhang, Kaina Yang, and Hao Li[2014] developed a fusion technique with two inputs obtained from the intensity saliency and orientation saliency. The intensity saliency is obtained from the Multiscale spectrum residuals method and orientation saliency is obtained from the interpolating biorthogonal integer wavelet transform. Then the orientation saliency map is thresholded and filtered. Then these two maps are weighted across by using Multiscale fusion at different scales to extract the saliency region [7]-[9]. This method considers only the bottom-up information which results to faults result.

Ashu Sharma, J.K. Ghosh [2015] extracts segments from the segmented image under the basis of the threshold value. If the saliency values of the clusters are superior or identical to the threshold value then they are segmented into the saliency region. Based on this process the saliency and non saliency regions are considered as foreground and background respectively. By segmenting them the saliency regions are extracted [10]-[12]. This method consists of only the saliency model for segmentation which results to the loss in extraction of edges accurately.

Libao Zhang, Xinran Lv, Jie Chen and Lan Zhang [2016] extract the saliency objects by following the three stages.In first stage the salient feature maps are constructed by calculating the spectrum information and histograms of multi spectral images.Next, based on the K-means clustering the salient features are selected by converting into the CIELAB color space and final saliency maps are generated fusing the information salient feature maps with common salient maps. Finally the saliency region is segmented by extracting ROI from the final saliency map [13]-[15]. But in this

process the k-means clustering technique require selecting of k clusters for features generation which is a difficult task because the results are depend on this selection.

Samik Banerjee, Nitin Gupta, Sukhendu Das, Pinaki Roy Chowdhury and L K Sinha [2016] used an unsupervised saliency detection method by preprocessing the images for denoising and contrast enhancement. This technique is helpful to detect the potential regions of interest which reduces the search space. These regions are additionally processed by with some morphological operations to get probable regions of saliency objects and lastly a conical pyramid is constructed for template representation of the target samples [16]-[18]. But this technique is not applicable under foggy or cloudy conditions.

Warinthorn Kiadtikornthaweeyot, Adrian R.L. Tatnall [2016] extracted the saliency region by considering histogram and morphological operations. In this process, the segmentation is made based on the histogram equalization and ROI is estimated based on the masking operations obtained from the morphological operations. In this method the regions of forest, roads and buildings are detected individually [19]-[21]. But in this process histogram classification is done manually leads to inaccurate results.

Libao Zhang n, Jie Chen, Bingchang Qiu [2016] worked on the high resolution areas which contains fine details like edges, structure and texture. To preserve the fine details we considered a map based on the normal directional lifting wavelet transform. Next, we judge the spectral saliency map by acquiring the self information offered in the spectrum. Then the final saliency map is obtained by fusing these two maps [22]-[24].The region of interest is segmented from the absolute saliency map based on the segmentation techniques.It should be noted that the principle followed for selecting the optimal transform direction is critical in ND-LWT.

Danpei Zhao, Yuanyuan Ma, Zhiguo Jiang, and Zhenwei Shi [2017] consider both bottom-up and top-down features based on the target attribute to generate the saliency map by fusing them. In this process Latent Dirichlet allocation based learning stop criterion is introduced at each level to judge the state of saliency detection. A back level propagation mechanism is employed to reinforce the target levels and for detection of target it uses hierarchical reinforcement learning algorithm [25]-[27]. But this method is adaptable to high resolution satellite images.

Hui Wu, Hui Zhang, Jinfang Zhang, Fanjiang Xu [2015] proposed a new target detection structure based on the convolutional neural networks to automatically learn the presentations from the massive image data in order to provide more computational efficiency. CNN can learn rich features and based on these features the Edge boxes can generate smaller set of object proposals based on the edges [28]-[30]. If the edges of the objects are not perfect then the detection is difficult.

3. CONCLUSION

In this paper by reviewing all the techniques used for detecting the saliency object in satellite images reveals that the researches focus mainly on the histogram classification, wavelet transforms and neural networks for saliency map estimation. These techniques show best results only in some typical conditions. However, histogram classification and neural networks depend on the edges of the target objectswhich cannot be acquired accurately. Hence we suggested a novel technique based on the discrete cosine stock well transform for

classification and in homogeneity contour model foe segmenting the saliency object in satellite images with accurate results in all conditions and with lower computational complexity.

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