A NOVEL APPROACH TO SOLVE POWER AND VOLTAGE UNBALANCE PROBLEMS IN CASCADED MULTILEVEL H-BRIDGE INVERTERS BASED SOLID STATE TRANSFORMER CONNECTED TO MICROGRID BY USING FUZZY LOGIC CONTROLLER

KALLEM NARSING REDDY(M.Tech)

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

email: kallem.narsingreddy@gmail.com

ABSTRACT-A new application of power and voltage balance control schemes for cascaded H-Bridge Multilevel Inverter (CHMI)-based Solid-State Transformer (SST) topology with fuzzy controller is proposed in this paper. The SST consists of a cascaded multilevel ac/dc rectifier, dual active bridge (DAB) converters with high-frequency transformers. The solid state transformer (SST) has the features of immediate voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation and dc output. Here we are using the fuzzy controller compared to other controllers i.e. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. To reduce load on the controller and simplify modulation algorithm, a master-slave control (MSC) strategy is designed for the dual active bridge (DAB) stage. This paper presents a compensation strategy based on three-phase d-q decoupled current controller. The fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system control and improve the efficiency. The proposed control method the three-phase grid currents and dc-link voltage in each module can be simultaneously balanced. By using the simulation results we can analyze that the proposed method and also the performance of the controller and its application to microgrid SST.

Index Terms—Cascaded H-bridge Multilevel Inverter (CHMI), Solid-State Transformer (SST), dual active bridge (DAB), three-phase d-q decoupled current controller, master-slave control (MSC), Fuzzy controller, power and voltage balance.

I.INTRODUCTION

The paper proposes the utility of the 3-phase SST and its controller with the electricity waft from the disbursed renewable strength assets to the grid under unbalanced situations. The control scheme solve the power and voltage unbalanced issues of 3-segment SST along with the unbalanced of different modules (DAB+CHMI) in each section and in the end inject a simply sinusoidal balanced 3-phase contemporary into the ac grid. The FREEDM system is a new medium-voltage microgrid composed of several solid state transformers (SST), high-bandwidth digital communication, and distributed control.

As the fundamental component of innovative smart microgrid system, SST is intended to replace the conventional line frequency transformers and performs the power flow control. Conventional transformers possess many unwanted residences inclusive of bulky and power quality susceptibility.

Compared with the preceding methods the proposed techniques have the following capabilities:

(1) The paper investigates the application of the SST converter in FREEDM system and its control with power flowing from the allotted renewable power resources to the grid under unbalanced conditions.

(2) The DAB stage is used to enhance the low enter voltage of renewable strength resources to medium voltage level of the ac grid distribution. Therefore, more than one renewable strength resources may be utilized in parallel to increase the power rating of the system.

(3) The dc-hyperlink voltage glide is controlled by unbiased controllers.

(4) It simplifies the controller of the DAB degrees the usage of master-slave method and affords excessive frequency galvanic isolation between the input and output.

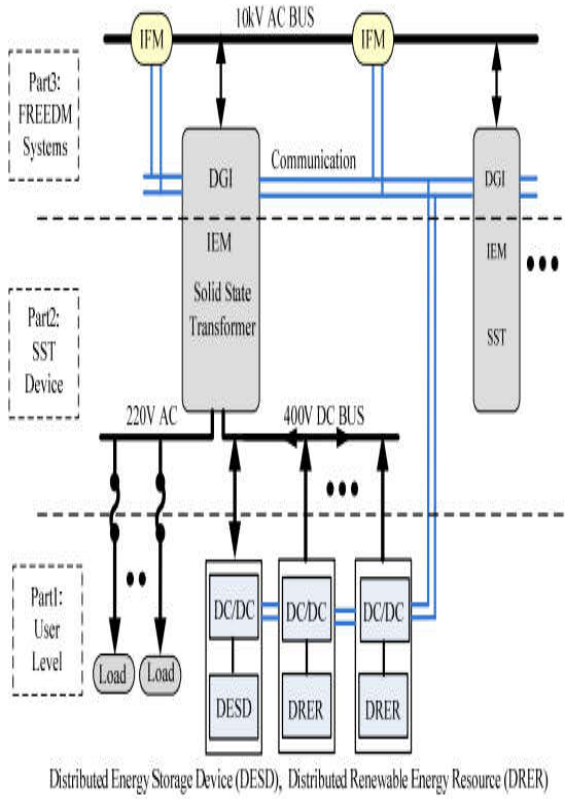


Fig. 1. The microgrid interface of the FREEDM system.

Fig. 1 shows a typical FREEDM system which consists of three parts. The first part is the user level interface that includes both a 400V-dc distribution bus and low voltage 220V-ac bus. The second part is an intelligent energy management (IEM) device, which is connected to 10kV ac distribution bus and supports the regulated buses. The IEM is actually formed by the SST that manages bidirectional power flow control to all devices connected to the low-voltage (400V-dc and 220V-ac) buses and loads. It also has many additional functions such as voltage regulation, voltage sag compensation, fault isolation and harmonic isolation. The third part is called the DGI (Distributed Grid Intelligence) operating system, which is embedded into the IEM device and utilizes the communication network to coordinate the system power management with other energy routers. Furthermore, an intelligent fault management (IFM) device is used to prevent potential faults in the 10kV-ac circuit and reconfiguration capability and uninterrupted power quality to the user [6]-[8].

An important objective of using the SST in the FREEDM system is to achieve compatibility and flexibility. It can regulate the low-voltage buses and provide active and reactive power control or power/frequency control for the grid side port.

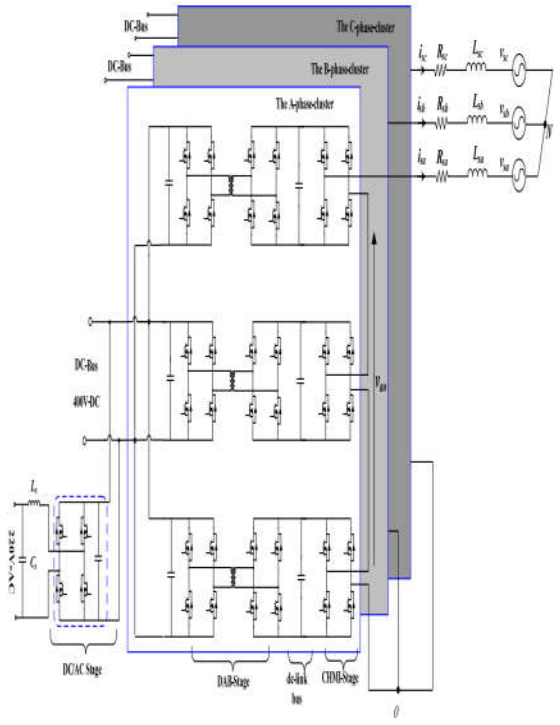


Fig. 2. Topology of the proposed 20kVA three-phase SST.

Fig. 2 shows the proposed 20kVA SST primarily based on the cascaded H-bridge multilevel inverter. The SST includes a dual active bridge (DAB) dc/dc stage to step up the 400V-dc input to the high-voltage dc hyperlink, a cascade H-Bridge multilevel dc/ac inverter level to provide active energy and reactive strength for the 10kV-ac grid, and a dc/ac stage to produce a 220V ac residential voltage for loads.

The controller employs the moving floating neutral factor manipulate set of rules to balance the energy on the 3 phase ac-side and the dynamic reference voltage method (feed forward compensation) to stability the dc-hyperlink voltage of different modules in each phase. A master-slave control (MSC) is used to manipulate the output of the DAB stage.

II.THREE-PHASE SST MODELING AND CONTROL

The topology and control strategy of three-phase SST (Fig. 2) are developed in this section. The prototype of the SST is rated as input dc-link voltage of 400V, output ac-voltage of 10kV and output power of 20kVA. The first stage of SST is high-frequency DAB converter which boosts low-voltage dc input to high-voltage dc link. The second stage is CHMI, which converts the dc link voltage to medium voltage ac grid, and controls active and reactive power delivered to grid.

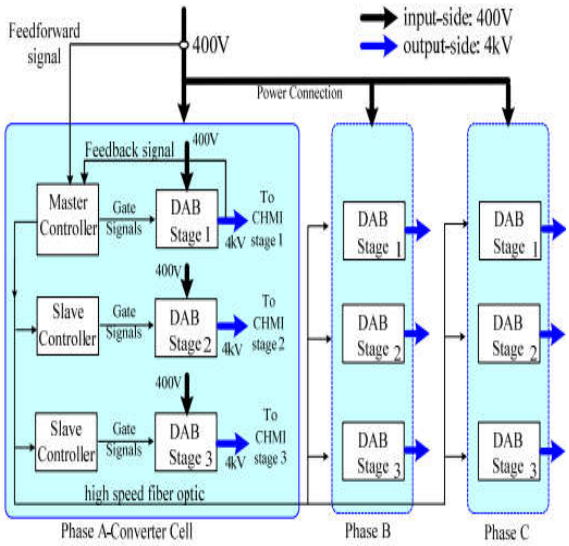


Fig. 3. Master-slave control diagram of the DAB converter stages.

Fig. 3 shows architecture of the DAB stages and their control circuit. The DAB stage steps up the 400V dc input to 4kV dc output which is fed to CHMI stage. In the proposed control circuit only one DAB converter is utilized as the master Fuzzy Logic Controller which executes all control and modulation calculations and sends the resultant converter driving command signals to the other DAB slave controllers via high speed fiber optic. Typically, DAB slave controllers only manage devices switching and protection. Also to calculate the power transferred by each module and implement the protection of over-voltage and over-current, the voltage and current of input-side and output-side are all sensed. Therefore, the proposed master-slave controller in the DAB stage not only provides the high frequency galvanic isolation, but also simplifies the complex algorithm and improves the dynamic performance.

The function of CHMI stage is to produce sinusoidal 3-phase output voltage/current and control the active/reactive power injected into the grid. Fig. 4 shows the block diagram of 3-phase decoupled current controller developed for the CHMI stage.

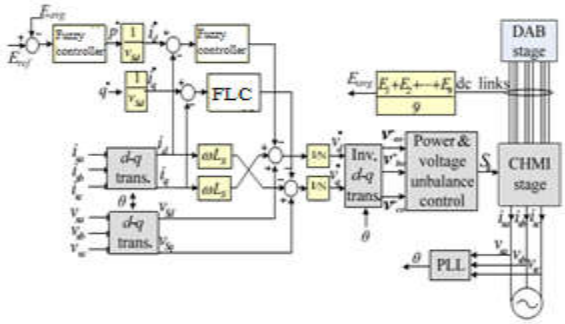


Fig. 4. Control scheme of the three-phase grid currents.

The dc-link voltage drift is indirectly dealt with by modulating the voltage reference amplitude of each phase according to the respective imbalance proportion which causes unbalanced power drawn by each module until the balance is achieved. In addition, the reactive power reference can be controlled at different values depending on the system requirements.

Due to the modularity of topology, Phase-Shifted PWM (PS-PWM) is the optimum modulation method for CHMI stage. The switching state of one H-bridge-module S_k is determined by the logical value of two signals, (S_{k1}, S_{k2}) which can be "1" and "0" representing the "ON" and "OFF" state of each switch, respectively. This leads to four different binary combinations that generate three different output voltage $+V_{dc}$, 0, and $-V_{dc}$. Since these H-bridge-modules are connected in series, the total output voltage of one phase m (m=a, b, c) is given by

$$v_{mN} = \sum_{y=1}^{k} v_{my} = \sum_{y=1}^{k} V_{dc}(S_{y1} - S_{y2}) \qquad (1)$$

Where k is the number of power modules per phase and V_{dc} is the dc-link voltage of each module. The series connection of k modules will produce 2k+1 voltage levels in the total converter output voltage.

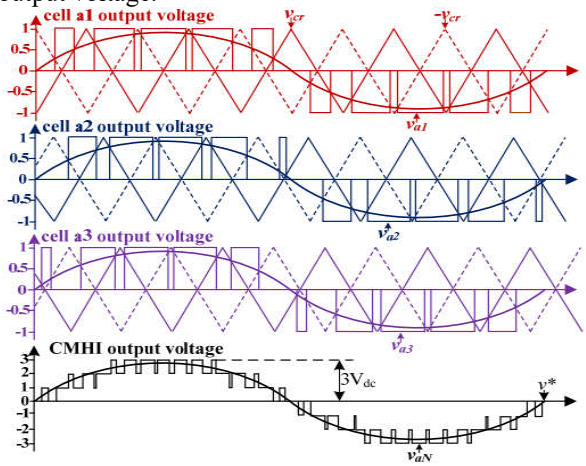


Fig. 5. Phase-shifted PWM waveforms for a 3-module CHMI.

The PS-PWM modulation principle with 3 modules per phase is shown in Fig. 5. Due to the modularity of the topology, each module can be modulated independently using unipolar PWM with the same reference signal [5]. In this paper, three modules carrier signals are controlled at the same frequency 1 kHz and shifted by 2π/3 rad from each other. Since the phase shift introduces a multiplicative effect, the CMHI line-to-neutral voltage has a switching pattern with 3 times the frequency the switching devices of each module. Hence, this converter can easily reach medium-voltage without the low frequency transformer and the total harmonic distortion (THD) is lower.

III.POWER AND VOLTAGE BALANCE CONTROL SCHEME

Since sending the same PWM signals to each DAB by fiber optic, the power is evenly distributed among the modules. However, this is unlikely to have identical switching devices and high-frequency transformer parameter for each DAB, resulting in the difference of power transferred by DAB modules. Consequently, this situation originates two types of imbalance in CHMI stage: per-phase and per-module. The first unbalance problem is the difference of real power delivered by each phase, $(P_a \neq P_b \neq P_C)$ while the second is the difference of real power delivered by each module of phase

$m(P_{m1} \neq P_{m2} \neq P_{m3})$.

These two unbalances affect the performance of the CHMI in two different ways: the per-phase unbalance affects the current inner-loop leading to unbalanced grid currents which generates a power pulsation in the output ac-side. The per-module unbalance will make the dc-link voltage drift from its reference value, result in distortion and potentially damaging power devices by overvoltage. In this section, these two types of unbalance will be addressed.

A.Per-phase Power Unbalance Compensation Scheme

The objective of this control approach is to share equally the power at the 3-phase ac-side under unbalance conditions. In order to present the scheme, assume that the power transferred by DAB of phase A is lower than phase B. As shown in Fig. 2, the line-to-neutral voltage equation of the power circuit can be described by

$$\begin{cases} v_{sa} = V_{ao} - L\frac{di_{sa}}{dt} - Ri_{sa} + u_{NO} \\ v_{sb} = V_{bo} - L\frac{di_{sb}}{dt} - Ri_{sb} + u_{NO} \\ v_{sC} = V_{ao} - L\frac{di_{sc}}{dt} - Ri_{sc} + u_{NO} \end{cases} \quad (2)$$

For a star-connection cascade inverter the neutral point is floating, since it is not grounded. Thus, it is difficult for current controller to directly produce the 3-phase reference voltages to maintain the balanced output currents under unbalanced conditions. Note that the common voltage u_{NO}can affect the 3-phase currents according to equation (4).

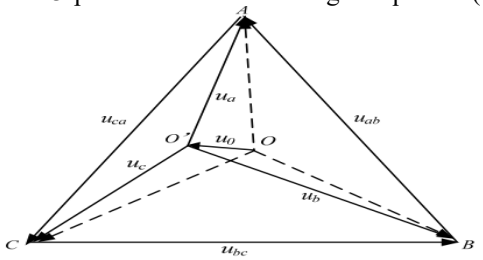


Fig. 6. Phasor voltage with the proposed neutral point shift method.

Fig. 6 shows an example of voltage phasor triangle to rebalance 3-phase currents under unbalanced conditions. When the power transferred by 3-phase modules is the same, the output line-to-neutral voltage amplitudes of each phase are equal as shown by dotted lines. Assume the power transferred by phase A is less than the others, if the reference output voltage of each phase is still the same, the output current of phase A will be lower. As a result, unbalanced output current occurs and causes failure for the grid connection. Therefore, to maintain balanced three-phase currents this paper employs the moving floating neutral point algorithm to produce different output voltage reference for each phase.

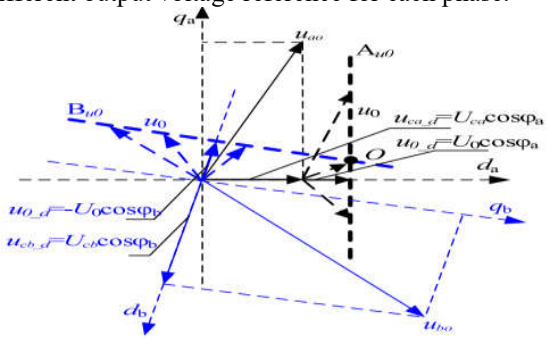


Fig. 7. Phasor diagram showing how to find out zero-sequence voltage U_0

The mathematical proof is presented as follow. First, calculate the amplitude and phasor of injection of zero sequence voltage U_0. The average active power in each phase can be expressed by

$$\frac{1}{2}U_{a0}I_a\cos(\varphi_{a0}-\varphi_{ia}) + \frac{1}{2}U_{a0}I_a\cos(\varphi_{a0}-\varphi_{ia}) = P_a + P_0 = P_{av}$$

$$\frac{1}{2}U_{b0}I_b\cos(\varphi_{b0}-\varphi_{ib}) + \frac{1}{2}U_0I_b\cos(\varphi_0-\varphi_{ib}) = P_b - P_0 = P_{av} \quad (3)$$

The equation (5) can be rewritten as

$$\frac{1}{2}U_0I_a\cos(\varphi_0-\varphi_{ia}) = P_{av} - P_0 = P_a(r_a-1)$$

$$\frac{1}{2}U_0I_b\cos(\varphi_0-\varphi_{ib}) = P_b - P_{av} = P_b(1-r_b) \quad (4)$$

By separately dividing the left and the right parts of (6) by each other, a factor can be obtained by

$$k_{com} = \frac{\cos(\varphi_0-\varphi_{ia})}{\cos(\varphi_0-\varphi_{ib})} = \frac{I_b}{I_a}$$

$$k_{com} = \frac{\cos(\varphi_0-\varphi_{ia})(r_a-1)}{\cos(\varphi_0-\varphi_{ib})(1-r_b)} \quad (5)$$

Substituting the obtained k_{com}

$$\frac{\cos(\varphi_0-\varphi_{ia})}{\cos(\varphi_0-\varphi_{ib})} = \frac{U_{a0}\cos(\varphi_{a0}-\varphi_{ia})(r_a-1)}{U_{b0}\cos(\varphi_{b0}-\varphi_{ib})(1-r_b)} \quad (6)$$

Then, a solution of the phase of U_0can be obtained by

$$\varphi_0 = \tan^{-1}\frac{\cos\varphi_{a0} - k_{com}\cos\varphi_{ib}}{k_{com}\sin\varphi_{ib} - \sin\cos\varphi_{a0}} \quad (7)$$

Finally, substituting the calculated into (5), the zero sequence of U_0can be obtained by using the known voltage and current parameters

$$U_{0m} = \left| \frac{2P_a r_a - U_{a0} I_a \cos(\varphi_{a0} - \varphi_{ia})}{I_a \cos\left(\tan^{-1}\left(\frac{\cos\varphi_{a0} - k_{com}\cos\varphi_{ib}}{k_{com}\sin\varphi_{ib} - \sin\cos\varphi_{a0}}\right)\right)} \right| \quad (8)$$

After obtaining the zero sequence voltage U_0 is calculated according to (11), and injecting to each reference to introduce the corresponding line-to-neutral voltage shift. This originates the compensated phase voltage reference is given in the Fig. 8. Then, prove that the zero-sequence voltage U_0 cannot change the three-phase summed active and reactive power.

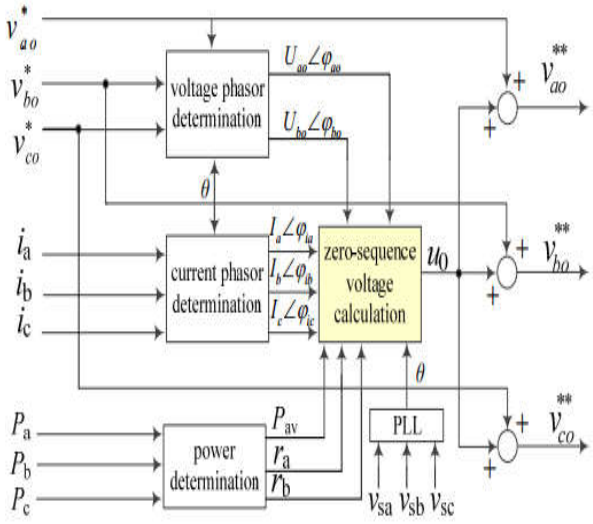


Fig. 8. Block diagram of the proposed per-phase power balance controller.

B.Per-Module Voltage Unbalance Control Mechanism

Each phase consists of three DAB dc/dc converters, the power unbalanced can appear on the different modules of one phase due to the device loss mismatching and H-Bridge active power differences. The dc link voltage drift must be avoided, because this unbalanced situation might cause the capacitor or IGBT device overvoltage and trigger the system overvoltage protection.

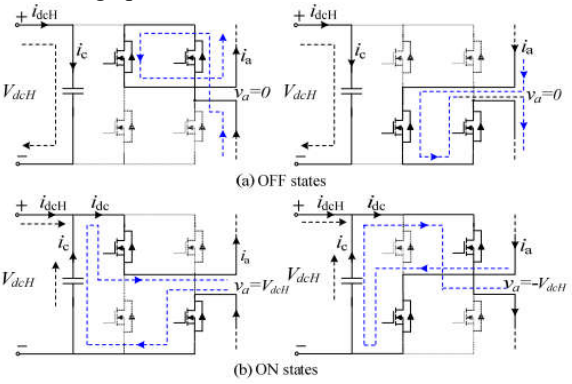


Fig.9. Per cell dc-link voltage dependence on the switching states of for one H-bridge module.

To better understand the modulation, the different switching states of one module are shown as Fig. 10.

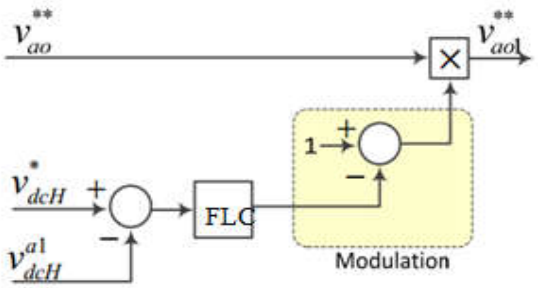


Fig. 10. Per-module dc-link voltage balance controller (feed forward compensation).

C.Analysis of Stability Operation Range

Due to the intrinsic constraints of the cascaded H-bridge structure, there is a limitation on the degree of unbalance in practical applications [22]. According to the principle of the compensation scheme, this might result in over modulation when the power transferred by DAB module is strongly unbalanced. If the power unbalance is out of the derived range, this controller will not be able to balance the dc-link voltages and 3-phase current. To better understand of the stability margin, the paper utilizes mathematical model to analyze the converter operation. In the steady state, according to Fig. 2 the voltage of Phase A can be described as follow:

$$\begin{cases} v_{a0} = v_{sa} + j\omega L i_{sa} - u_{No} \\ v_{sn} = v_{ao} + u_{No} \\ v_{sn} = v_{sa} + j\omega L i_{sa} \end{cases}$$

$$v_i = (m_{di} + j m_{qi}) E_{ref} \quad (9)$$

Where E_{ref} is the dc-link output voltage reference of DAB module, v_i is the ac-side output voltage of ith H-bridge, i_{sa} is the output ac current and m_{di} and m_{qi} are the modulation index of the direct and orthogonal components of the associated module, respectively.

IV.FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

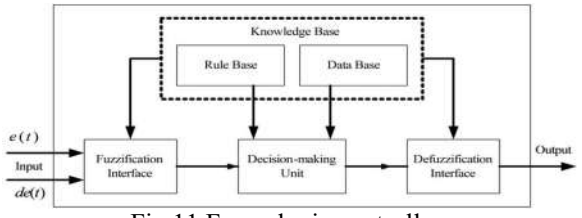


Fig.11.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

TABLE I: Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor. In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (10)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (11)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output.

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (12)$$

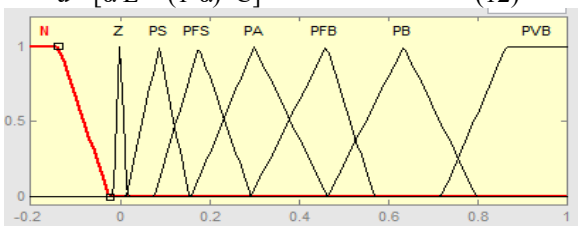


Fig 12 input error as membership functions

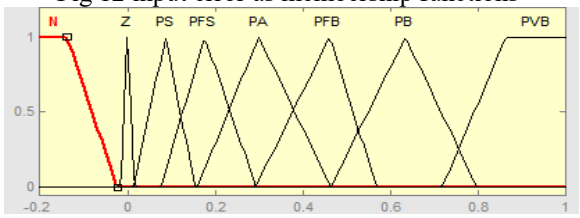


Fig 13 change as error membership functions

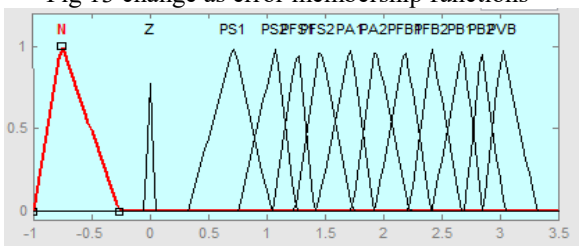


Fig.14 output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

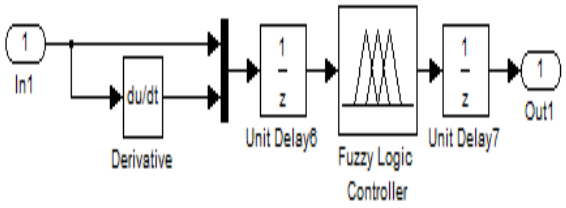


Fig 15.fuzzy logic controller in simulation

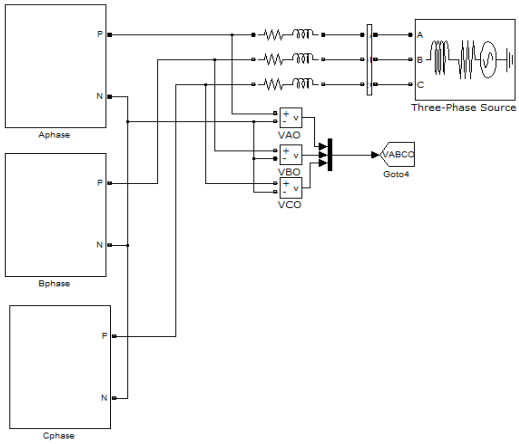


Fig.16 Block diagram of simulation

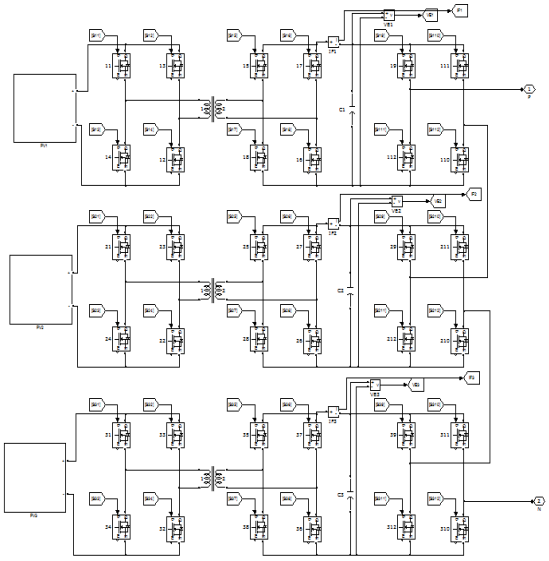


Fig.17 Simulation diagram of SST

V.SIMULATION RESULT

To verify the proposed power and voltage balance controller simulation prototype of Fig. 2 is implemented using simulation. The simulation parameters are listed in Table I.

Table II

Circuit Parameters of The Simulation System

Basic Parameters	Symbol	Value
Output AC Voltage	V_S	10kV
Power Rating	P	20kVA
Cascaded Number	N	3
AC-Side Inductance	L_{AC}	2mH
AC-Side Resistance	R_S	0.1mΩ
Switching Device Frequency	f	500Hz
DC-Link Capacitance	C	5mF

The PV module curves corresponding to different power levels are shown in Fig. 18. The simulation results for the dynamic and steady state performance are illustrated in Fig. 19-21.

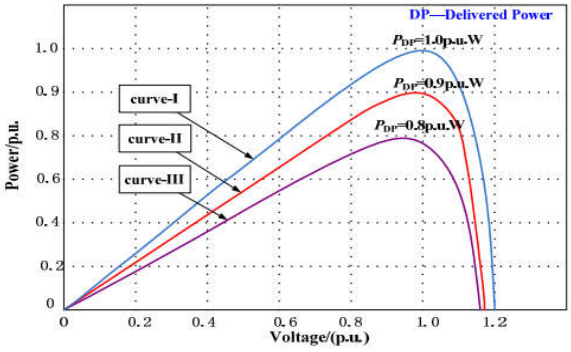
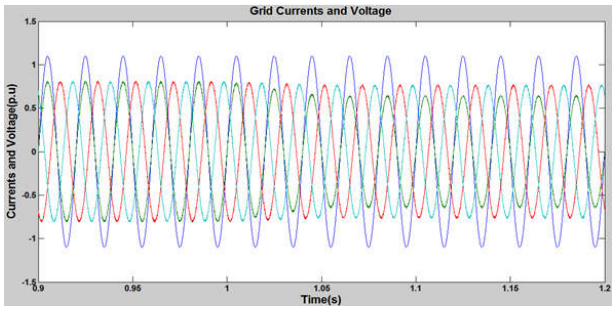
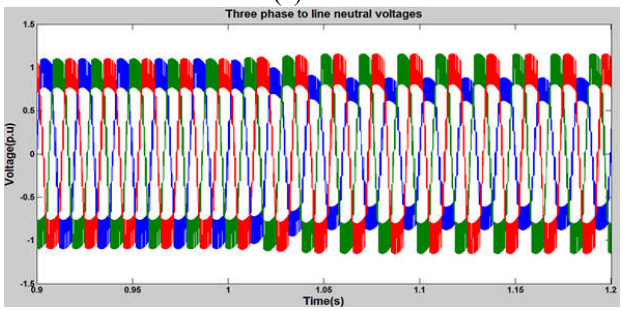


Fig. 18. Power versus voltage curves of PV module.

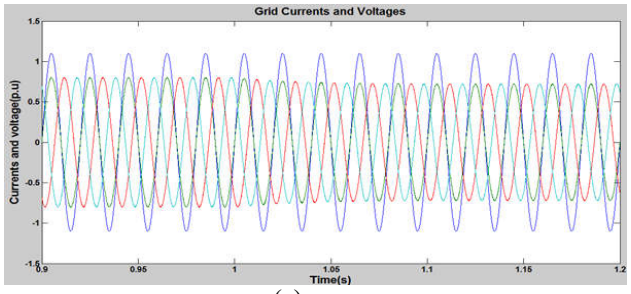


(a)

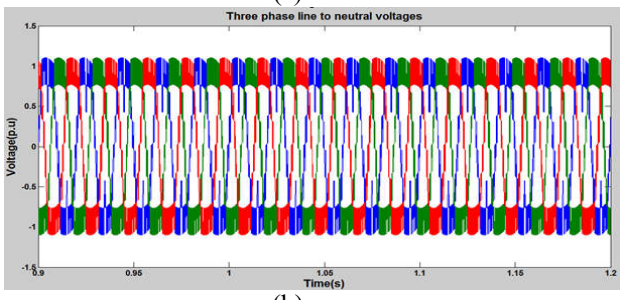


(b)

Fig. 19. Dynamic performance without power balance control. (a) Grid currents $(i_a, i_b, i_c)$and the grid voltage . v_{sa}(b) Three-phase line-to-neutral voltages .(v_{ca}, v_{cb}, v_{cc})



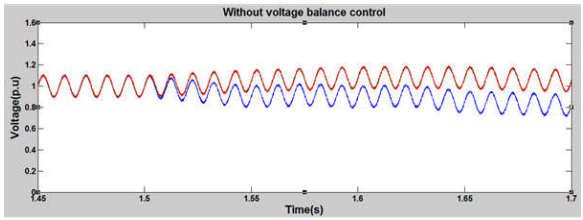
(a)



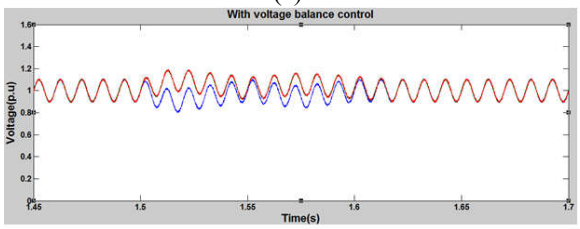
(b)

Fig. 20. Dynamic performance with power balance control. (a) Grid currents (i_a, i_b, i_c) and grid voltage v_{sa}. (b) Three-phase line-to-neutral voltages(v_{ca}, v_{cb}, v_{cc}) .

Fig. 19 shows the dynamic performance of 3-phase output currents with a step phase unbalance in phase A at t=1s and no power balance control. Fig. 20 shows 3-phase output currents with the power balance control.



(a)



(b)

Fig. 21. Dynamic performance of three DC-link voltages of phase B. (a) Without voltage balance control. (b) With voltage balance control.

To validate the voltage balance control, the dc-link voltages of three modules of phase B are given in Fig. 21. Fig. 21(a) shows the three dc-link voltages cannot maintain at the reference value without voltage unbalance control. The module that delivers more power has higher dc-link voltage. Fig. 21(b) shows the three dc-link voltages of phase B with the proposed voltage balance control.

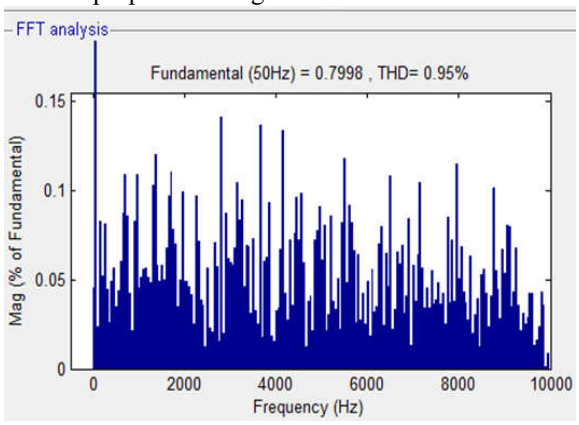


Fig 22 THD analysis with PI Controller

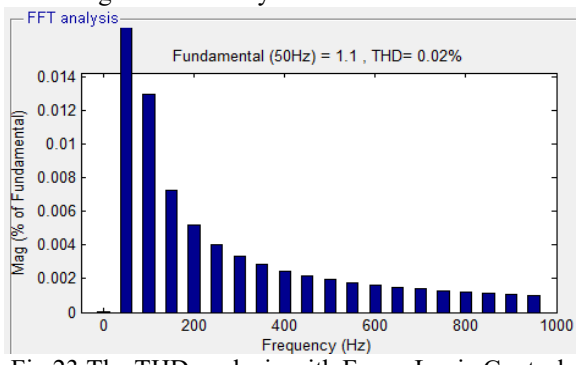


Fig 23 The THD analysis with Fuzzy Logic Control

VI.CONCLUSION

This paper investigates the application of the 3-phase SST and its controller with the energy flow from the distributed renewable energy resources to the grid under unbalanced conditions. This paper presents a compensation strategy based on three-phase d-q decoupled current controller. The fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system and improves the efficiency. In The proposed control method the three-phase grid currents and dc-link voltage in each module can be simultaneously balanced. The detailed control method is analyzed to address the presence of power and voltage unbalance: among three phases and the different modules of one phase. In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. The proposed balance control strategy is characterized for producing high quality grid currents and reactive power compensation. By using the simulation results we can analyze the proposed method.

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