DESIGN OF AN OVERLOAD CDMA ROUTER CROSSBAR ARCHITECTURE FOR NOC

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ABSTRACT: On-chip interconnects are the performance bottleneck in modern system-on-chips. Code-division multiple access (CDMA) has been proposed to implement on-chip crossbars due to its fixed latency, reduced arbitration overhead, and higher bandwidth. In this paper, we advance overloaded CDMA interconnect (OCI) to enhance the capacity of CDMA network-on-chip (NoC) crossbars by increasing the number of usable spreading codes. Serial-OCI and P-OCI architecture variants are presented to adhere to a different area, delay, and power requirements. The parallel OCI crossbar achieves N times higher bandwidth compared with the serial OCI crossbar at the expense of increased area and power consumption. Further to increase the speed of OCI crossbar we are implementing Brent Kung Adder in place of parallel adder architecture. This kind of extension results in High-speed P-OCI and serial-OCI compare to proposed P-OCI and serial-OCI architectures respectively.

Index Terms—Code-division multiple access (CDMA) interconnect, CDMA router, network-on-chip (NoC), NoC physical layer, overloaded CDMA crossbar.

I. INTRODUCTION

Code-division multiple access (CDMA) is another medium sharing technique that leverages the code space to enable simultaneous medium access. In CDMA channels, each transmit-receive (TX-RX) pair is assigned a unique bipolar spreading code and data spread from all transmitters are summed in an additive communication channel. The spreading codes in classical CDMA systems are orthogonal—cross-correlation between orthogonal codes is zero—which enables the CDMA receiver to properly decode the received sum via a correlator decoder. Classical CDMA systems rely on Walsh–Hadamard orthogonal codes to enable medium sharing. CDMA has been proposed as an on-chip interconnect sharing technique for both bus and NoC interconnect architectures. Many advantages of using CDMA for on-chip interconnects include reduced power consumption, fixed communication latency, and reduced system complexity. A CDMA switch has less wiring complexity than an SDMA crossbar and less arbitration overhead than a TDMA switch, and thus provides a good compromise of both. However, only basic features of the CDMA technology have been explored in the on-chip interconnect literature. NoCs provide a scalable solution for large SoCs, but they exhibit increased power consumption and large resource overheads. The NoC layering model splits the transaction into four layers: 1) application; 2) transport; 3) network; and 4) physical layers. A crossbar is the basic building block of the NoC physical layer. A cross-bar switch is a shared communication medium adopting a multiple access technique to enable physical packet exchange.

Overloaded CDMA interconnect (OCI) crossbar architecture increases the CDMA router capacity by 100% at marginal cost. Crossbar overloading relies on exploiting special properties of the used orthogonal spreading code set, namely, Walsh–Hadamard codes, to add a set of nonorthogonal spreading codes that can be uniquely identified on the receiver side.

The contributions of this paper are as follows.

1) Introduce two novel approaches that can be deployed in CDMA NoC crossbars to increase the router capacity and,

consequently, bandwidth by 100% at marginal cost.

2) Present the OCI mathematical foundations, spreading code generation procedures, and OCI-based router architectures.

II. RELATED WORK

Utilizing CDMA as a medium access conspires in crossbar switches gives ideal qualities like the settled exchange dormancy and low mediation overhead. Nikolic et al. have proposed a versatile CDMA-based fringe transport to diminish the quantity of parallel exchange lines and point-to-point (PTP) transports and to stay away from the overhead of TDMA referees. This approach decreases the stick check when utilized at the interface of various peripherals to different PEs since the information from the peripherals are included and transmitted less lines. The expansion in the exchange dormancy because of information spreading is worthy since peripherals as a rule work at bringing down frequencies than the ace PEs. A master-slave transport wrapper has been exhibited in and, where the information are packaged and spread utilizing orthogonal CDMA codes to diminish the quantity of parallel exchange lines. The control signals are not encoded to encourage interconnection to other TDMA transports.

The CDMA-based switch allows simultaneous packet transmission due to code-space multiplexing. This approach reduces the hop count in multicasting schemes and allows packets to reach the destination PEs simultaneously, which is preferred in real-time applications. The assignment of spreading codes to TX-RX pairs is dynamic based on the request from each node. Two architectures have been introduced in the CDMA-based network: a serial CDMA network, where each data chip in the spreading code is sent in one clock cycle, and a parallel CDMA network, where all data chips are sent in the same cycle. The CDMA-based serial and parallel networks have been compared with a conventional CDMA network, a mesh-based NoC, and a TDMA bus. For the same network area, the bandwidth of the parallel CDMA network is higher than the throughput of the mesh-based NoC and the TDMA bus due to the simultaneous medium access nature of CDMA.

III.EXISTING METHOD

In this section, overloaded CDMA in wireless communications and the requirements of its on-chip interconnect counterpart and preliminaries of the classical on-chip CDMA.

A. Overloaded CDMA in Wireless Communications:

Direct sequence spread spectrum CDMA (DSSS-CDMA) is the main approach for medium partaking in remote communications where an arrangement of orthogonal spreading codes made out of a surge of chips of length N are duplicated by the transmitted information bits to such an extent that every datum bit is spread in N cycles.

A one of a kind spreading code is relegated to each TX-RX combine sharing the correspondence channel. Information floods of clients sharing the channel are spread and all the while transmitted to an added substance correspondence channel. De spreading is accomplished by applying the connection operation to the got whole, where every recipient can separate its information by relating it with the doled out spreading code.

The switch is composed of a number of XOR encoders, a channel adder, and accumulator-based decoders. In the encoder, an N-chip length binary orthogonal code, generated from a Walsh spreading code set, is XOR-ed with the transmitted data bit and sent out serially, indicating that a single bit is spread in a duration of N clock cycles.

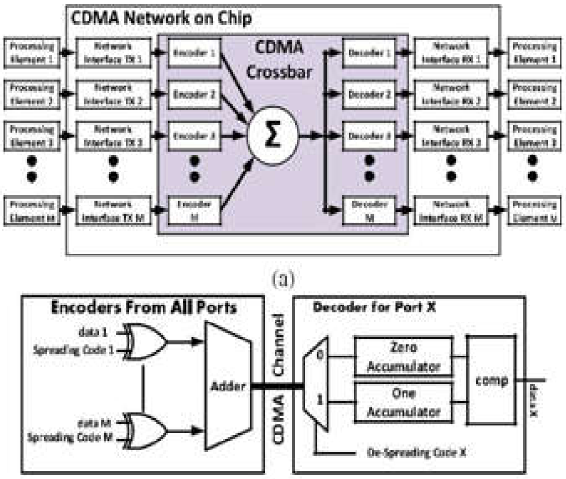


Fig. 1 (a) CDMA NoC router architecture. (b) Classical CDMA crossbar.

B. Classical CDMA Crossbar Switch

Fig. 1(a) illustrates the high-level architecture of a CDMA-based NoC router. The physical layer of the router is based on the classical CDMA switch.

Therefore, the crossbar transaction frequency ft and operating clock frequency fc are related as ft = fc/ N.

$$S(i) = \sum_{j=1}^{M} d(j) \oplus C_o(j, i) \qquad (1)$$

where S(i) is an m-bit binary number representing the channel sum at the ith clock cycle, the crossbar width m = log2 M, d(j) is the data bit from the jth encoder, Co(j, i) is the ith chip of the jth orthogonal spreading code, and ⊕ is the XOR operation. In the ordinary CDMA crossbar, the adder has M = N − 1 input bits and m = log2 M = log2 N output bits.

IV. PROPOSED METHOD

The main difference between the overloaded and classical CDMA routers is that M > N − 1 for the former due to channel overloading. Each PE is connected to two network interfaces (NIs), transmit and receive NI modules. During packet transmission from a PE, the packet is divided into flits to be stored in the transmit NI first-input first-output (FIFO). The router arbiter then selects M winning flits at most from the top of the NI FIFOs to be transmitted during the current transaction. The selected flits must all have an exclusive destination address to prevent conflicts, and a winner from two conflicting flits is selected according to the router's priority scheme.

A. OCI Crossbar High-Level Architecture

The main objective of this paper is increasing the number of ports sharing the ordinary CDMA crossbar presen while keeping the system complexity unchanged using simple encoding circuitry and relying on the accumulator decoder with minimal changes. To achieve this goal, some modifications to the classical CDMA crossbar are advanced. Fig. 2 depicts the high-level architecture of the OCI crossbar for a single-bit interconnection. The same architecture is replicated for a multi-bit CDMA router. M TX-RX ports share the CDMA router, where spread data from the transmit ports are added using an arithmetic binary adder having M binary inputs and an m-bit output, where m = log2 M.

B. OCI Code Design

The Walsh–Hadamard spreading code family has a featured property that enables CDMA interconnect overloading. The difference between any consecutive channel sums of data spread by the orthogonal spreading codes for an odd number of TX-RX pairs M is always even, regardless of the spread data. This property means that for the N − 1 TX-RX pairs using the Walsh orthogonal codes, one can encode additional N − 1 data bits in consecutive differences between the N chips composing the orthogonal code. Thus, exploiting this property enables adding 100% non orthogonal spreading codes, which can double the capacity of the ordinary CDMA crossbar.

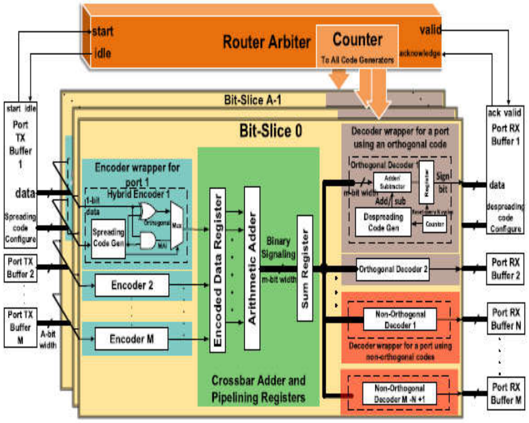


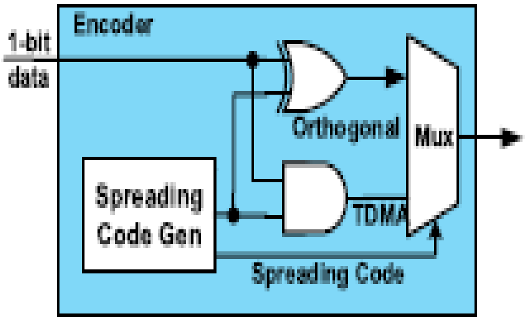
Fig. 2. High-level architecture and building blocks of the OCI crossbar.

C. OCI Crossbar Building Blocks

Two variants are realized for each OCI crossbar, reference, and pipelined architectures. The pipelined architecture is implemented to increase the crossbar operating frequency, and consequently, bandwidth by adding nonfunctional pipelining registers to reduce the crossbar critical path. The OCI crossbar shown in Fig. 2 is basically composed of three main building blocks: 1) the encoder wrappers; 2) the decoder wrappers; and 3) the crossbar adder blocks, which are described in the following.

1) Crossbar Controller: Toward the start of every crossbar exchange, the controller relegates spreading codes to various encoders. The task of orthogonal de spreading codes to get ports is settled, i.e., does not change between the crossbar exchanges. In this way, for a switch port to start the correspondence with the get port it addresses, its encoder must be doled out a spreading code that matches the predetermined decoder. In the event that two distinct ports demand to address a similar decoder, the controller permits one access and suspends the other as per a predefined mediation conspire. This code task conspire is called recipient based convention.

2) Hybrid Encoder: The encoder is hybrid, it can encode both orthogonal and nonorthogonal data. A transmitted data bit is XOR-ed/AND-ed with the spreading code to produce the orthogonal/non orthogonal spread data, respectively. A multiplexer chooses between the orthogonal and nonorthogonal inputs according to the code type assigned to the encoder as depicted by Fig. 2(a). The encoder is replicated N times for the P-OCI crossbar.



(a)

Fig 2(a) T-OCI/P-OCI hybrid encoder.

Crossbar Adder: For a spreading code set of length N, the number of crossbar TX-RX ports is equal to M = 2(N − 1). In the T-OCI crossbar, sending a “1” chip to the adder is mutually exclusive between non orthogonal transmit ports according to the T-OCI encoding scheme. This indicates that among the 2(N −1) inputs to the adder, there are guaranteed (N − 2) zeros, while the maximum number of “1” chips is N. Therefore, a multiplexer is instantiated to select only a single input of the non orthogonal TDMA encoded data bits and discard the remaining bits that are guaranteed to be “0.”

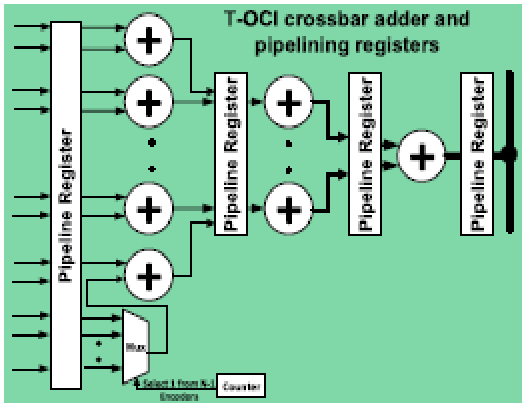


Fig2(b) T-OCI pipelined crossbar tree adder, in which the adder is replicated N times for P-OCI crossbar.

4) Custom Decoder: There are four decoder types for different CDMA decoding techniques: the orthogonal T-OCI and P-OCI decoders and the over-loaded T-OCI and P-OCI decoders. The orthogonal T-OCI decoder is an accumulator implementation of the correlator receiver. N − 1 accumulator decoders are instantiated in all CDMA crossbar types for orthogonal data despreading. Instead of implementing two different accumulators (the zero and one accumulator), an up-down accumulator is implemented and the accumulated result is the difference between the two accumulators of the conventional CDMA decoder as shown in Fig 2(d).

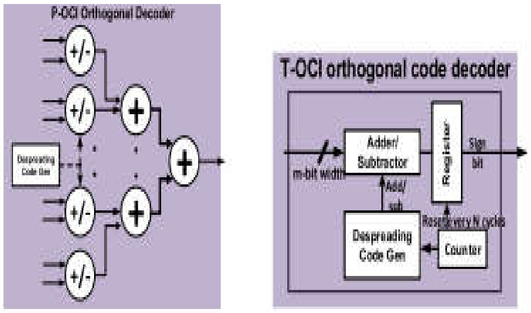


Fig2(c) P-OCI orthogonal decoder. 2(d) T-OCI orthogonal decoder.

The accumulator adds or subtracts the crossbar sum values according to the despreading code chip and resets every N cycles. The sign bit of the accumulated value directly indicates the decoded data bit, where the positive sign is decoded as “1,” while the negative sign is decoded as “0.” The P-OCI orthogonal decoder shown in Fig. 2(c) differs from the T-OCI orthogonal decoder in receiving the adder sum values concurrently not sequentially; therefore, the accumulator loop is unrolled into a parallel adder.

Nonorthogonal Decoder:

The T-OCI overloaded decoder depicted in Fig. 2(e) is composed of a 2-bit register to store the LSBs of two sum values, first of which is S(0) and the second is S(j − N + 1), where j is the number of the T-OCI decoders (N ≤ j ≤ 2N − 2). The two bits are fed to the XOR gate, which decodes nonorthogonal spread data. The T-OCI decoder is replicated N times to implement the P-OCI decoder of Fig. 2(f). The 2-bit register is not needed anymore because the S(0) and S(j−N+1) values exist in the same cycle. The T-OCI and P-OCI crossbar architectures contain (N − 1) orthogonal decoders and (N − 1) overloaded decoders.

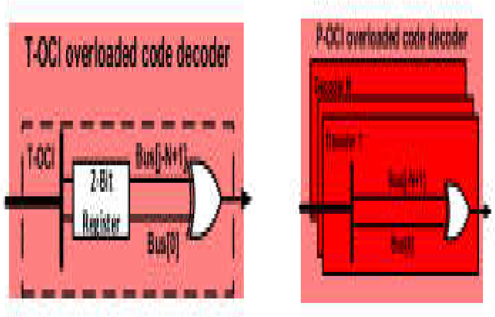


Fig: 2(e) T-OCI nonorthogonal decoder. (f) P-OCI nonorthogonal decoder.

V. BRENT KUNG ADDER

The structure of any adder greatly affects the speed of the circuit. The logarithmic structure is considered to be one of the fastest structures. The logarithmic concept is used to combine its operands in a tree-like fashion. The logarithmic delay is obtained by restructuring the look-ahead adder. The restructuring is dependant on the associative property, and the delay is obtained to be equal to (log2N) t, where 'N' is the number of input bits to the adder and t is the propagation delay time. Hence, for a 16-bit structure, the logarithmic adder has a delay equal to '4t', while for a simple ripple carry adder the delay is given by (N-1)t and is equal to '15t' for 'N' and 't' being the number of input bits and the delay time, respectively. Hence it is seen that this structure greatly reduces the delay, and would be especially beneficial for a structure with a large number of inputs. This advantage is, however, obtained at the expense of a large area and a complex structure.

Brent Kung Architecture

In order to approach the structure known as the Brent Kung Structure, which uses the logarithmic concept, the entire architecture is easily understood by dividing the system into three separate stages:

1. Generate/Propagate Generation
2. The Dot (·) Operation
3. Sum generation

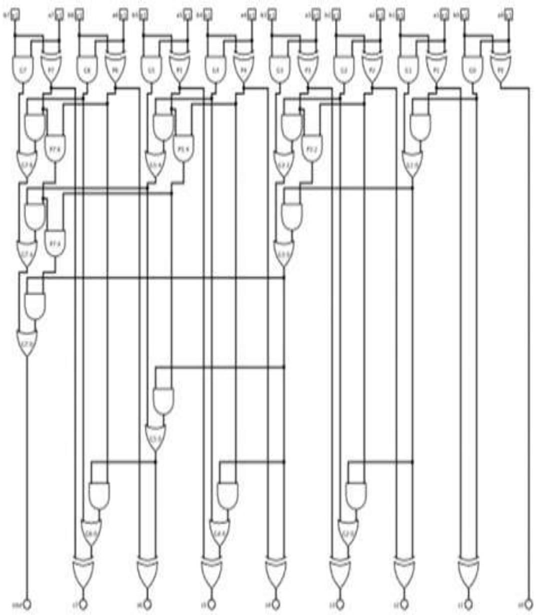
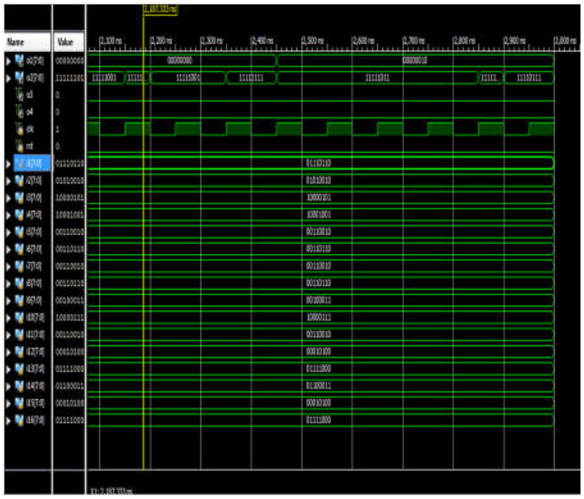


Fig:3 Schematic of 8-bit Brent Kung Adder

VI. RESULTS

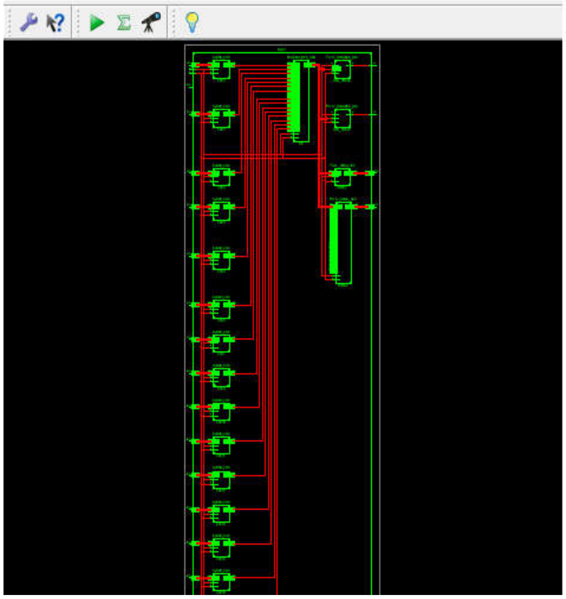
PROPOSED RESULTS:

Simulation Results:

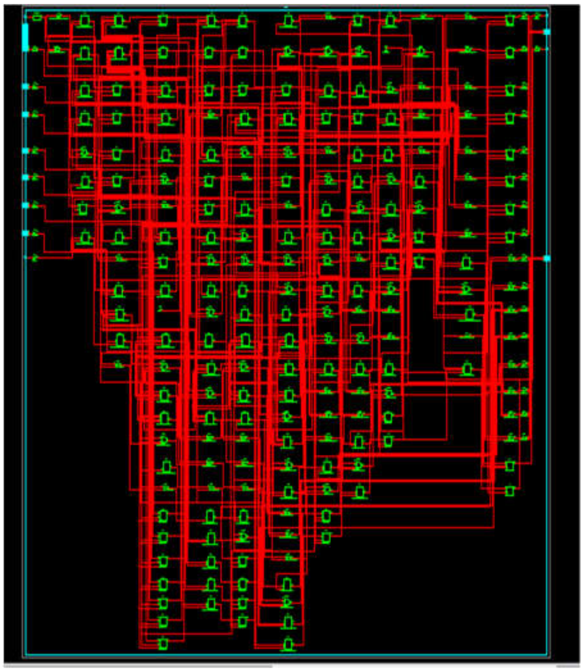


Name	Value
o1[7:0]	00000000
o2[7:0]	11111101
o3	0
o4	0
clk	1
rst	0
i1[7:0]	01110110
i2[7:0]	01010010
i3[7:0]	10000101
i4[7:0]	10001001
i5[7:0]	00110010
i6[7:0]	00110110
i7[7:0]	00110010
i8[7:0]	00110110
i9[7:0]	00100011
i10[7:0]	10000111
i11[7:0]	00110010
i12[7:0]	00010100
i13[7:0]	01111000
i14[7:0]	01100011
i15[7:0]	00010100
i16[7:0]	01111000

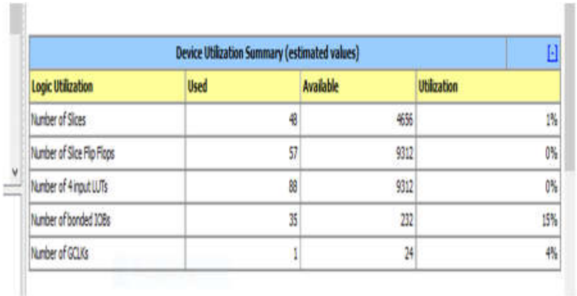
RTL Schematic:



Technology Schematic:

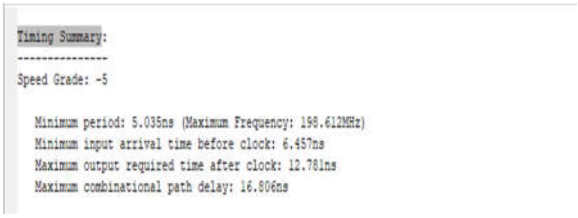


Design and Summary:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	48	4656	1%
Number of Slice Flip Flops	57	9312	0%
Number of 4 input LUTs	88	9312	0%
Number of bonded IOBs	35	232	15%
Number of GCLKs	1	24	4%

Timing report:



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Timing Summary:
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Speed Grade: -5

   Minimum period: 5.035ns (Maximum Frequency: 198.612MHz)
   Minimum input arrival time before clock: 6.457ns
   Maximum output required time after clock: 12.781ns
   Maximum combinational path delay: 16.806ns
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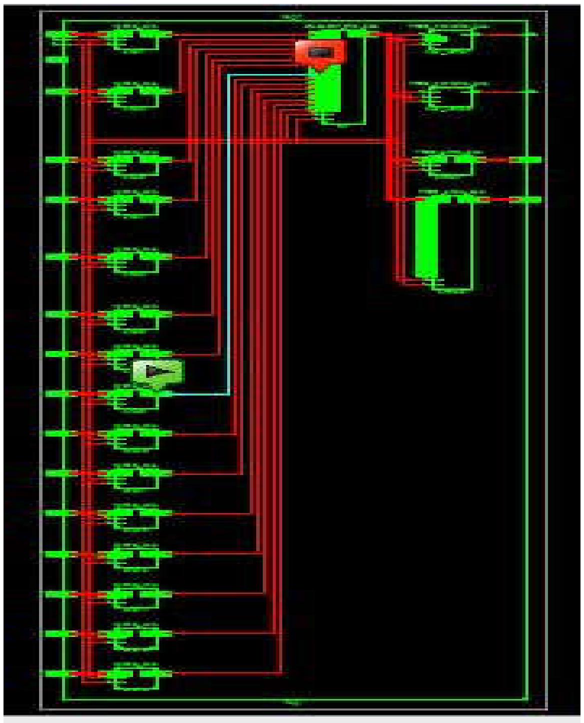
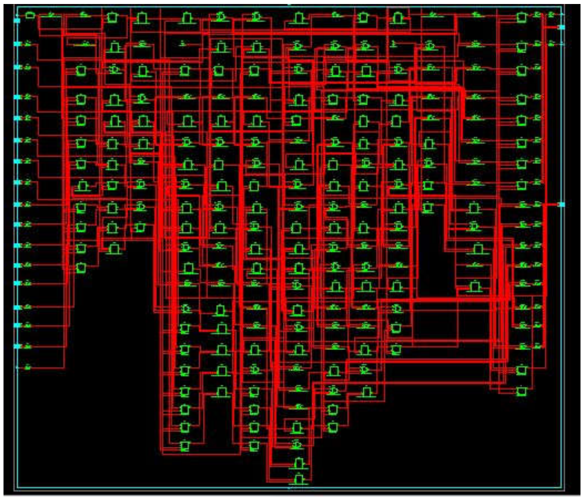
USING BRENT KUNG ADDER RESULTS:

Simulation Results:

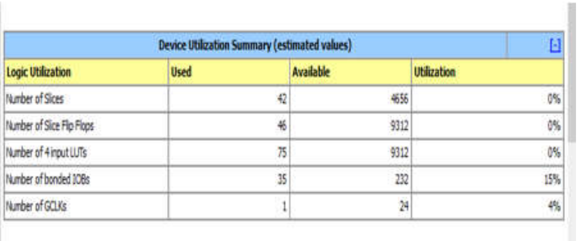
RTL Schematic:



Technology Schematic:

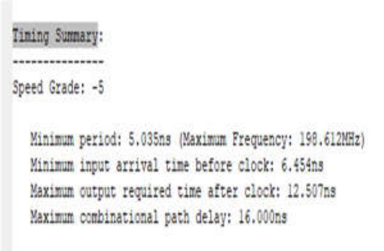


Design and Summary:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	42	4656	0%
Number of Slice Flip Flops	46	9312	0%
Number of 4 input LUTs	75	9312	0%
Number of bonded IOBs	35	232	15%
Number of GCLKs	1	24	4%

Timing Report:



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Timing Summary:
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Speed Grade: -5

   Minimum period: 5.035ns (Maximum Frequency: 198.612MHz)
   Minimum input arrival time before clock: 6.454ns
   Maximum output required time after clock: 12.507ns
   Maximum combinational path delay: 16.000ns
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VII. CONCLUSION

In this paper, we introduced the concept of area-time efficient OCI crossbars as the physical layer enabler of NoC routers. We exploited High-speed low area adders in the proposed system. Two crossbar architectures that leverage the overloaded CDMA concept, namely, T-OCI and P-OCI, are advanced to increase the CDMA crossbar capacity. We exploited featured properties of the Walsh spreading code family employed in the classical CDMA crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CDMA crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars with Brent Kung adder are implemented and validated on a Xilinx ISE design Suite. The use of Brent Kung adder gives better performance than the proposed system.

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