CHARGE PUMP CIRCUIT CONCEPT FOR SINGLE-PHASE TRANSFORMERLESS INVERTER WITH FUZZY LOGIC CONTROLLER FOR GRID-TIED PV APPLICATIONS

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ABSTRACT-- This project proposes a charge pump circuit concept for single phase transformerless inverter with FLC for PV applications. The topology is derived from the concept of a charge pump circuit in order to eliminate the leakage current. It is composed of four power switches, two diodes, two capacitors, and an LCL output filter. The unbiased of grid is specifically allied with negative extremity of PV board that makes a constant basic mode vtg and zero leakage current. The charge pump circuit generates the negative output voltage of the proposed inverter during the negative cycle. A analogous full control procedure is used to control the injected current. The precept advantages of furthered inverter are: 1) unbiased of grid is directly allied with -ve terminal of PV board, so the spillage current is wiped out; 2) its minimized size; 3) ease; 4) the exerted dc vtg of furthered inverter is same as the FL inverter not at all like neutral point clasped (NPC), active NPC, and HB inverters); 5) adaptable establishing setup; 6) ability of RP stream; and 7) high productivity. An entire depiction of working precept and examination of furthered in verter are exhibited. The obtained results clearly validate the performance of the proposed inverter and its practical application in grid-tied PV systems.

INTRODUCTION

Over the last two decades, the photovoltaic (PV) power systems have become very popular among the renewable energy sources, because they generate electricity with no moving parts, operate quietly with no emissions, and require little maintenance [1], [2]. Distributed grid-connected PVs are playing an increasingly role as an integral part of the electrical grid. However, due to the large stray capacitors between the PV panels and the ground, PV systems suffer from a high common mode (CM) current, which reduces the system efficiency and may cause safety issues like electric shock. In order to eliminate the leakage currents, transformers are commonly used in the PV system to provide galvanic isolation. However, it possesses undesirable properties including large size, high cost, and weight with additional losses [3]. Thus, eliminating the transformer is a great benefit to further improve the overall system efficiency, reduce the size, and weight [4].

One of the important issues in the transformerless gridconnected PV applications is the galvanic connection of the grid and PV system, which leads to leakage current problems. For transformerless grid-connected inverters, full-bridge (FB) inverter, neutral point clamped (NPC), active NPC (ANPC) inverter [5], and many other topologies such as H5, H6, and highly efficient and reliable inverter concept (HERIC) were proposed to reduce the leakage current with disconnecting of the grid from the PV during the freewheeling modes [6]. However, these topologies are not totally free from CM current or leakage current. The leakage current still exists due to the parasitic capacitor of the switch and stray capacitance between the PV panel and ground. So, some of these topologies require two or more filter inductors to reduce the leakage current, which leads to a rise in the volume and cost of the system [7].

Fig. 1 illustrates a single-phase grid-tied transformerless inverter with CM current path, where P and N are the positive and negative terminals of the PV, respectively. The leakage current (iLeakage) flows through a parasitic capacitor (CP) between the filters (L1 and L2), the inverter, grid, and ground impedance (zg). This leakage current may cause safety problems, reduce the quality of injection current to the grid, as well as decrease the system efficiency [8].

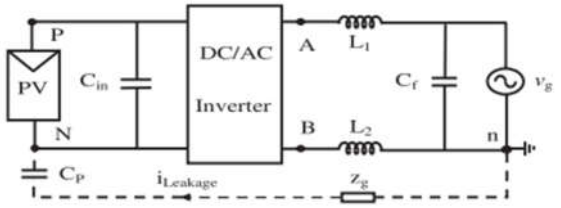

Fig. 1. Block diagram of a single-phase grid-connected transformer less inverter with a leakage current path.

In order to eliminate the leakage current, the CM voltage (CMV) (vcm)must be kept constant during all operation modes according to [9]. The vcm with two filter inductors (L1, L2) is calculated as follows:

$$v_{cm} = \frac{v_{An}+v_{Bn}}{2} + \frac{(v_{An} - v_{Bn})(L_2 - L_1)}{2(L_1 + L_2)} \quad (1)$$

where vAn and vBn are the voltage differences between the midpoints A and B of the inverter to the dc bus minus terminal N, respectively. If L1 = L2 (asymmetrical inductor), vcm is calculated

according to (1) and the leakage current appears due to a varying CMV. If L1 = L2 (symmetrical inductor), vcm is simplified to

$$v_{cm} = \frac{v_{An} + v_{Bn}}{2} = const \quad (2)$$

In this state, the CMV is constant and the leakage current is eliminated. In some structures such as the virtual dc-bus inverter [10] and NPC inverter, one of the filter inductors is zero and only one filter inductor is used. In this state, after simplification of vcm, it will have a constant value according to (3) and the leakage current will be eliminated

$$v_{cm} = \frac{v_{An} + v_{Bn}}{2} + \frac{v_{An} - v_{Bn}}{2} = const \ (L_1 = 0)$$

$$v_{cm} = \frac{v_{An} + v_{Bn}}{2} - \frac{v_{An} - v_{Bn}}{2} = const \ (L_2 = 0) \quad (3)$$

As shown in Fig. 2, there are various transformerless grid connected inverters based on the FB inverter in the literature to overcome these problems.

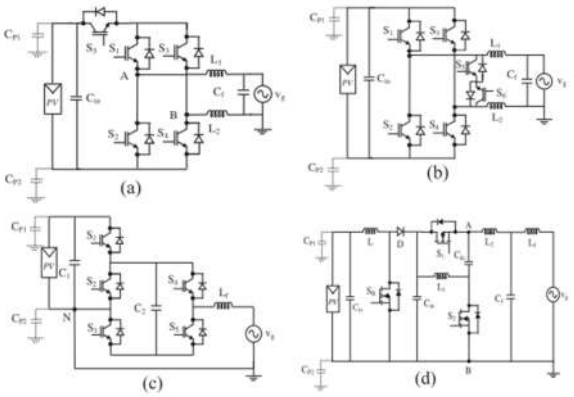

Fig. 2. Single-phase grid-tied transformerless PV inverter topologies: (a) H5 inverter, (b) HERIC inverter, (c) virtual dc-bus inverter [10], and (d) CM inverter proposed in [18].

The H5 inverter that is a FB-based inverter topology, com pared to the conventional FB inverter, needs one additional switch (S5) on the dc side to decouple the dc side from the grid as shown in Fig. 2(a). This inverter has a variable CMV with a small leakage current and it suffers from low efficiency due to three switches operating at the same time [11].

As shown in Fig. 2(b), the HERIC topology needs two extra switches on the ac side to decouple the ac side from the PV module in the zero stage. HERIC combines the merits of unipolar and bipolar modulation. The main advantage of the HERIC inverter is its high efficiency due to only two switches operate at the same time in all operation modes. This topology does not allow for reactive power flow [12].

Topologies based on H6 are also proposed in [13] and [14] to eliminate the leakage current of the grid-tied PV application. These inverters consist of six power switches and some diodes for disconnecting the dc side from the grid. These topologies are more costly than the FB inverter, because they use extra switches and diodes. Another disadvantage of these topologies is lower efficiency due to the current that circulates through three power switches at the same time [15]. Several high efficient new H6 transformerless inverters are proposed in [16] and [17] to achieve lightweight and also lower cost. They have the capability of reactive power injection to the grid. The leakage current is not totally eliminated in these topologies, which is the main disadvantage of them.

Another solution to eliminate the leakage current is the direct connection of the negative PV terminal to the neutral point of the grid, such as the virtual dc-bus inverter in [10] and the unusual topology in [18]. In these topologies, the leakage current is completely eliminated by the topology structure. As shown in Fig. 2(c), the virtual dc-bus inverter is composed of five insulated-gate bipolar transistors (IGBTs), two capacitors, and one filter inductor Lf . Only one filter inductor is used in this topology to eliminate the leakage current, but it is very large. The virtual dc-bus generates the negative output voltage. The main drawback of this topology is that there is no path to charge the capacitor C2 during the negative cycle and this will cause a high output total harmonic distortion (THD). The topology presented in [18], which is shown in Fig. 2(d), has a common ground with the grid. The number of semiconductors used in this topology is low. However, the output voltage of this inverter is only two levels including positive and negative voltages without creating the zero voltage, which requires a large output inductor L2 and a filter. The inductor medium-type inverter [19] also called “Karschny” is another topology that is derived from the buck–boost topology. This inverter has a high reliability without capability of giving the reactive power to the grid and has four power switches in the current path at the same time, which will reduce the efficiency.

This paper introduces a new transformerless inverter based on charge pump circuit concept, which eliminates the leakage current of the grid-connected PV systems using a unipolar sinusoidal pulse width modulation (SPWM) technique. In this solution, the neutral of the grid is directly connected to the negative terminal of the charge pump circuit, so the voltage across the parasitic capacitor is connected to zero and the leakage current is eliminated. The

charge pump circuit is implemented to generate negative output voltage the modulation strategy of the proposed inverter because the leakage current is eliminated by the circuit topology. The pro posed topology consists of only four power switches, so the cost of the semiconductors is reduced and the power quality is improved by three-level output voltage in order to reduce the output current ripple. During operation of the proposed inverter, the current flows through two switches; thus, the conduction loss is also lower. The used dc voltage of the proposed inverter is the same as the FB inverter (unlike NPC, ANPC, and half-bridge (HB) inverters). The proposed inverter is capable of delivering reactive power into grid too. Thus, it can satisfy the require ment of the standard VDE-AR-N 4105. This paper is organized as follows. The charge pump circuit concept is explained in Section II. Based on it, a novel inverter topology is derived, and the modulation strategy and operation principles are described in detail. The current stress analysis of the switches, calculation of the power losses, and control scheme along with a compari son have been done in Section III. Experimental validations of the proposed grid-tied inverter is presented in Section IV, and finally, conclusions are given in Section V.

PROPOSED TOPOLOGY AND MODULATION STRATEGY

A.Charge Pump Circuit Concept

The concept of a simple charge pump circuit to be used in the proposed topology to generate the inverter negative output voltage is shown in Fig. 3. The circuit consists of two diodes (D1, D2) and two capacitors (C1, C2). This simple charge pump circuit gives a negative dc output voltage at the point of C equal to the voltage of point A [20]. The capacitor C1 is used to couple the voltage point of A to the node D. Two Schottky diodes D1 and D2 are used to pump the output volt age. When the diode D2 is forward biased, the capacitor C1 is charged by diode D2. The diode D1 is reversed in this state. When the diode D1 conducts, capacitor C2 is charged through the capacitor C1 by using node n and switch S2. In steady state, the output voltage of the negative charge pump circuit (vCn) can be derived by

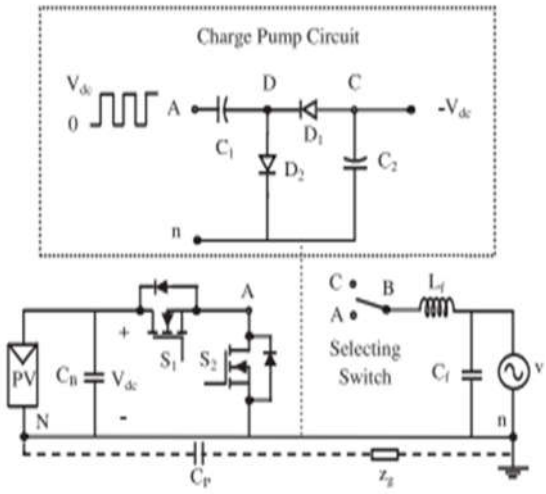

Fig. 3. Schematic diagram of the proposed inverter including the charge pump circuit.

$$v_{Cn} = -V_{dc} + V_{cut-in-D1} + V_{cut-in-D2} \quad (4)$$

where Vdc is the input voltage, Vcut−in−D 1 and Vcut−in−D 2 are the cut-in voltages of the diodes D1 and D2, respectively. For high power applications, these values can be negligible.

The above principle is integrated into the proposed inverter by using additional switching devices. The voltage difference between point A of the inverter to the point n is + Vdc or zero, according to the switching state of the S1 and S2, respectively. The voltage of C1 and C2 must be kept constant during all operation modes by selecting proper switching states. Point B must be connected to the points A or C with extra switches. This creates three different voltages, namely + Vdc, zero, and −Vdc for the inverter operation. In summary, the charge pump circuit in the transformerless inverter has the following characteristics for grid-tied applications.

1) This circuit has a common line with the negative terminal of the input dc voltage and the neutral point of the grid that causes the leakage current to be eliminated.

2) The charge pump circuit has no active device and it has a lower cost for grid-tied applications.

3) The capacitor of the proposed inverter charges every switching cycle, which reduces the size of the required capacitor with the switching frequency.

4) The capacitor of the charge pump circuit charges with a switching cycle that eliminates the pulse duration sensitivity to generate the negative voltage. B. Proposed Topology As shown in Fig. 4, the proposed topology consists of four power switches (S1 − S4), two diodes (D1, D2), two capacitors (C1, C2) based on the charge pump circuit

as described in Section II-A. An LCL-filter is used to eliminate harmonics of the output current.

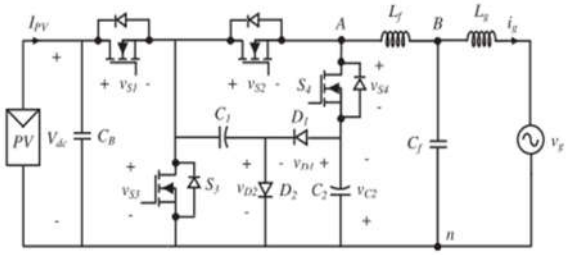

Fig. 4. Proposed single-phase transformerless grid-connected inverter

This new topology is modulated using simple SPWM. Fig. 5 shows the gate drive signals for the proposed inverter under the current lagging condition. According to the direction of the inverter output voltage and output current, theoperation of the proposed inverter is divided in four regions as shown in Fig. 6. These four different regions can be defined as follows.

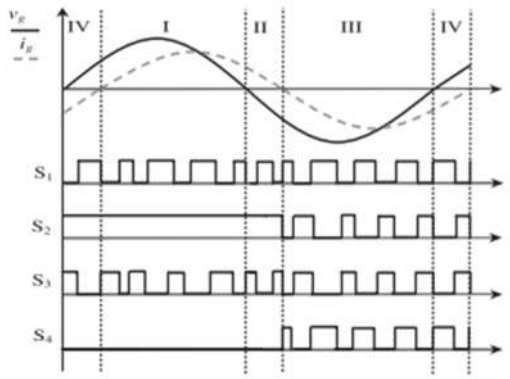

Fig. 5. Switching pattern of the proposed topology with reactive power flow.

1**) Region I:** the inverter output voltage and the output cur rent are positive; energy is transferred from dc side to grid side as shown in Fig. 6(a).

2) Region II: the inverter output voltage is negative and the output current is positive; energy is transferred from grid side to dc link as shown in Fig. 6(c).

3) Region III: the inverter output voltage and the output current are negative; energy is transferred from dc link to grid side as shown in Fig. 6(e).

4**) Region IV:** the inverter output voltage is positive and the output current is negative; energy is transferred from grid side to dc side as shown in Fig. 6(g). In the regions I and IV, the switches S1 and S3 will be ON and OFF with the switching frequency fs to produce positive and zero voltage while S2 remains ON for the whole positive half cycle.

When the switches S1 and S2 are ON, the output voltage of the inverter (vAn) will be + Vdc (positive state) as shown in Fig. 6(a) and (g). During this time interval, diode D1 is reverse biased and D2 is ON, so the capacitor C1 is charged through diode D2 and the voltage across the capacitor C2 maintains to be constant. In this state, when the switches S2 and S3 are ON, vAn will be 0 (zero state) as shown in Fig. 6(b) and (h).

In the zero state at positive cycle, the capacitors C1 and C2 are connected in parallel through D1. The capacitor C2 is charged by the capacitor C1 with negative polarities by the charge pump circuit to provide the negative voltage level.

In the regions II and III, the negative and zero voltage levels are produced. Fig. 6(c) and (e) shows the equivalent circuit that S4 and S1 are ON. The negative voltage is generated, when switch S4 is turned ON and the voltage across the capacitor C2 appears at the inverter output voltage (vAn = −Vdc) (negative state). The negative output voltage of the inverter is produced by the capacitor C2. In this state, S1 is switching simultaneously with S4. In addition to this, C1 is charged by the capacitor CB through S1 in order to maintain a constant voltage for the capacitor C1.

The voltage across the capacitor C1 can be kept constant in this state by the modulation strategy. In this period, the circuit operation of the zero state is similar to the zero state of positive half-period of the grid as shown in Fig. 6(b) and (h). Based on the analysis given above, three sequences exist for the output voltage and current of the proposed inverter. 1) If the sequence is I → III, then the inverter is in the unity power factor condition (PF = 1). 2) If the sequence is IV → I → II → III, then the inverter is in the current lagging condition. 3) If the sequence is I → IV → III → II, then the inverter is in the current leading condition. The aluminum electrolytic capacitors are used for the capacitors C1 and C2 of the proposed inverter in the experimental setup.

These capacitors have a limited life span because the electrolyte finally dissipates in to the element. Inrush current and voltage stress on the capacitors decrease the lifetime of them. Consequently, in order to reduce the equivalent series resistance (ESR) losses and to ensure the capacitor's lifetime, the capacitance of the aluminum electrolytic capacitors is chosen a little higher than the design values. One of the important elements in the capacitor design is the inrush current of the capacitors. In this case, the charging time constant of capacitor C2 (τC 2) can be expressed as follows:

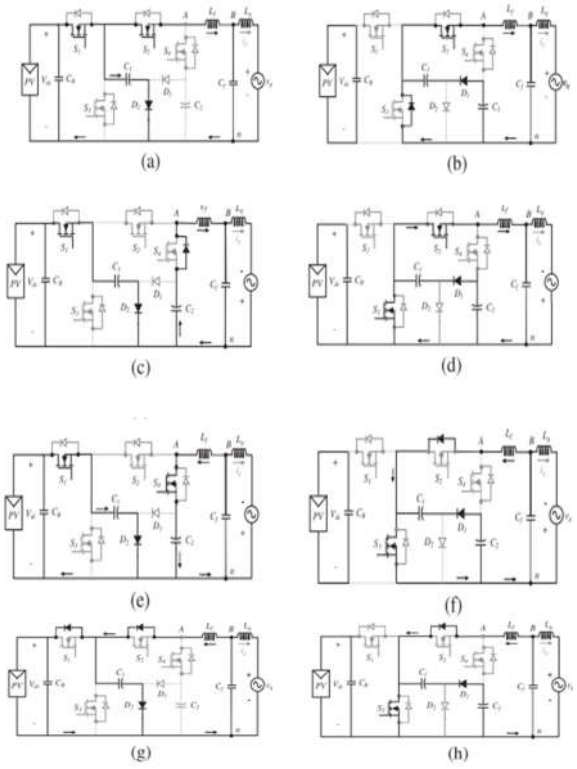

Fig. 6. Operational stages of the proposed inverter during (a), (b) re gion I, (c), (d) region II, (e), (f) region III, and (g), (h) region IV. (a) vAn = +Vdc , ig > 0. (b) vAn = 0, ig > 0. (c) vAn = −Vdc , ig > 0. (d) vAn = 0, ig > 0. (e) vAn = −Vdc , ig < 0. (f) vAn = 0, ig < 0. (g) vAn = +Vdc , ig < 0. (h) vAn = 0, ig < 0.

$$\tau_{C2} = R_{e1}C_{e1} \qquad (5)$$

where Re1 and Ce1 will be as follows:

$$R_{e1} = R_{D1} + R_{S3} + R_{C1} + R_{C2},\ C_{e1} = \frac{C_1 C_2}{C_1 + C_2} \qquad (6)$$

in which RC 1, RC 2 are the ESR of the capacitors, RS3 de notes the resistor of switch S3 in the conducting state, and RD1 represents the resistor of diode D1. The current through capacitors (iCapacitors) is calculated by

$$i_{Capacitors} = C_{e1}\frac{V_{C1} - V_{C2}}{\tau_{C2}} \qquad (7)$$

According to (5), the charging time constant of C2 is larger than its natural discharging time constant and VC 1 − VC 2 has a very small value in steady state. Due to these analyses and according to (7), the capacitor current value is small in this period and leads to an improvement in the lifespan.

ANALYSIS OF THE PROPOSED TOPOLOGY

A. Current Stress Analysis and Capacitors Design

A current stress analysis of the proposed topology is presented in this section. The maximum value of the current stress occur on the switches S1 and S3, because the capacitor C1 is charged through switch S1 and the capacitor C2 is charged through switch S3. Using the PSCAD software, simulation results of the current in the switches S1 and S3 for an output power of 500 W are shown in Fig. 7.

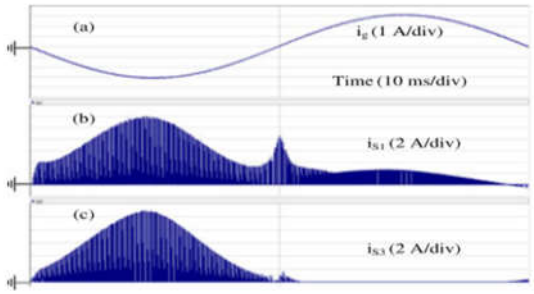

Fig. 7. Simulations of the current of switches: (a) grid current (ig) [1 A/div], (b) (iS 1) [2 A/div], and (c) (iS 3) [2 A/div].

The selected parameters of the simulations are the same as the experimental 500 W prototype. These parameters are listed in Table IV. The maximum value of the current in these switches occurs at the negative state in simulation results as shown in Fig. 7. In the negative half-period of the grid, the circuit shifts between the negative and zero states. During the negative state, the capacitor C1 is charged by the capacitor CB , while the capacitor C2 is discharged by the grid. As a result, the voltage values of the vC 2 − vC 1 and vCB − vC 1 are increased. When the circuit shifts to zero state, the capacitor CB is charged by the PV panel, whereas the capacitor C1 is discharged by the capacitor C2 in the paralleling mode.

Therefore, the voltage difference between the capacitors C1 and CB as well as the capacitors C1 and C2 is decreased. The equivalent circuits of the zero and negative states of the proposed topology for the current stress analysis are shown in Fig. 8(a) and (b), respectively. The power switches are modeled with a resistor (Rs) and a constant voltage source (von). The capacitor is considered as an ideal capacitor with a series resistor (RC), the PV panel is regarded as a current source (IPV), and the diode of the topology is modeled with a resistor (Rd). The forward voltage drop of the diodes is neglected.

According to the electric circuit theory, the grid voltage in series with a grid-side inductor (Lg) can be equivalent with the current source (ig) as shown in Fig. 8. The value of the capacitors C1 and C2 determines the max imum current of the power switches. The additional current on the switches S1 and S3 is created by the voltage differ ence between the capacitors C1, C2, and CB . So, by defin ing two variables vdiff ,1 = vC 1 − vC 2 − von and vdiff ,2 = vCB − vC 1 − von, the state equation for zero and negative states can be taken separately.

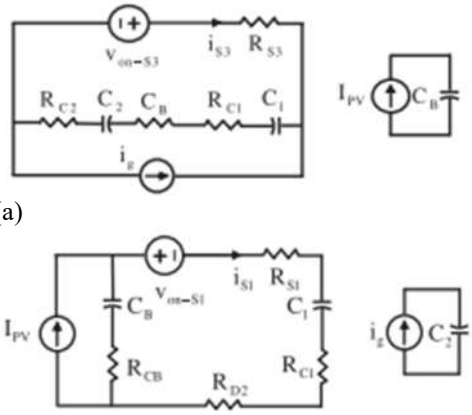

Fig. 8. Equivalent circuit of the proposed converter during (a) zero state and (b) negative state.

According to Fig. 8(a), at the zero state

$$\frac{dv_{diff.1}}{dt} = \frac{v_{diff.1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_{e1}} \quad (8)$$

$$\frac{dv_{diff.2}}{dt} = \frac{I_{PV}}{C_B} - \frac{v_{diff.1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_{e1}} \quad (9)$$

According to Fig. 8(b), in -ve state

$$\frac{dv_{diff.1}}{dt} = \frac{R_{Cb} I_{PV} + v_{diff.2}}{(R_{cb} + R_{e2}) C_1} + \frac{i_g}{C_2} \quad (10)$$

$$\frac{dv_{diff.2}}{dt} = \frac{I_{PV}}{C_B} + \frac{R_{Cb} I_{PV} - v_{diff.2}}{R_{e2} C_{e2}} \quad (11)$$

where in (8)–(11), Re2 and Ce2 will be as follows:

$$R_{e2} = R_{D2} + R_{S1} + R_{C1} + R_{CB}, C_{e2} = \frac{C_1 C_B}{C_1 + C_B} \quad (12)$$

By utilizing the averaging strategy at the switching cycle Ts, and linearizing (8)– (11), the normal estimation of iS 1 and iS 3 at the -ve and zero states is equivalent to (13) and (14), separately:

$$\frac{dv_{diff.1}}{dt} = (1 + s(t)) \left(\frac{v_{diff.1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_1} \right) - s(t) \left(\frac{R_{Cb} I_{PV} + v_{diff.2}}{(R_{cb} + R_{e2}) C_1} + \frac{i_g}{C_2} \right) \quad (13)$$

$$\frac{dv_{diff.2}}{dt} = (1 + s(t)) \left(\frac{I_{PV}}{C_B} - \frac{v_{diff.1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_1} \right) - s(t) \left(\frac{I_{PV}}{C_B} + \frac{R_{cB} I_{PV} - v_{diff.2}}{R_{e2} C_{e2}} \right) \quad (14)$$

where s(t) denotes the switching state function given as follows:

$$s(t) = \begin{cases} 1, & when\ the\ circuit\ is\ at\ positive\ state \\ 0, & when\ the\ circuit\ is\ at\ zero\ state \\ -1, & when\ the\ circuit\ is\ at\ negative\ state \end{cases} \quad (15)$$

Rearranging (13) and (14) and using the averaging method in switching cycle Ts, we have

$$\frac{d}{dt}\langle v_{diff.1} \rangle T_s - \frac{\langle v_{diff.1} \rangle T_s (1 + d(t))}{(R_{e1} + R_{s3}) C_{e1}} + \frac{\langle v_{diff.2} \rangle T_s d(t)}{(R_{e2} + R_{cb}) C_1} = -\frac{R_{s3} \langle i_g \rangle T_s (1 + d(t))}{(R_{e1} + R_{s3}) C_{e1}} - \frac{(R_{Cb} I_{PV}) d(t)}{(R_{e2} + R_{cb}) C_1} - \frac{\langle i_g \rangle T_s d(t)}{C_2} \quad (16)$$

$$\frac{d}{dt}\langle v_{diff.2} \rangle T_s + \frac{\langle v_{diff.2} \rangle T_s d(t)}{R_{e2} C_{e2}} + \frac{\langle v_{diff.1} \rangle T_s (1 + d(t))}{(R_{e1} + R_{s3}) C_1} = \frac{I_{PV}}{C_B} - \frac{R_{s3} \langle i_g \rangle T_s (1 + d(t))}{(R_{e1} + R_{s3}) C_{e1}} - \frac{(R_{Cb} I_{PV}) d(t)}{R_{e2} C_{e2}} \quad (17)$$

where d(t) and ig (t) are

$$d(t) = M \sin \omega t \quad (18)$$

$$i_g(t) = I_m \sin \omega t \quad (19)$$

where ω signifies the rakish frequency of O/P current, M is proportion of dc vtg and grid vtg, and Im speaks to pinnacle O/P current of inverter.

The normal current of iS 1 and iS 3 amid Ts feasible found as takes after:

$$\langle i_{s1} \rangle T_2 = \frac{\langle v_{diff.1} \rangle T_s + R_{s3} \langle i_g \rangle T_s}{R_{e1} + R_{s3}} \quad (20)$$

$$\langle i_{s3} \rangle T_2 = \frac{\langle v_{diff.2} \rangle T_s + R_{Cb} I_{PV}}{R_{e2}} \quad (21)$$

The simulation results of present coursing via the switches S1 and S3 for the O/P power 500 W are appeared in Fig. 7. The estimation of present that goes via S1 and S3 to reach to its greatest at the -ve state is appeared in this figure as well. At the -ve state,

$$\langle i_{s1,max} \rangle_T = \frac{1}{2} \left(\frac{C_1}{C_1 + C_2} + 1 \right) \left(\frac{M I_m}{1 - M} + \frac{T_s}{R_{e1} C_{e1}} \frac{1 - M}{2} \right) \quad (22)$$

$$\langle i_{s3,max} \rangle_T = \frac{1}{2} \left(\frac{C_1}{C_1 + C_B} + 1 \right) \left(\frac{M I_m}{1 - M} + \frac{T_s}{R_{e2} C_{e2}} \frac{1 - M}{2} \right) \quad (23)$$

Equations (22) and (23) indicate that the values of C1/(C1 + C2) and C1/(C1 + CB) should be calculated small enough, and the values of the Re1Ce1 and Re2Ce2 should be smaller than the switching period in order to minimize the current stress on the switches. Therefore, there is a tradeoff between the current stress on the switches and the size of the switched capacitors. To achieve these objectives, the capacitors C1, C2, and CB must be set to C1 < C2 and C1 < CB to reduce C1/(C1 + C2) and C1/(C1+CB), respectively.

The value of C1/(C1 + C2) and C1/(C1 + CB) is almost set to 1/4 by considering the capacitance of the capacitors, and hence, iS 1,max = 4Im and iS 3,max = 4Im . These values can be limited by a small resistor or a small inductor between the capacitors if needed. According to this analysis, the current flowing through the capacitors of C1 and CB has the same value of the current flowing through switch S3 and S1, respectively. The relationship between the voltage and current passing through the capacitors is calculated by

$$i_C = C\frac{\Delta v_C}{\Delta t} \qquad (24)$$

The required capacitance of C1 and CB for the proposed in verter can be derived by equaling the capacitor power magnitude to the grid power ripple magnitude. The capacitance C1 and CB can be calculated as follows:

$$C_{1or\,B} = \frac{I_{C1\ or\ B(\max)}}{(\widehat{V}_r V_n) f} \qquad (25)$$

where IC 1max and IC B max are the maximum current that passes through the capacitors C1 and CB , respectively. ∧V r, Vn, and f are the capacitor voltage ripple magnitude, nominal voltage on the capacitor, and the frequency during maximum current, respectively. By applying suitable values for these parameters in (25), the capacitance of C1 and CB is calculated.

B.CONDUCTION AND SWITCHING LOSSES OF POWER DEVICES

During the positive power cycle, the grid current flows through switches S1 and S2 and the capacitor C1 is charged through diode D2 at the positive state as shown in Fig. 6(a) and (g). At zero state, the grid current flows through S2 and S3 and the capacitor C2 is charged through diode D1. In this cycle, there are two switches on the grid current path and one diode is conducting in each state. In the negative cycle of the grid, the grid current flows through S4. The capacitor C1 is charged through diode D2 and switch S1 at the negative state as shown in Fig. 6(c) and (e). The voltage drop of the power devices can be derived by

$$MOSFET: v_{DS}(t) = i(t)R_{DS} \qquad (26)$$
$$Diode: v_{AK}(t) = V_F + i(t)R_{AK} \qquad (27)$$

where vDS is the drain source voltage drop of the MOSFET, RDS is the drain source resistance of the MOSFET during on the state operation, vAK is the anode cathode voltage drop of the diode, VF is the equivalent voltage drop under zero current condition of the diode, RAK is the anode cathode resistance of the diode during the on state, and i(t) is the grid current. The duty ratio of the conducting devices is given in Table I us ing the unipolar SPWM strategy in the proposed grid-connected inverter. The average value of the conduction losses of the MOS FET switch (PMOSFET Cond) during half of the fundamental period is calculated by

TABLE I
DUTY RATIO OF EACH CONDUCTING DEVICE

Semiconductor devices	Duty ratio (d)	
	Positive cycle ($v_g > 0$)	Negative cycle ($v_g < 0$)
S_1	$M\sin\omega t$	$M\sin\omega t$
S_2	1	$1-M\sin\omega t$
S_3	$M\sin\omega t$	$1-M\sin\omega t$
S_4	0	$M\sin\omega t$
D_1	0	$M\sin\omega t$
D_2	$M\sin\omega t$	0

$$P_{MOSFET.Cond} = \frac{1}{\pi}\int_0^{\pi} v_{DS}(t)i(t)d_{MOSFET}(t)d\omega t \qquad (28)$$

The average value of the conduction loss in the diode (PDiode Cond) during the on state mode is calculated by

$$P_{diode.Cond} = \frac{1}{\pi}\int_0^{\pi} v_{AK}i(t)d_{Diodes}(t)d\omega t \qquad (29)$$
$$\frac{1}{\pi}\int_0^{\pi}(V_F + i(t)R_{AK})\,i(t)d_{Diodes}(t)d\omega t$$

The aggregate conduction losses of MOSFET switches and diodes (PFurthered Cond) for the furthered inverter amid a fundamental period feasible computed from

$$P_{Proposed.cond} = P_{MOSFETs} + P_{diodes}$$
$$= 4\left(\frac{4MR_{DS}I_m^2}{3\pi}\right) + \left(\frac{R_{DS}I_m^2}{2}\right) + \left(R_{DS}I_m^2 - \frac{4MR_{DS}I_m^2}{3\pi}\right) + 2\left(\frac{MV_FI_m}{2} + \frac{4MR_{AK}I_m^2}{3\pi}\right)$$
$$= 3.1W \qquad (30)$$

The device manufacturer and circuit parameters for efficiency evaluation of proposed inverter are listed in Table II. In silicon carbide power MOSFET switches, the recovery cur rent of the diodes is eliminated and therefore the switching losses for the diodes are negligible. The switching losses of the MOSFET switch can be found as follows:

TABLE II
SPECIFICATIONS AND POWER DEVICES FOR EFFICIENCY EVALUATION

Parameters	Value
Input voltage	400 V
Grid voltage/frequency	220 V/50 Hz
Rated power	500 W
AC output current (RMS)	2.3 A
Switching frequency	24 kHz
Duty ratio (M)	0.78
MOSFET switches	C2M0080120D, $R_{DS} = 0.05\ \Omega$
Diode (D_1–D_2)	C3D10060A, $V_F = 0.7$ V, $R_{AK} = 0.01\ \Omega$

$$P_{MOSFET.sw} = f_{sw}E_{OSS}V_F \qquad (31)$$

where Eoss is put away energy that feasible accomplished from datasheet that is equivalent to 45 μJ. The aggregate switching losses of switches in furthered inverter feasible inferred as takes after:

$$P_{Total-sw} = 4f_{sw}E_{OSS}V_F = 3.46W \qquad (32)$$

C.Conduction Losses in the Capacitors

The ESR of the capacitors of the proposed inverter is achieved from aluminum electrolyte capacitor datasheets and it is divided into two parts. The first part of the conduction losses in the ca pacitors is similar to the conventional transformerless inverters including FB, H5, HERIC, etc. The second part of the conduc tion losses is related to the inrush current during the charging of the capacitors. These losses can be defined as follows:

$$P_{CAP.Cond.1} = \frac{2(R_{C1}+R_{CB})}{\pi}\int_0^{\pi} d_c(t)i_{S1}^2(t)d\omega t \qquad (33)$$

$$P_{CAP.Cond.2} = \frac{2(R_{C1}+R_{C2})}{\pi}\int_0^{\pi} d_c(t)i_{S3}^2(t)d\omega t \qquad (34)$$

where dc(t) is the duty ratio of the capacitor. The aluminum electrolytic capacitors are used in the experimental hardware. The simulation result of this loss with PSCAD software is totally around 3.1 W at 500 W prototype.

D.Control Scheme

The control strategy of the proposed grid-tied single-phase inverter is shown in Fig. 9. It contains two cascaded loops [21]: the first loop is an inner control loop, which has the responsibilities to generate a sinusoidal current and the outer control loop is implemented for the current reference generation, where the power is controlled. A proportional resonant (PR) controller provide an infinite gain at the resonant frequency (fres) and can eliminate the steady state error when tracking a sinusoidal signal, which is an index of power quality. Due to these features, the PR controller is selected instead of the FLC controller in the current control loop in this topology [22]. The transfer function of this controller can be found as follows:

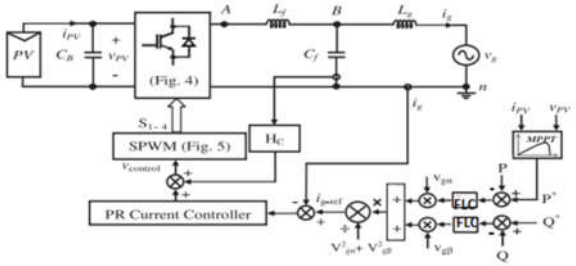

Fig. 9. Control block diagram of the proposed single-phase grid-tie inverter based on single-phase PQ theory.

$$G_{PR}(s) = K_p + \frac{2K_r}{s^2+\omega^2} \qquad (35)$$

where k p is the proportional gain, kr is the fundamental resonant gain, and ω is the resonant frequency. The power control loop requires orthogonal signal genera tion systems to create quadrature components (vgα, vgβ and i gα, igβ) corresponding to the grid voltage vg and grid current i g, and then it generates a current reference, which is used in the inner current control loop. According to the single-phase PQ theory [23], [24], the current reference can be produced by reg ulating the active and reactive powers. The active power (P) and reactive power (Q) for the proposed topology can be calculated by [24]

$$P = \frac{v_{g\alpha}i_{g\alpha} + v_{g\beta}i_{g\beta}}{2}$$
$$Q = \frac{v_{g\alpha}i_{g\alpha} - v_{g\beta}i_{g\beta}}{2} \qquad (36)$$

where v gα, vgβ , igα, and igβ are the α and β components of grid voltage and current, respectively. The active power and reactive power references (P∗ and Q∗) can be tuned by the operators {R– 3} or in the control unit, when the MPPT control is activated. The current reference can be computed in the αβ-reference frame, which simplifies the overall control. If PI controllers are used for power regulations, the grid current reference (ig-ref) can be derived as follows [24]:

$$i_{g-ref} = \frac{1}{v_{g\alpha}{}^2 + v_{g\beta}{}^2}[v_{g\alpha} \quad v_{g\beta}]\begin{bmatrix} G_p(s) & (P-P^*) \\ G_q(s) & (Q-Q^*) \end{bmatrix} \quad (37)$$

where G p(s) and Gq(s) are the PI controllers for active power and reactive power, respectively.

The LCL filter is adopted as the grid interfaced filter in this proposed topology. High output current quality in the proposed inverter can be obtained if the output filter is configured cor rectly. The first design consideration is the calculation of the filter parameters, which can be determined by current ripple and filter values [25]. The inverter-side inductor (Lf) value is calculated by considering 10–20% of the ripple on the output current, which is given by

$$L_f = \frac{(v_{dc} - v_{An})(M \sin \omega t)}{f_{sw}\Delta i_L} \quad (38)$$

where fsw is the switching frequency and ΔiL represents the peak-to-peak ripple current on the Lf . The inverter output volt age (vAn) can be calculated as follows:

$$v_{An} = MV_{dc} \sin \omega t \quad (39)$$

By replacing (39) with (38) and simplifying it, we have

$$L_f = \frac{(v_{dc})(RF)}{f_{sw}\Delta i_L} \quad (40)$$

where RF is the ripple current and can be calculated from

$$RF = M \sin \omega t - M^2 \sin \omega t^2 \quad (41)$$

The maximum achievable value of modulation index (M) is RFmax = 0.25 [26]. The maximum value of the filter capacitor is calculated by (42), limiting to be less than 5% of the nominal value [27]

$$C_{f,max} = \frac{0.05P_n}{2\pi f V_{rms}^2} \quad (42)$$

where Pn is the nominal power, Vrms denotes the root mean square (RMS) grid voltage, and f presents the grid frequency. There is a relation between the inverter-side inductor (Lf) and the grid side (Lg). This value is determined with the ratio be tween the ripple attenuation (r) as described in [28]

$$L_g = rL_f \quad (43)$$

The grid-side inductor (Lg) value feasible determined by

$$10f \le f_{res} \le 0.5f_{sw} \quad (44)$$

The resonant frequency for the LCL filter is given by

$$f_{res} = {}^1/_{2\pi}\sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \quad (45)$$

The second consideration is the current control strategy effec on the output filter design. In the closed-loop control system, the combination of L and C can cause a resonance problem, which may lead to instability of the controller. The active damping is used to smooth the resonance peak of the LCL filter as shown in Fig. 9 [29], [30]. A block diagram of the control system is shown in Fig. 10. The Bode diagram of the transfer function from vcref to ig is defined by G(s). This diagram is shown in Fig. 11 in order to demonstrate the effect of active damping by the filter capacitor current (Hcic)

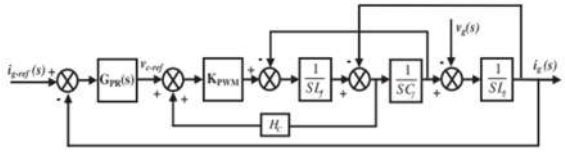

Fig. 10. Control diagram of the injected current with capacitor current feedback active damping.

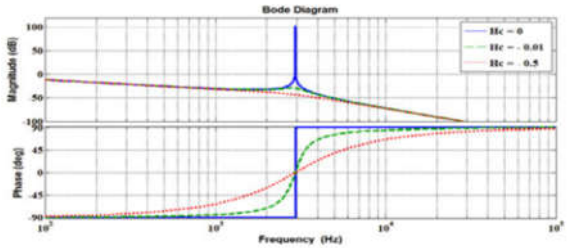

Fig. 11. Bode plot of the system in the case of different values for the active damping gain HC

$$G(s) = \frac{K_{PWM}G_1(s)}{1 + H_C K_{PWM} L_g C_f G_1(s) s^2} \quad (46)$$

where

$$G_1(s) = \frac{1}{sL_g + sL_f(1 + s^2 L_g C_f)} \quad (47)$$

and K pwm = 1 and HC is the active damping gain. The effec of HC is shown in Fig. 11, where a high value of HC shows better resonance peak damping capabilities.

E.Comparison With Other Known Topologies

A comparison of the transformerless inverter structures with respect to number of semiconductor devices, passive elements, THD of the current, and number of switches in the current path is listed in Table III.

TABLE III

comparison of the proposed topology with the conventional transformerless topologies

Converter	Semiconductor devices				Switches in the current path	THDi (%)
	Switches	Diodes	C	L		
H5	5	0	1	3	3	2
HERIC	6	0	1	3	2	1.9
CM in [31]	7	2	2	2	4	2.5
CM in [32]	6	0	3	2	3	2.8
CM in [33]	6	6	2	2	3	2.2
Proposed	4	2	3	2	2	2.1

This comparison includes conventional H5, HERIC inverter, and several common ground transformer less inverters like [31]–[33] with the proposed inverter. It can be seen from Table III that the proposed topology utilizes the least amount of active and passive components compared to the other topologies, which reduces the number of driver cir cuits, complexity of control, and power losses of the inverter. In this comparison, it is shown that the H5 and HERIC inverters are using extra switches to disconnect the grid side from the dc side, and this disconnection is incomplete due to the para sitic capacitance of switches. Therefore, the high-frequency CM current flows through parasitic capacitors. Thus, these topolo gies need extra filters to absorb the CM current according to Table III and the analysis given in Section I. Due to the con figuration of the charge pump circuit in the proposed topology, the CM current is completely eliminated without extra filters. In addition, the dc voltage used in the proposed inverter is the same as the conventional FB inverter, and only half of the dc voltage used in conventional HB, NPC, and ANPC inverters, while the performance in eliminating the CM current is better than the FB-based inverters. The THD of the grid currents for these topologies is listed in Table III. It can be seen that all the single-phase transformerless topologies have similar THD of the grid current.

The number of switches in the current path is related to the conduction losses. It can be seen from Table III that the num ber of switches in the current path and semiconductor devices of the CM inverter [31] are larger than the other topologies. Fig. 12 shows the power semiconductor losses distribution ac cording to the switching frequency at the rated power of all inverter topologies listed Table III with the same circuit param eters.

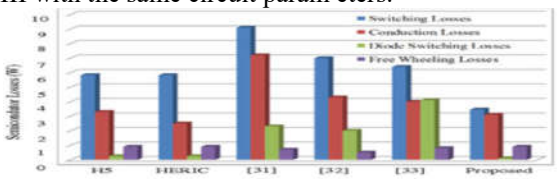

Fig. 12. Total semiconductor power losses distribution for the H5, HERIC, [31]–[33] and the proposed topologies at rated power.

The switching losses are calculated based on the datasheet of the devices. The calculation process is studied in detail in the literature [34]. The total semiconductor losses consist of the switching losses, conduction losses, switching losses of diode, and freewheeling losses. It is important to know that the con duction loss internal SiC diode of MOSFET implemented in the proposed inverter is less than the conduction loss of the IGBT body diode used in the H5, [31]–[33]. As shown in Fig. 12, the H5 and HERIC topologies have almost the same switching losses, because the number of high frequency switches is the same. The proposed topology has the lowest switching losses according to the analysis presented in Section III.

According to Table III, the conduction losses of [31] are high because many switches are used in the current path during the inverter oper ation. Freewheeling losses of all inverter topologies are almost the same. As a result, Shen et al. [31] have the highest total losses and the proposed topology has the lowest losses because of low switching and conduction losses at 500 W output power, which validate the theoretical analysis.

SIMULATION RESULTS

In order to verify the feasibility of the proposed topology, a 500 W, single-phase transformerless grid-tied inverter has been built in the laboratory and experimentally tested. The configuration and parameters used for the ex perimental tests are listed in Table IV. The experimental results of the proposed grid-connected inverter with unity power factor (PF = 1) operation are presented in Fig13. The grid voltage has the same phase as the injected grid current as shown in Fig. 13(a) and (b). Fig. 13(c) shows that the inverter output voltage vAn has three levels as + Vdc, 0, and −Vdc without the LCL-filter circuit. This determines that the proposed topology is

TABLE IV

PARAMETERS FOR THE 500 W PROTOTYPE

Parameter	Value	Parameter	Value
Power rating (P)	500 W	Capacitance (C_1)	220 μF, 500 V
Input voltage (V_{dc})	400V	Capacitance (C_2)	330 μF, 500 V
Output voltage (v_{Bn})	220 V (RMS)	L filter (L_f)	4 mH
Input capacitor (C_B)	470 μF, 500 V	C filter (C_f)	2.2 μF
Power switches ($S_1 - S_4$)	C2M0080120D, SiC MOSFET	L_g	2 mH
Diodes (D_1, D_2)	C3D10060A Schottky Diode	Switching frequency (f_s)	24 kHz

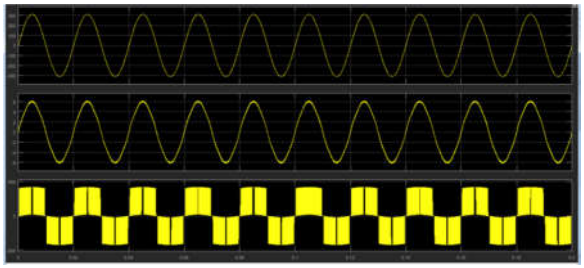

Fig. 13 Simulation results of the proposed topology with unity power factor (PF = 1) operation. (a) vg [500 V/div], (b) ig [5 A/div], (c) vA n [500 V/div], and (d) fast Fourier transform analysis of ig [50 V/div and 125 Hz/div].

modulated with unipolar SPWM. From Fig. 13, it is clear that the output current and voltage of the proposed inverter are highly sinusoidal with low harmonic distortion due to the three-level inherency of the output voltage. The current harmonic distribution is demonstrated in Fig. 13(d). It can be seen that the 5th-, 7th-, and 11th-order harmonics are very low and the output voltage and current of the topology are very close to be sinusoidal.

The experimental results for the THD measurement of the grid current are equal to 2.1% in unity power factor operation and it is lower than the recommended value by the IEEE STD 519- 1992 [35]. The RMS value of the current injected to the grid is equal to 2.3 A, and the output power is 500 W. Figs. 14 and 15 demonstrate the experimental results for the inverter operating under current lagging condition (PF = + 0.8) and leading condition (PF = – 0.8), respectively.

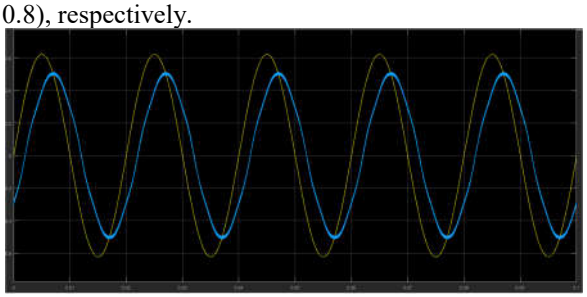

Fig. 14. Experimental results of the proposed topology with lagging power factor operation. (a) vg [500 V/div] and (b) ig [2 A/div].

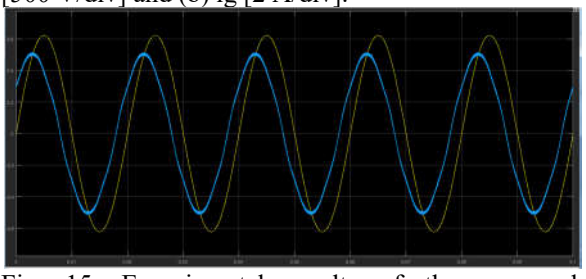

Fig. 15. Experimental results of the proposed topology with leading power factor operation. (a) vg [500 V/div] and (b) ig [2 A/div].

The partial enlargement of the grid current ig, grid voltage vg, and three level output voltage vAn is provided in Fig. 16. It is clear that the pulse duration of the output voltage (vAn) is in agreement with the switching frequency. The experimental results of the voltage across the switches S1, S2, S3, and S4 under 400 V input voltage conditions are shown in Fig. 18. The voltage stress of the switches S1, S2, and S3 is the same as the input dc voltage and on the switch S4 is double of the input voltage. The voltage stress of the capacitors and diodes is shown in Fig. 18. From the experimental waveforms of the output voltage, it can be seen that there are no voltage overshoots across the MOSFET switches.

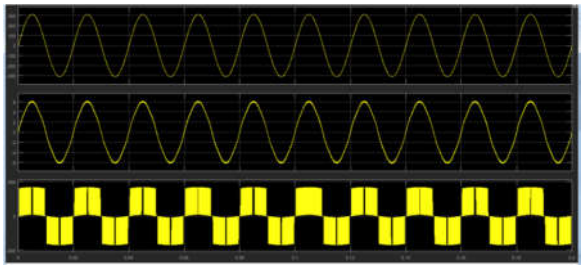

Fig. 16. Experimental enlarged results of the proposed topology. (a) vAn [500 V/div], (b) vg [250 V/div], and (c) ig [5 A/div], time [400 μs/div]

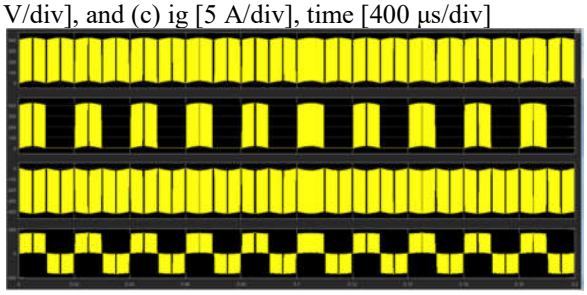

Fig. 17. Experimental results for drain source voltage of switches. (a) vS 1 [250 V/div], (b) vS 2 [500 V/div], (c) vS 3 [250 V/div], and (d) vS 4 [500 V/div].

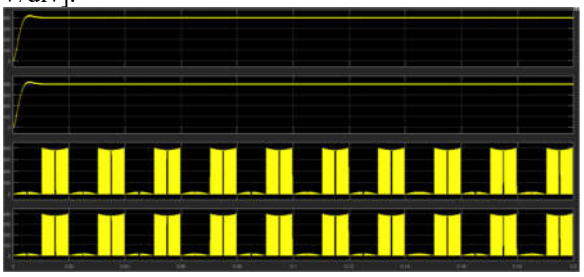

Fig. 19. Experimental results of the capacitor and diode voltages. (a) vC 1 [250 V/div], (b) vC 2 [500 V/div], (c) vD 1 [250 V/div], and (d) vD 2 [250 V/div].

Fig. 19 (a)–(c) shows the experimental waveforms of the grid voltage vg, the grid current ig, and the CM voltage vCM in the proposed topology. It can be seen that by applying unipolar mod ulation SPWM

strategy, the CMV of the proposed inverter has been kept constant. As a result, the CM current of the proposed inverter is eliminated due to the configuration of the charge pump circuit. Therefore, this solution with a charge pump cir cuit provides a new idea for using the proposed inverter for PV applications.

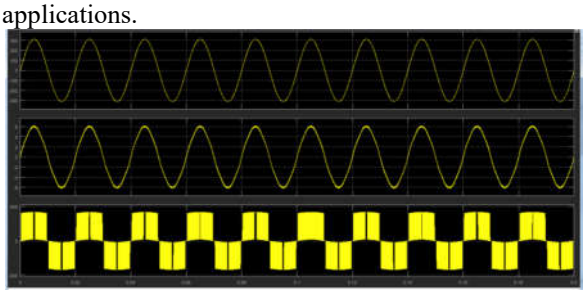

Fig. 19. Experimental results of the proposed topology. (a) vg [250 V/div], (b) ig [5 A/div], and (c) CMV [200 V/div].

The performance of the control strategy is confirmed by ap plying a step change to the proposed inverter. A PR current controller is adopted with ki = 2000 and kp = 20 as shown in (35). Fig. 20 shows the performance of the proposed inverter under the load step change. It has been demonstrated that the proposed inverter can track step change when the output power is decreased from 200 W to zero. As it can be seen, this test demonstrates the effectiveness of the power control strategy used in this paper in terms of fast response

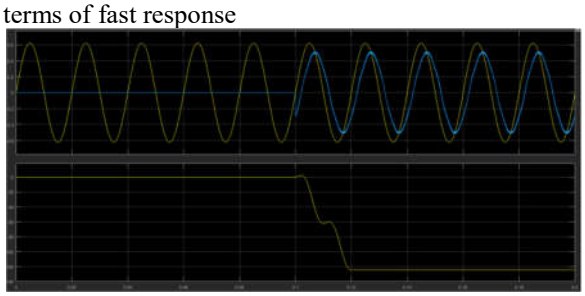

Fig. 20. Experimental results of the proposed topology in dynamic state. (a) vg [250 V/div], (b) ig [10 A/div], and (c) active power (P) [400 W/div]..

As described in the previous section, the efficiency of the pro posed inverter mainly relies on the losses of the power devices. Fig. 21 shows the efficiency of the H5, HERIC, [31]–[33] and the proposed inverter {R–2} having the same output power and unity PF. The efficiency comparison curves illustrate the exper imental results under the same dc-link voltages, output power, switching frequency, and 220 Vrms ac output voltage conditions. The only difference is the components. IGBTs are used in the H5, HERIC, [31]–[33], while SiC MOSFETs are used in the pro posed inverter. A VOLTECH PM300 power analyzer has been used to measure the efficiency of the proposed inverter. It may be noted that the efficiency diagram covers the total power device losses and the filter inductor losses.

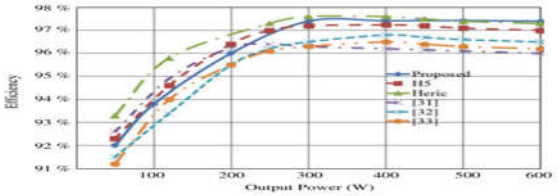

Fig. 21. Efficiency comparison for transformerless topologies under different output power and unit power factor.

The curves show that the HERIC has the highest efficiency for the low power applications but the leakage current characteristic is worse in comparison to the proposed topology. The efficiency of the proposed inverter is lower than the H5 and a little less than the HERIC topology at low power, while it is better at high power. The measured maximum efficiency of the proposed inverter is around 97.4% at 500 W. The experimental efficiency of the proposed inverter confirms the power loss calculation in Section III-B . As shown in (48), the California Energy Commission (CEC) efficiency is calculated combining different weighted factors at different output power levels [36]

$$\eta_{\mathrm{CEC}} = 0.04\,\eta_{10\%} + 0.05\,\eta_{20\%} + 0.12\,\eta_{30\%} + 0.21\,\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}. \quad (48)$$

The calculated CEC efficiency of the proposed transformer less inverter is 97.2%. As a result, the conduction loss in the semiconductors of the proposed inverter is similar to the H5 and HERIC inverters and the total device loss for the HERIC topol ogy at low power is higher than the proposed inverter. Hence, the proposed inverter reduces the output current ripple in addition to maintain a high efficiency without leakage current.

CONCLUSION

This paper proposed a new single-phase transformerless in verter for a grid-tied PV system using a charge pump circuit concept. The concept is proposed to generate the negative output voltage in the proposed inverter. This new topology generates a three level output voltage by employing unipolar SPWM. The negative terminal of the proposed topology is the same as the neutral line in the grid; thus, the leakage current is well sup pressed and the transformer is eliminated. The proposed topol ogy has also the ability to deliver reactive power into the grid. In addition, the proposed topology can be realized with a mini mum number of components; hence, a higher power density can be achieved with lower design cost. Compared to other existing

transformerless topologies, the performance depicted by the pro posed inverter is good. A theoretical analysis performed and it is validated by experimental results for a grid-connected inverter prototype. The proposed topology is verified with a 500 W pro totype. The maximum efficiency of the proposed inverter is mea sured to be 97.4%. Experimental results and loss calculations demonstrate the validity of the proposed inverter with lower THD for the grid-connected inverter. It can be concluded that the proposed topology is suitable for a grid-tied transformerless inverter.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid connected inverters for photovoltaic modules," IEEE Trans. Ind. Electron., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[2] X. Guo, R. He, J. Jian, Z. Lu, X. Sun, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," IEEE Trans. Power Electron., vol. 31, no. 3, pp. 1841–1846, Mar. 2016.

[3] W.-J. Cha, K.-T. Kim, Y.-W. Cho, S.-H. Lee, and B.-H. Kwon, "Evalu ation and analysis of transformerless photovoltaic inverter topology for efficiency improvement and reduction of leakage current," IET Power Electron., vol. 8, no. 2, pp. 255–267, 2015.

[4] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," IEEE Trans. Electromagn. Compat., vol. 52, no. 4, pp. 902–913, Nov. 2010.

[5] T. Bruckner, S. Bernet, and H. G ¨ uldner, "The active NPC converter and ¨ its loss-balancing control," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 855–868, Jun. 2005.

[6] D. Barater, E. Lorenzani, C. Concari, G. Franceschini, and G. Buticchi, "Recent advances in single-phase transformerless photovoltaic inverters," IET Renewable Power Gener., vol. 10, no. 2, pp. 260–273, 2016.

[7] W. Yu et al., "High-efficiency inverter with H6-type configuration for photovoltaic non-isolated ac module applications," in Proc. Annu. IEEE Appl. Power Electron. Conf. Expo., 2010, pp. 1056–1061.

[8] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid connected power system," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 752–762, Feb. 2012.

[9] F. Bradaschia, M. C. Cavalcanti, P. E. P. Ferraz, F. A. S. Neves, E. C. Santos, and J. H. G. M. da Silva, "Modulation for three-phase transformerless z-source inverter to reduce leakage currents in photovoltaic systems," IEEE Trans. Ind. Electron., vol. 58, no. 12, pp. 5385–5395, Dec. 2011.

[10] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual dc bus concept for cost-effective grid-connected PV power systems," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 793–805, Feb. 2013.

[11] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single phase transformerless photovoltaic inverters for leakage current suppression," IEEE Trans. Ind. Electron., vol. 62, no. 7, pp. 4537–4551, Jul. 2015.

[12] H. Schmidt, C. Siedlke, and J. Ketterer, "DC/AC converter to convert direct electric voltage to alternating voltage or current," U.S. Patent 7 046 534 B2, May 16, 2006.

[13] M. Islam and S. Mekhilef, "H6-type transformerless single-phase in verter for grid-tied photovoltaic system," IET Power Electron., vol. 8, pp. 636–644, 2015. [14] W. Yu, J. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET in verter with H6-type configuration for photovoltaic non isolated ac-module applications," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[15] W. Cui, B. Yang, Y. Zhao, W. Li, and X. He, "A novel single-phase transformerless grid-connected inverter," in Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc., 2011, pp. 1067–1071.

[16] M. Islam, N. Afrin, and S. Mekhilef, "Efficient single phase transformer less inverter for grid-tied PVG system with reactive power control," IEEE Trans. Sustain. Energy, vol. 7, no. 3, pp. 1205–1215, Jul. 2016.

[17] M. Islam and S. Mekhilef, "Efficient transformerless MOSFET inverter for a grid-tied photovoltaic system," IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6305–6316, Sep. 2016.

[18] N. Vazquez, M. Rosas, C. Hern ´ andez, E. V ´ azquez, and F. Perez, "A new ´ common-mode transformerless photovoltaic inverter," IEEE Trans. Ind. Electron., vol. 62, no. 10, pp. 6381–6391, Oct. 2015.

[19] Wechselrichter, German Patent DE 19642522 C1, Apr. 23, 1998.

[20] G. F. W. Khoo, R. H. Douglas, and R. A. McMahon, "Analysis of a charge pump power supply with a floating voltage reference," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 47, no. 10, pp. 1494–1501, Oct. 2000.

[21] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation sys tems," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[22] W. L. Chen and J. S. Lin, "One-dimensional optimization for proportional resonant controller

design against the change in source impedance and solar irradiation in PV systems," IEEE Trans. Ind. Electron., vol. 61, no. 4, pp. 1845–1854, Apr. 2014.
[23] M. Saitou and T. Shimizu, "Generalized theory of instantaneous active and reactive powers in single-phase circuits based on Hilbert transform," in Proc. 33rd Annu. IEEE Power Electron. Spec. Conf., 2002, vol. 3, pp. 1419–1424.
[24] Y. Yang, F. Blaabjerg, and H. Wang, "Low voltage ride-through of single phase transformerless photovoltaic inverters," IEEE Trans. Ind. Appl., vol. 50, no. 3, pp. 1942–1952, May/Jun. 2014.
[25] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaab jerg, "Evaluation of current controllers for distributed power generation systems," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 654–664, Mar. 2009.
[26] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3118–3128, Sep. 2010.
[27] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," IEEE Trans. Ind. Electron., vol. 57, no. 12, pp. 4106–4114, Dec. 2010.
[28] A. G. Matias, F. Alejandro, L. Piotr, C. Tomasz, D. Valcan, and P. Ale jandro, "Control of grid converter for wind turbines," Partial fulfillment of the requirements for M.S. degree, Aalborg Univ., Aalborg, Denmark, Groups PED-842, MCE2-830, 2009.
[29] R. P. Alzola, M. Liserre, F. Blaabjerg, R. Sebastian, J. Dannehl, and F. W. Fuchs, "Analysis of the passive damping losses in LCL-filter-based grid converters," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2642– 2646, Jun. 2013.
[30] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A new design method for the passive damped LCL and LLCL filter-based single-phase grid-tied inverter," IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4339–4350, Oct. 2013.
[31] J. M. Shen, H. L. Jou, and J. C. Wu, "Novel transformerless grid-connected power converter with negative grounding for photovoltaic generation system," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1818–1829, Apr. 2012.
[32] L. C. Breazeale and R. Ayyanar, "A photovoltaic array transformer-less inverter with film capacitors and silicon carbide transistors," IEEE Trans. Power Electron., vol. 30, no. 3, pp. 1297–1305, Mar. 2015. [33] Y. Wang and R. Li, "Novel high-efficiency three-level stacked-neutral point-clamped grid-tied inverter," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3766–3774, Sep. 2013.
[34] F. Hong, R. Z. Shan, H. Z. Wang, and Y. Yangon, "Analysis and calculation of inverter power loss," Proc. CSEE, vol. 28, no. 15, pp. 72–78, May 2008.
[35] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, IEEE Standard 519-1992, 1993.
[36] C. Liu, Y. Wang, J. Cui, Y. Zhi, M. Liu, and G. Cai, "Transformerless photovoltaic inverter based on interleaving high-frequency legs having bidirectional capability," IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1131–1142, Feb. 2016.

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