Design of Energy Efficient TCAM Based Search Engine using Priority Decision in Memory Technology P.Dakshyani¹, S.Mahaboob Subahan²

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Abstract: The energy efficient TCAM (ternary content -addressable memory) search engine uses the concept of high speed memory that searches its entire content in a single clock cycle. And this type of memory based search engine uses the three different types of inputs which are 0(low), 1(high), and x(don't care). The existing system of TCAM search engine uses the priority encoder (PE) to select highest priority match entry for resolving the multiple match problems. To protect against from the attacks such as spam and virus, the TCAM based search engine uses the expression matching across multiple packets of data. By using the concept of priority encoder, more energy is consumed by the pattern updates and search operations. To overcome this the proposed system of "Energy Efficient of TCAM Search Engine" uses the concept of Three phase search operation that utilize the length information of matched pattern to decide the longest pattern match data. Therefore this paper proposes a PDM (priority decision in memory) technology in order to eliminate the need of priority encoder and also uses the concept of sequential input-state (SIS) scheme to disable the mass of redundant search operations in state segments. Thus the PDM-based technology can improve energy consumption of TCAM when compared with normal priority encoder. Therefore, the proposed system of energy efficient TCAM search engine uses the 45nm CMOS technology and reduces its energy consumption of TCAMsearch engine and compared with area, power and delay.

Index Terms: Ternary Content Addressable Memory (TCAM), Priority Encoder, Priority Decision in Memory (PDM), Sequential Input-State (SIS) scheme.

I. INTRODUCTION

Phenomenal growth in the number of Internet users and the increasing popularity of bandwidth-hungry real-time applications has resulted in a demand for very high-speed networks. The Internet is a mesh of routers and switches, which process data packets and forwards them toward their destinations. A CAM can be used as a co-processor for the network processing unit (NPU) to offload the table lookup tasks. Recent applications of CAMs include real-time pattern matching in virus/intrusion-detection systems and gene pattern searching in bioinformatics. Since the capacities and word-sizes of CAMs used in most of these applications are much smaller than the CAMs used in networking equipment, the current CAM research is primarily driven by the networking applications, which require high capacity CAMs with low-power and high-speed operation. CAM is an outgrowth of random access memory (RAM). In addition to the conventional READ and WRITE operations, CAMs also support SEARCH operations. A CAM stores a number of data words and compares a search key with all the stored entries in parallel. If a match is found, the corresponding memory location is retrieved. In the presence of multiple matches, a priority encoder (PE) resolves the highest priority match. Recently, regular expression matching algorithms have been implemented in ternary content-addressable memory (TCAM)-based search engines for exploiting their parallel comparison and wildcard search abilities to achieve high speeds. Ternary content addressable memories (TCAMs) are hardware-based parallel lookup tables with bit-level masking capability. They are attractive for applications such as packet forwarding and classification in network routers. These TCAMbased search engines can be used to monitor patterns spread across multiple packets in a flow, because they run a unique state machine instance for each flow. To check the packet head (IP address/port number/protocol) and payload, the TCAM-based search engine is implemented in firewalls. Moreover, TCAM-based search designs can be used not only in network security of firewalls but also in broader applications, such as wireless sensor networks, biometrics, face recognition, and vehicle license plate recognition.

In this paper, we present circuit/architectture code sign techniques that can be widely used in decoupling 4 transistor 2 resistance (4T2R), to get pattern length information, which is encoded into the pattern data. We address several design issues, including how to get the longest pattern length for the matching entries, how to search the pattern length of matching entries that have the longest pattern length, and how to reduce energy consumption in search operations. In summary, the primary contributions of this paper are as follows.

1) We propose an energy-efficient TCAM search engine utilizing TCAM features to get mask length information from the pattern data, and discard the PE in priority-decision in memory (PDM) technology.

This resolves the ordering issue of patterns for energy reduction. These techniques do not require significant architectural modification.

2) We utilize a sequential input-state search scheme to significantly reduce unnecessary search operations in the state segment, thereby enabling search energy reduction. This technique does not alter the data flow during search execution, and hence does not cause any extra search operation.

3) We employ a circuit/architecture co-design to demonstrate that our proposed method is an attractive option for TCAM-based search engines in embedded systems because of its non-volatility, low dynamic energy, and low standby power.

II. EXISTING SYSTEM

In the existing system, the TCAM-based search engines need to maintain sorted lists with pattern lengths to resolve multiple matches. For this purpose a priority encoder (PE) is used. A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority encoder. Here we first explore the negative effect of a PE in a TCAM array and point out the unsuitability of conventional SRAM-based TCAM architectures that use PEs in an embedded system. Then, to show the limitations of implementation, we describe energy overhead for the use of PEs.

A. Limitations of Pattern Update

In TCAM-based search engines, the limitation of TCAM arrays is that pattern data have to be stored in order of lengths. Therefore, if a new pattern appears, then in order to keep the same order of pattern length, the shorter pattern, which compares to the new one, has to be reordered to the top entry in the TCAM array, to make space for the new one. The pattern table, both in the TCAM array and in the SRAM array, is difficult to update immediately, which considerably increase the overhead in energy consumption with a shuffle update. In our observations, as shown in Fig. 1, we find that the write energy increases with the pattern reorder ratio, which indicates that the percentage of the stored pattern data has to be made space and restored to keep the ordering of their lengths for additional pattern data.





Although nonvolatile TCAM (nvTCAM) based search engines can reduce the most leakage compared with SRAM-based TCAM search engines, the bulk of the energy consumption in nvTCAM based search engines is determined by the number of write operations, which is due to the high costs of the write operation.

B. Overhead of Energy Consumption

Furthermore, the focus of prior research in TCAM array is on how to mitigate the well-known issue of search operation overhead. However, based on the same restrictions, PEs are needed for multiple match selection. When the number of PEs grows as TCAM capacity increases, the energy consumption of PEs needs to be discussed. The simulation, which includes TCAM arrays and PEs, is done by HSPICE. The small and medium search count represents the average data usage in a given active ratio of light and medium Internet user, respectively. Fig.2 shows that SRAM-based TCAM search engines, which have high leakage power with increasing capacity, are not suitable for embedded systems. In contrast, the energy of TCAM array is also a significant part of the overall energy consumption in search engines. In addition, we cannot neglect the energy overhead of PE for all memory technologies. The percentage of PE energy in total energy consumption varies from 12% to 26%, depending on TCAM type, PE design, and search count. This shows that with increasing search count and capacity, the importance of the energy consumption of the PE as a fraction of overall energy becomes larger.



Fig.2. Search energy consumption in TCAM search engines

This result in slow update and increases energy consumption in update and search operations. On the other hand, high energy consumption in the TCAM array is really the most critical challenge for TCAM designers, because all entries of the TCAM are searched in parallel comparison, which causes a large amount of power dissipation in match lines (MLs) switching. Therefore, restrictions on the ordering of TCAM arrays and the high energy consumption of search operation are major issues in TCAM-based search engines.

Disadvantages

- More power consumption.
- More silicon area.
- More propagation delay.
- Not fixed the sub threshold level properly.

III. PRELIMINARIES

The proposed system presents a PDM (priority decision in memory) technology in order to eliminate the need of priority encoder in order to

disable the mass of redundant search operations in state segments. Thus the PDM based technology can improve energy consumption of TCAM when compared with normal priority encoder. Therefore, the proposed system of energy efficient of TCAM search engine uses the 45nm CMOS technology and reduces its energy consumption of TCAMsearch engine

RCSD-4T2R nvTCAMs have been designed to achieve small area and fast/low-power wake-up operations. Fig. 3 shows the circuit scheme for a resistive memory (RRAM)-based nvTCAM comprising two RRAM devices (RT/RB), two comparison transistors (NC/NCB), a write-control transistor (NWC), and an ML-driver transistor (NML).



Fig.3. Schematic of RCSD-4T2R nvTCAM cell

In the standby mode, word line, writevoltage-control and dynamic source line (DSL) are maintained at 0, and the ML is kept at a pre charge voltage (VPRE). Pre-charge of the power line voltages in a high voltage DC application is a preliminary mode which limits the inrush current during the power up procedure. A high-voltage system with a large capacitive load can be exposed to high electric current during initial turn-on. This current, if not limited, can cause considerable stress or damage to the system components. In some applications, the occasion to activate the system is a rare occurrence, such as in commercial utility power distribution. In other systems such as vehicle applications, pre-charge will occur with each use of the system, multiple times per day. Precharging is implemented to increase the lifespan of electronic components and increase reliability of the high voltage system.

After the pre charging operation, different search data are put on data lines to perform search operations. Several operations corresponding to the nature of the input nature are described as follows (summary in Table 1).

1) In the Search 1 operation, a DSL pulse is passed to node NX (output of RT/RB) through NC and RT. When RT is low resistance state (LRS) and RB is high resistance state (HRS) (cell data =0), VNX will exceed the threshold voltage of NML (VTH-NML)for a period TNX. NML will be turned ON and generate a large current to pull down ML voltage (VML). In this case, the search result is a mismatch. In contrast, if RT is HRS and RB is LRS (cell data=1) or RT is HRS and RB is HRS (cell data=X), low peak voltage (VNX-HRS) is generated at node NX for a period TNX. NML is in the cutoff region, because VNX-HR Sis below VTH-NML. Therefore, VML is kept near VPRE.

Table 1: Search o	perations in	RCSD-	4T2R
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Operation	Cell Data	V _{NX}	V_{ML}	Result	
6 1 1	0	>V _{TH-NML}	Low	Mismatch	
Search 1 (DL=1, DLB=0)	1	<v<sub>TH-NML</v<sub>	High	Match	
	Х	<v<sub>TH-NML</v<sub>	High	Match	
Search 0 (DL=0, DLB=1)	0	<v<sub>TH-NML</v<sub>	High	Match	
	1	>V _{TH-NML}	Low	Mismatch	
	Х	<v<sub>TH-NML</v<sub>	High	Match	
Masked inputs (DL=0, DLB=0)	0, 1, X	<v<sub>TH-NML</v<sub>	High	Match	
DL=1, DLB=1	0	>V _{TH-NML}	Low	Mismatch	
	1	>V _{TH-NML}	Low		
	Х	<v<sub>TH-NML</v<sub>	High	Match	

2) The Search 0 operation is very similar to Search 1 operation. When cell data are 0 or X, VML is kept near VPRE (match). In contrast, if cell data are 1, VNX will exceed the threshold voltage of NML to enable NML and ML will be pulled down (mismatch).

3) If data lines are masked inputs (DL =DLB=0), irrespective of whether the cell data are 0, 1, or X, 4T2R will behave the same as in the matched case. After the developing time of ML, the sense amplifier is turned ON to detect VML and generate a digital output.

4) In the last situation of Table 1, DL=DLB=1are useless inputs in 4T2R, because regardless of whether the cell data are 0 or 1, ML is always mismatched. This input cannot be used to search data in TCAM but we can utilize it to obtain pattern length information. The operation will be discussed

in more detail in proposed system. We, therefore, propose a new memory technology combined with TCAM array and PDM, which employs shuffle-free pattern data update and discards the PE to achieve update energy improvement. The proposed method utilizes the length information of the matched patterns to decide the longest pattern match unlike the existing solutions that use PEs to determine the match. Furthermore, we utilize a sequential inputstate (SIS) scheme to reduce the search energy generated by PDM and to reduce the search operations of the state segment.

IV. ENERGY EFFICIENT NONVOLATILE TCAM SEARCH ENGINES

Distinct advantages of nvTCAM over TCAM include low leakage and non volatility of the cell. In the proposed architecture, TCAM plus PDM technology is proposed to remove the restriction on ordering to employ shuffle-free pattern data update and discard the PE to achieve energy improvement. The proposed method utilizes the length information of the matched patterns to decide the longest pattern match unlike the existing solutions that use PEs to determine the match. In addition, the TCAM entry is physically partitioned into two isolated segments that use a different memory technology, because the input length is shorter than the state length, as shown in Fig. 4. This means that we can utilize a SIS scheme to improve the search energy generated by PDM and to reduce the search operations of the state segment (depending on the distribution of hex signatures of packets in applications).



Fig.4. Energy-efficient TCAM search engines.

A. Three-Phase Search Operation of Priority-Decision in Memory

Prior research shows that AS-TCAM search engines without PEs can reduce data update energy and propagation delay in PEs. A vertical logical operation with mask-encoded prefix-length has been proposed to remove the PE in search operations by using a two-stage comparison. However, the hardware overhead of this approach is a big constraint. More importantly, the abovementioned approaches are not suitable for implementation in nvTCAM search engines, because the pattern length is encoded into pattern data in a 4T2R cell unlike the pattern length of AS-TCAM cells, which is stored independently. Therefore, we do not get pattern length information directly from the 4T2R cell. Based on the above-mentioned methods, we propose a three phase search method that combines TCAM cells and PDM technology in each cell. Fig. 5 shows the functions of three phases in a TCAM array employed with the PDM method. The search function of the TCAM array is that each entry is parallel in comparison, as shown in Fig. 5(a). In the search operation, each bit of a search key is compared with the corresponding bit of stored data in the TCAM array.



Fig.5. Three phases of PDM.

However, multiple matches will result in search operation because of don't care bits (X). In Fig. 5(a), for example, four entries that contain pattern data and pattern length are stored in an arbitrary order in the TCAM entry. A parallel comparison is performed on the entries, and then, entries 1, 2, and 4 are matched with the search key 10100101. Next, a pattern length evaluation scheme operates corresponding bits from different pattern lengths in the matching entry. A feature can be observed from the mask data consisting of continuous "1"s and "0"s, as shown in Fig. 5(b).

The pattern length evaluation scheme uses pattern length of entries whose pattern data are matched with the search key to obtain the longest pattern length. As shown in Fig. 5(b), the longest pattern length is 11111100 evaluated by the pattern length evaluation scheme from the pattern lengths of entries 1, 2, and 4. Notice that the storage order does not affect the results. Finally, the longest pattern length is obtained from Phase 2. We can then find the longest pattern match entry having a pattern length that exactly matches the longest pattern length from Phase 2 by searching the matched entries from Phase 1 in a parallel comparison. Fig. 5(c) shows a search of the pattern lengths of entries 1, 2, and 4 by the longest pattern length (11111100) and that the resulting exact match of the pattern length of entry 2.

Therefore, we can evaluate the longest pattern match entry in an arbitrarily ordered array by using PDM technology. The operation of the circuit design will be discussed in more detail in next section.

B. 4T2R plus Priority-Decision in Memory

A typical 4T2R plus PDM method consists of three major components, as shown in Fig. 6. The first component is a 4T2R cell that is used to store the pattern data and compare the stored pattern with the search key. The second component is the necessary evaluation logic to find the longest pattern length of matching pattern entries. Fig. 6(a) shows that two NMOS transistors are placed in series to implement this circuit, which is controlled by the NX and ML result from the 4T2R cell.

The third component is a pattern length comparison scheme, which is used to find the longest pattern match entry by searching the matched entries for an entry that contains the longest pattern length.



Fig.6. 4T2R plus PDM – (a) finding the longest pattern length by the pattern length evaluation scheme, (b) longest pattern length searching in the pattern match entries

The pattern length comparison scheme consists of four transistors containing parallel comparison circuits in which the second search operation of the pattern length is performed.

1) Search Match Pattern Data: Fig. 7 shows the circuit design of a 4T2R plus PDM method, which includes a 4T2R cell, a pattern length evaluation, and a pattern length comparison circuit. In this phase, the circuit operations are the same as previously described. In other words, the original 4T2R TCAM cell is not modified. Although we cannot use DL =DLB=1 to search data in the cell, this input can indicate whether data are care or don't care. We utilize this feature to find the longest pattern length.

2) Find Longest Pattern Length: The purpose of Phase 2 is to find the longest pattern length in the matching entries whose pattern data match the search key in Phase 1. At the beginning of Phase 2, column mask data line (CMD) is pre charged to VPRE and the control signals are put on data lines (DL =DLB=1) to perform the pattern length evaluation. When DL =DLB=1, cell data can identify whether these data are in the "0" or "1" state. If cell data are "0" or "1" state (NX =1), VNX will exceed the threshold voltage of NM (VTH–NM). When DL =DLB=1, cell data can identify whether these data are in the "0" or "1" state. If cell data are "0" or "1" state (NX =1), VNX will exceed the threshold voltage of NM (VTH-NM).



If, simultaneously, the result of Phase 1 result (P1R) is a mismatch, first search transistor (NFS) will be turned OFF to keep near VPRE in CMD. In addition, if the cell data are don't care (NX=0), a low peak voltage (VNX–HRS)is generated to cutoff NM due to VNX–HRS being below VTH–NML. Therefore, VCMD is kept near VPRE whether the entry of Phase 1 is a match or not, as shown in Table 3.4. As long as the pattern length bit in the column of matching entries is "0" or "1" state, VCMD will be pulled down to ground. The pattern length evaluation is operated in each bit and the results are output to the register for Phase 3.

Table 2: Find Longest Pattern Length in Phase 2

Operation	Data	(RT, RB)	V _{NX}	NM	Phase 1/NFS	CMD
	٥	(I DC LIDC)		<u>On</u>	Match/On	0
	0	(ско,пко)	- V TH-NML	Uli	Mismatch/Off	1
Phase 2	1			0.	Match/On	0
(DL=1, DLB=1)	I	(пкэ,скэ)	✓ V TH-NML	On	Mismatch/Off	1
000 1)	v		-V	Off	Match/On	1
	A (IIKS, IIKS) VTH-NML UI	UII	Mismatch/Off	1		

3) Search for the Longest Pattern Match: The target of Phase 3 is to find the longest pattern match entry in the TCAM by using match entries from Phase 1 and longest pattern length from Phase 2. At first, mask MLs (MMLs) of the matching entries are pre charged to VPRE. After the pre charging operation, the control signals are put on data lines (DL= DLB=1) and Phase 2 result (P2R) from the register is applied to perform the pattern length compare operation. All scenarios are summarized in Table 3.

Table 3: Find Longest Pattern Length in Phase 3

Operation	Data	(RT, RB)	V _{NX}	Phase 2 /PSS	MX	MML
	0	(LRS,HRS)	>V _{TH-NML}	"0" or "1" /On	101 111 0 N	Match
	1	(HRS,LRS)	>V _{TH-NML}		0	Maten
Phase 3	Х	(HRS,HRS)	<v<sub>TH-NML</v<sub>		1	Mismatch
(DL=1, DLB=1)	0	(LRS,HRS)	>V _{TH-NML}	don't care /Off		N/A
,	1	(HRS,LRS)	>V _{TH-NML}		N/A	
	Х	(HRS,HRS)	<v<sub>TH-NML</v<sub>		0	Match

When the P2R and cell data are "0" or "1," second-search transistor (PSS) and mask-search transistor (NMC) will be turned ON but masksearch controller (PMC) will be turned OFF. Therefore, MX will be pulled down to ground to disable MML-driver transistor (NMML) and MML is kept near VPRE. If P2R is "0" or "1" state but cell data are don't care, PSS and PMC will be turned ON but ZNMC will be turned OFF. MX will rise to VDD to enable NMML and MML is pulled down to ground. If P2R and cell data are don't care, PSS and NMC will be turned OFF, followed by PMC, then MX will disable NMML to keep MML near VPRE. Otherwise, there is no situation of the matching entries in which, simultaneously, the P2R is don't care and cell data are "0" or "1" because that would violate the meaning of the longest pattern length. According to the above-mentioned description, we can find the longest pattern match entry in the TCAM array by using PDM technology. Therefore, new pattern data can be inserted in any TCAM entry with no sorting requirement for the pattern data and regardless of the pattern length.

V. SEQUENTIAL INPUT STATE-SEARCH SCHEME

One challenge in implementing TCAM-based search engines is to identify the energy overhead of search operations that negatively impact system energy. We know that most of the energy overhead is caused by the frequent charging and discharging of highly matched lines in a TCAM array. In prior studies, the segmented ML scheme is a well-known and very useful technique to efficiently reduce energy consumption in TCAM-based search engines. A ripple pre charge TCAM was proposed to selectively pre charge the highly matched lines to efficiency reduce energy consumption in packet classifiers; the four most significant bits of the destination address in packets can determine 80% of the prefix mismatches. In addition, there are more than 60% opportunities to reduce search operations in the vehicle license plate recognition. As mentioned before, we know that the input length in a TCAM entry is shorter than the state length, so the search operations of the state segment are disabled whether the search operations in input segment are mismatched or not. To reduce dynamic energy, we need to disable the state segment if the search of input segment is mismatched. We, therefore, analyze the distribution of hex signatures in a Clam AV virus database to propose a SIS search scheme to improve energy consumption in TCAM search engines. Fig. 8 shows that on average, about 93.75% of search operations in the state segment are redundant and can be skipped without changing the final search result.



Fig.8. Distribution of hex signatures in input segment.

Precharging is implemented to increase the lifespan of electronic components and increase reliability of the high voltage system. Due to this significant amount of needless search operations, there is, therefore, great potential to use the SIS scheme for energy reduction in the proposed TCAM search engines. Fig. 3.9 shows that we propose a state search driver to support the proposed SIS scheme, which is used to reduce the search operation of the TCAM entries in the state segment.



Fig.9. Scheme of sequential input-state search

In the proposed SIS scheme, if the search result of the TCAM entry in the input segment is matched, the pre charge circuit of state segment will be enabled, and then, the corresponding TCAM entry of the state segment will be searched. In contrast, when the search result of the TCAM entry in the input segment is mismatched, the search operation of the corresponding TCAM entry in the state segment will be disabled. The general evaluation of search state segment is described in Table 4.

 Table 4: Evaluation of Search State

 Segment

Pre-Charge Control	ML	Search state segment?
Low	High	Yes
High	Low	No
High	High	No
Low	Low	No

Although the proposed SIS scheme needs extra circuits to reduce the search operations in the state segment, it becomes an attractive option for energy saving, because the significant amount of needless search operations is disabled.

VI. SIMULATION RESULTS

The energy efficient in ternary content addressable memory is designed and simulated in Tanner EDA Tool. The schematic diagrams of proposed system are first presented, followed by the Test Bench structure of the proposed system. The waveforms of proposed system are observed in W Edit and the results of Power consumption and simulation time are given in T-Spice.



Fig.10. Schematic of 4T2R plus PDM



Fig.11. Schematic of 8bit 4T2R Plus PDM



Fig.12. Testbench of 4T2R Plus PDM



Fig.13. Testbench of 8Bit 4T2R Plus PDM



Fig.14. Output Waveforms of 4T2R Plus PDM



Fig.15. Output Waveforms of 8Bit 4T2R Plus PDM

* BEGIN NON-GRAPHICAL DATA

Power Results UVDD from time 0 to 1e-005 Average power consumed -> 3.240000e-012 watts Max power 3.240000e-012 at time 0 Min power 3.240000e-012 at time 0 * END NON-GRAPHICAL DATA * Parsing 0.00 seconds * Setup 0.00 seconds * DC operating point 0.00 seconds * Transient Analysis 0.31 seconds * Overhead 1.09 seconds * ----* Total 1.40 seconds * Simulation completed with 2 Warnings * End of T-Spice output file

Fig.16. Power report of 4T2R Plus PDM

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Power Results
UVDD from time 0 to 1e-005
Average power consumed -> 3.240000e-012 watts
Max power 3.240000e-012 at time 0
Min power 3.240000e-012 at time 0
* END NON-GRAPHICAL DATA
* Parsing
                               0.01 seconds
* Setup
                               0.00 seconds
 DC operating point
                               0.01 seconds
* Transient Analysis
                               0.31 seconds
* Overhead
                               0.53 seconds
* -----
* Total
                               0.87 seconds
* Simulation completed with 8 Warnings
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* End of T-Spice output file

Fig.17. Power report of 8Bit 4T2R Plus PDM

VI. CONCLUSION

In this paper the energy-efficient based TCAM search engine using methodology of Priority Decision in Memory is presented. This system overcomes the drawbacks such as more energy consumption for pattern updates and search operations that are encountered in exiting system which uses priority encoder. А simple memory modification based on PDM method is proposed as an alternative, which can be widely used in TCAM-based designs. It can improve update energy efficiency and update pattern table quickly, because pattern data can be stored in an arbitrary order by discarding the PE. Here in addition to this we use an SIS scheme for disabling the mass of redundant search operations in the state segment to reduce energy consumption. We also demonstrate that the PDM method and the SIS scheme are attractive options for designing energy efficient search engines in embedded systems. This system is designed in both single-bit and 8-bit architectures, which witnesses the employing of system in further work. Both systems are designed and simulated in Tanner EDA where its porformance and power consumption are also presented.

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