Comparative Analysis of Multilevel Inverter Topologies with Reduced device Count

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Abstract—

Multilevel inverter topologies are used in industrial power applications without use of transformers and filters. paper proposes multilevel inverter topologies: the topologies are nine level CHB multilevel inverter and two nine level hybrid multilevel inverter topologies. This paper comparative analyses the total blocking capabilities, no of switching pattern, conduction duration & variation switch of multilevel inverter topologies. The performance of the Multilevel Inverter is increased by using the embedded switching pattern. This inverter produces the pulses by using the embedded controller. This scheme reduces the switching loss. These proposed topologies have the ability of producing the high quality output voltage which is nearer to the sinusoidal waves .Simulation is performed using MATLAB/ SIMULINK. © 2014. In this paper various Multi level inverter topologies with reduces power switch count are reviewed and analyzed. Topologies are analyzed, based on both(qualitative & quantitative) parameters and a detailed comparison of these topologies as presented

Index Terms— **power distribution, fundamental switching frequency operation, Blocking capabilities ,conduction switching, multilevel inverters (MLI), reduced device** count **, source configuration.**

I. INTRODUCTION

DC to AC power conversion technology in the modern set-of generation, transmission, distribution and utilization of electric power. Nowadays Multilevel inverters are becoming one of the industrial solutions for DC power source utilization (such as electricity obtained from batteries, solar panels or fuel cells) [1-2-3], high dynamic performance and power-quality demanding applications covering a power range from 1 to 30 MW [3–7-8]. They play a crucial role in variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, active filters and flexible AC transmission systems applications. Multilevel inverters are three types.

Diode clamped MLI , Flying capacitors MLI ,Cascaded H- bridge MLI can withstand for important applications like hybrid electric vehicles, reactive power compensation , , uninterruptible power supplies and regenerative applications. With recent advent of power electronics devices, digital controllers and sensors, the role of power inverters also envisaged and acknowledged in frontiers such as futuristic smart grids and renewable energy sources based power generation [9]. A multilevel inverter is basically a power electronic interface that produces a desired output voltage by connecting various DC sources and switches in the appropriate manner [9-10]. The basic concept of an MLI to achieve higher power is to use switching devices (power semiconductor switches) like IGBTs, MOSFETs, etc. along with appropriate DC voltage sources to perform the power conversion by synthesizing a staircase voltage waveform. batteries, and renewable energy voltage sources can be used as the multiple input DC sources. This paper reviews new topologies of MLI s that have semiconductor switches and gate driver circuits with higher number of steps in the output including the generation of 9 level multilevel inverter output waveform using switches with Symmetric and Asymmetric topology, DC sources and Reduced Device Count Multilevel Inverters (RDC-MLI) topologies.

II. TOPOLOGIES

Topologies are reducing the number of controlled switching
power semiconductor devices for a given number of phase Type of RDC-MLI Topologies are:

1) Cascaded half-bridge-based multilevel dc-Link (MLDCL) inverter [5]-[12].
2) series-connected switched sources (SCSS)-based MLI [17], [18];
3) reversing voltage (RV) topology [22], [11];
4) multilevel module (MLM)-based MLI [7];

While a detailed analysis of these topologies is presented in Section , it is important to appreciate that there are several similarities between the different RDC-MLI topologies which can be clearly seen if they are drawn with a similar structure,

III. REVIEW OF MLI TOPOLOGIES WITH REDUCED DEVICE COUNT

1. Cascaded Half-Bridge-Based MLDCL Inverter

The circuit diagram of the cascaded H-bridge multilevel DC-link inverter topology shown in Figure 1 consists of multilevel DC-link voltage source inverter. Figure. a diagram of the presented cascaded H-bridge MLDCL inverter topology Various modes of switching sequence is given in the table 1 to produce DC bus voltage Vbus with the shape of staircase with (n=4) steps, where n is the number of cell sources the MLDCL inverter can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases [8].With various valid switching combinations that can be used to obtain the MLDCL voltage vbus(t) are summarized in Table I .It can be observed from Table I that to obtain a given level, four switches conduct simultaneously for the pulse generation part and two switches conduct for the pulse-generation part (switches MOS 8 and MOS10 for the positive half cycle, Q9 and Q11 for the negative half cycle, and MOS 8,9,10,11 for the zero level).It can be observed from the topology that each power switch of repeating sequence part must possess a minimum voltage blocking capability equal to the sum of the input voltage values. Thus, these switches are rated higher as compared to the switches in the part. However, since the zero level can be synthesized using switches of the polarity-generation part, the higher rated switches MOS = 1 to 4} can be operated at fundamental switching frequency.For a symmetric source configuration with VDC,1 = VDC,2 = VDC,3 = VDC,4 = VDC, it can be observed that the switches Sj {j = 1 to 8} need to block a voltage of VDC and need to conduct a current equal to the load current while the switches mos = 1 to 4} need to block a voltage equal to 4VDC and conduct a current equal to the load current. Moreover, it can be observed from Table I that since voltage levels VDC, 2VDC, 3VDC, and 4VDC can be synthesized combining all the input sources in groups of one, two, and three, respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing the trinary source configuration cannot be employed for this topology. As it can be observed from Table I, a binary source configuration with VDC,1 = VDC, VDC,2 = 2VDC,VDC,3 = 4VDC, and VDC,4 = 8VDC is possible .

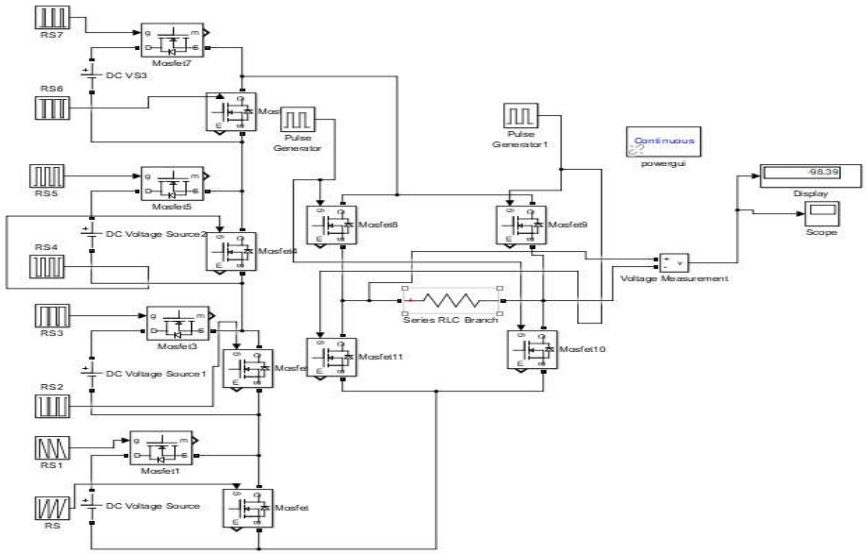

Fig.1.1 MATLA/ Simulink model of MLDCL topology for nine level inverter in which valid switching combinations for the "SCSS-MLI" is shown.

Table -1.1

State	V_{BUS}(t)	Switching in ON State
1	V_{dc1}	S_2,S_3,S_5,S_7
2	$V_{dc1}+V_{dc2}$	S_2,S_4,S_5,S_7
3	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2,S_4,S_6,S_7
4	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_2,S_4,S_6,S_8
5	0	S_1,S_3,S_5,S_7

Table -1.2

MLDCL BASED MLI		
Blocking Capabilities of MLDCL Based mli		
S .No	Switch No	Voltage
1	S1=S2=S3=S4=S5=S6=S7 =100V	Equal voltage blocking
Conduction switch and Variation switch of MLDCL Based MLI		
S.no	Switch No conduction duration	Calculation in (t) sec
1	for S1	0.000559 sec ,1 x10^{-7} sce,8.57 x10^{-4} sec
2	for S2	8.57 x10^{-3} sec
3	for S3	0.001229 sec , 8.16 x10^{-3} sec
4	for S4	7.109 x10^{-3} sec
5	for S5	0.002263 sec ,2.4639 x10^{-3} sec
6	for S6	9.8 x10^{-3} sec
7	for S7	0.003129 sec ,3.42 x10^{-3} sec.
8	for S8	3.449$10^{-3}$ sec.

1.1 Waveform

The switching signals shown in Figure 1.1 are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage Vbus for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels, whose voltages are -(V1+V2+.....+ Vn) , -(V1+V2+.....Vn-1).....,-V2, -V1 ,0, V1, V2,.....(V1+V2+....Vn-1), (V1+V2+....Vn). Where V1, V2.....Vn are voltages of cell sources. The desired AC output voltage (V bus)an of cascaded H-bridge is shown in the Figure 1

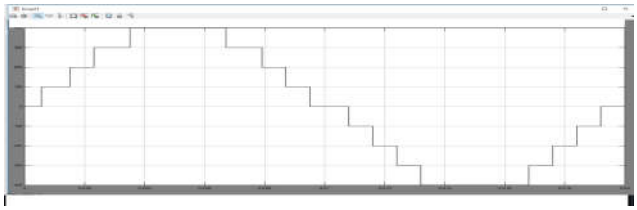

Fig-1.2 waveform of mldcl inverter

1.2 Number of Switching Devices

MLDCL are consisting the No of DC I/P voltage source of switching devices required =2n+4 & no of voltage levels generated =2n+1.

1.3Total voltage blocking Capacity

The MOSFET switches are triggered by proper switching signals to produce multi level DC-link bus voltage Vbus. Multilevel DC-link voltage source consists of 8 switches named S1 –S8. The cell source is bypassed with S1on and S2 off, or adds to the DC link voltage by reversing the switches. Based on this principle the switches in four cells can perform PWM if necessary or switching the switches at twice the fundamental frequency of output voltage. The switching patterns of a controlled switch are

given in the Table 1.2 . to produce DC bus voltage Vbus with the shape of stair case with (n=4) steps, where n is the number of cell sources output voltage

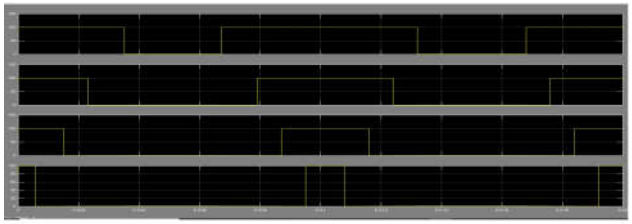

Fig:-1.4 Total voltage blocking capabilities

1.4 Conduction duration & Variation switches

Conduction duration Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 4. Table 2 gives the sequence of closure and opening of switches. Based on switching sequence of the switches suitable program has written and burned to the AT89c51 microcontroller for producing triggering pulses for the MOSFETs in the MLDCL voltage source .

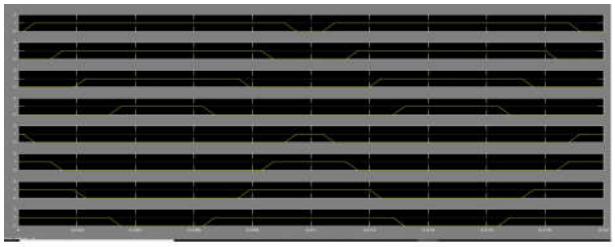

Fig 1.5 Conduction duration & variation switch

2. Series-connected switched sources (SCSS)-based MLI

A modified form of SCSS topology objective of reducing the no. of switch as compared to the classical CHB topology .the topology with four i/p DC source V_{dc} [1- 4] is shown in fig.1 the low potential terminal of the sources are all connected through power switch .these terminal are also connected the higher potential terminal of the processing sources through power switch as illustrated in fig with s/w [1-8].this interconnection is capable of synthesizing a multilevel rectified waveform V_{bus}. Which is imparted +ve & -ve polarities using using the H bridge comparising s/w MOS [1-4]. The possibilities of synthesizing various s/w combination of I/P dc level are summarized in table 1 .it can seen that the structure through simple allows a much no of valid state infect not even the i/p DC level offered by the sources can all be obtained as V_{bus}. Except that the V_{dc}. Thus this topologies does not offer any possibility of employing asymmetric sources configuration .the source configuration mandatory need to be symmetric i.e. V_{dc1} =V_{dc2} = V_{dc3} = V_{dc4} = V_{dc} .which such a configuration various s/w would be differently voltage rated s/w mos [1-4]should be minimally rated at 4 V_{dc}.

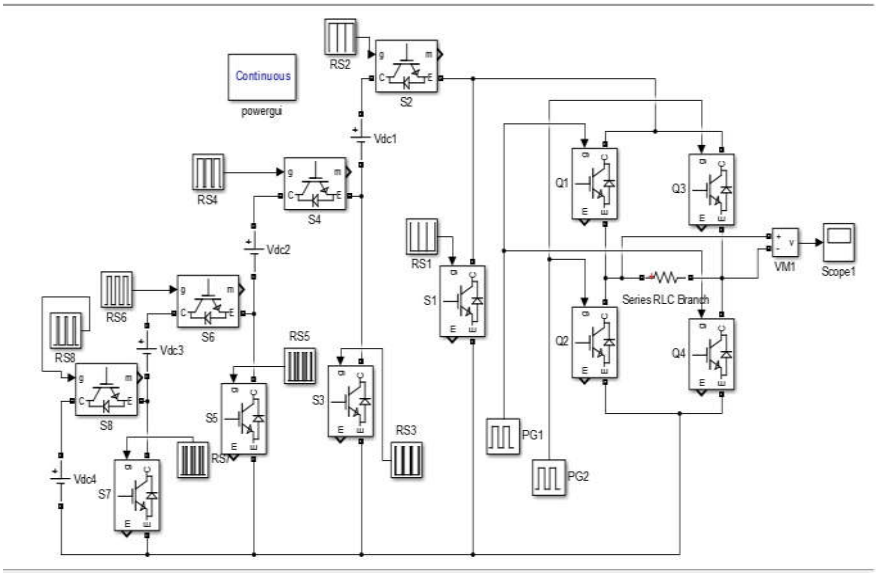

Fig.2.1 MATLA/ Simulink model of SCSS topology for nine level inverter in which valid switching combinations for the "SCSS-MLI" is shown in

Table -2.1

State	V_{BUS}(t)	Switching in ON State
1	V_{dc1}	S_2, S_3
2	$V_{dc1}+V_{dc2}$	S_2, S_4, S_5
3	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2, S_4, S_6, S_7
4	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_2, S_4, S_6, S_8
5	0	S_1

Table -2.2

SCSS BASED MLI		
Blocking Capabilities of SCSS Based mli		
S.No	Switch No	Voltage
1	S1=S2=S3=S4=S5=S6=S7 =200V	
Conduction switch and Variation switch Of SCSS Based MLI		
S.No	Switch No (conduction duration)	Calculation in (t) sec
1	S1	5.559 x10^{-4}sec ,1 x10^{-7} sce, 8.57 x10^{-4} sec
2	S2	8.57 x10^{-3} sec
3	S3	6.7x10^{-4}sec , 8.029 x10^{-3} sec
4	S4	7.109 x10^{-3} sec
5	S5	1.0339 x10^{-3} sec, 6.7022x10^{-3} sec
6	S6	1.0339 x10^{-3} sec
7	S7	8.65 x10^{-3} sec , 1.1566 x10^{-3} sec.
8	S8	3.449 x10^{-3} sec.

2.1 Waveform

The switching SCSS inverter in turn to alternate the voltage polarity of the DC bus voltage Vbus for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels . fig.2.1

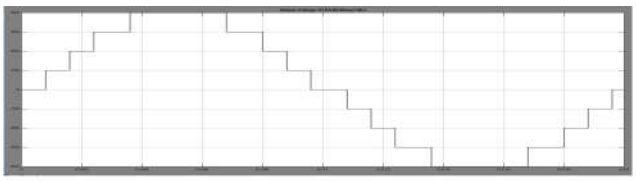

Fig-2.1 . waveform of scss inverter

The desired AC output voltage Van of SCSS is shown in the Figure.

2.2 No of Switching Devices

SCSS are consisting the No of I/P voltage source of switching devices required =2n+4 & no of voltage levels generated =2n+1.

2.3 Total voltage blocking Capacity

The MOSFET switches are triggered by proper switching signals to produce bus voltage Vbus. Multilevel voltage source consists of 8 switches named S1 –S8. The cell source is bypassed with S1on and S2 off, or adds to the DC voltage by reversing the switches. Based on this principle the switches in four cells can perform PWM if necessary or switching the switches at twice the fundamental frequency of output voltage. The switching patterns of a controlled switch are given in the Table . to produce DC bus voltage Vbus with the shape of stair case with (n=4) steps, where n is the number of cell sources output voltage.

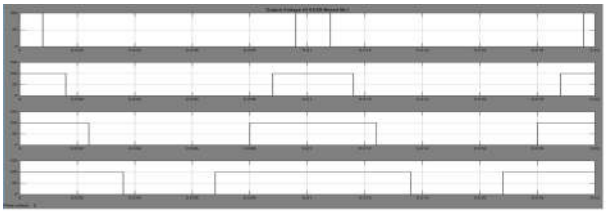

Fig-2.3 waveform of blocking capabilities of SCSS

2.4 Conduction Duration & Variation Switch

Conduction duration Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 1. Table 2.2 gives the sequence of closure and opening of switches. Based on switching sequence of the switches suitable program has written and burned to the AT89c51 microcontroller for producing triggering pulses for the MOSFETs in the MLDCL voltage source .

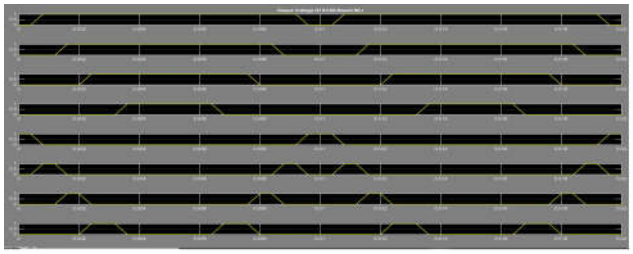

Fig-2.4 waveform of cond duration & variation switch of SCSS

3. Multilevel module (MLM)-based MLI

MLM BASED MLI aim to reduce the no of switch .this topology is a hybrid multilevel topology comprising of two part .the part 1 consist the i/p dc sources & bidirectional –blocking –bidirectional –conducting switches & its synthesize a multilevel half –wave voltage waveform .the voltage stress on these switches is not disturb uniformly .the part 2 is a simple H-bridge connected at the o/p of the part 1 whitch generates -ve & +ve polarities for the o/p voltage .the s/w in this part are unidirectional –blocking –bidirectional –conducting & have to with stand the maxi voltage generated by the part 1 .how ever these s/w can be operated at the line freq .thus these s/w are high –voltage low- freq switches.

A single phase topology for Nine level converter is shown in fig. where $V_{dc1} = V_{dc2}=V_{dc3}=V_{dc}$.the operating state are listed in table-1 .it is evident that all possible combinations of the i/p voltage level are not utilized thus in this topology .equal load sharing among the i/p dc sources is not possible. The s/w in the H bridge (mos 8,9,10,11).are each subjected to the voltage stress of 3 Vdc,The switches S1 & S4 need to have a minimum voltage –blocking capability of $3V_{dc}$.whereas S2 & S3 should be selected to bear the voltage stress of 2 V_{dc}.however ,only one s/w in the part 1 & two s/w in the part 2 need to conduct simultaneously .the topology does not allow asymmetrical sources configuration (binary or trinity).because its not possible to synthesize all subtractive & additive combination

Table -3.1

State	V_{BUS}(t)	Switching in ON State
1	V_{dc1}	S_2
2	V_{dc1}+V_{dc2}	S_3
3	V_{dc3}+V_{dc4}	S_1,S_3,S_5
4	V_{dc1}+V_{dc2}+V_{dc3}	S_4
4	V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}	S_5
5	0	S_1

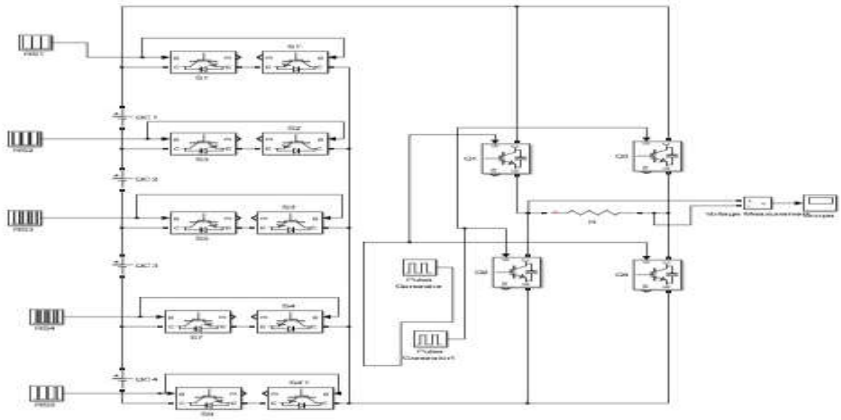

Fig.3.1 MATLA/ Simulink model of MLM topology for nine level inverter

Table -3.2

MLM BASED MLI		
Blocking Capabilities of MLM Based MLI		
S.No	Switch No	Voltage
1	S1=S2=S3=S4=S5=S6=S7 =100V	Equal voltage blocking
Conduction switch & Variation switch of MLM Based MLI		
S. No	Switch No conduction duration	Calculation in (t) sec
1	S1	5.55 x10^{-3}sec ,8.57 x10^{-4} sec
2	S2	6.73 x10^{-4} sec, 8.029 x10^{-4} sec.
3	S3	1.0339 x10^{-3} sec, 8.029 x10^{-3} sec
4	S4	8.65 x10^{-4} sec, 9.5566 x10^{-4} sec
5	S5	4.2X10^{-3} sec

3.1 Waveform

The switching signals MLM based inverter in turn to alternate the voltage polarity of the DC bus voltage Vbus for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels, whose . The desired AC output voltage Van of MLM MLI is shown in the Figure. 3.1

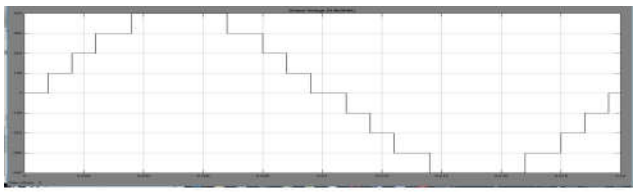

Fig-3.1 waveform of MLM based MLI

3.2 No of Switching Devices

MLM based MLI are consisting the No of unidirectional switch =4 & No of bidirectional switch = N+1.No of voltage levels generated =2n+1

3.3 Total voltage blocking Capacity

The MOSFET switches are triggered by proper switching signals to produce multi level bus voltage Vbus. Multilevel Voltage source consists of 8 switches named S1 –S8. The cell source is bypassed with S1on and S2 off, or adds to the voltage by reversing the switches. Based on this principle the switches in four cells can perform PWM if necessary or switching the switches at twice the fundamental frequency of output voltage. The switching patterns of a controlled switch are given in the Table . to produce DC bus voltage Vbus with the shape of stair case with (n=4) steps, where n is the number of cell sources output voltage

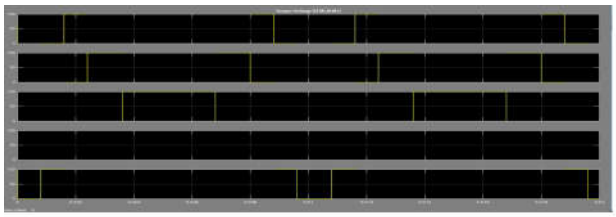

Fig-3.3 waveform of blocking capabilities of MLM based MLI

3.4 Conduction Duration & Variation Switch

Conduction duration Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 3. Table 3.2 gives the sequence of closure and opening of switches. Based on switching sequence of the switches suitable program has written and burned to the AT89c51 microcontroller for producing triggering pulses for the MOSFETs in the MLM voltage source.

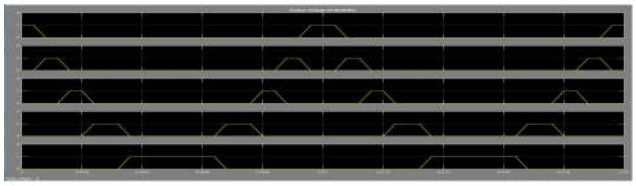

Fig-3.4 waveform of con duration & variation switches of MLM based MLI

4. Reversing voltage (RV) topology

The reversing voltage topology proposed [12] is illustrated in fig -12 its hybrid topology which separate the o/p in to two part .one part synthesizes a multilevel stepped voltage half wave .this part is part 1 comprising i/p dc sources of V_{dc}.[1-4] & s/w [1-8].A full bridge comprising s/w [1-8],is connected to the part 1 so as to obtain both +ve & -ve polarity for the o/p voltage .this part is named the part 2 in the way .the component are utilized effectively .the s/w in the part 2 need to withstand the total additive voltage of the part 1 .this topologies exhibit modularity for the part 1 .

Various possible states to obtains different levels at the part 1 v bus (t) . are summarized in table 2 .it can be noted that the switches with high blocking voltage ax the mos (1-4) ,can be operated at fundamental switching freq .if symmetric sources are used such that Vdc1=Vdc2=Vdc3=Vdc4=Vdc, then all switches of the part 1 experience a voltage stress of Vdc .while the four switches of the part 2 are required Part are required to have a minimum voltage – blocking capability of 4Vdc each .it can also be inferred from table 4.2 that for symmetric source configuration ,equal load sharing amongst them is not possible for a DC link created with connected capacitor .it can also be observed from that the no of switches conducting simultaneously to synthesize a required voltage level is not the same ,& thus conduction losses & switching losses for the switches may not be the same more ever ,since the topology Does not facilities the synthesis of all additive & subtractive combinations of i/p voltage sources ,trinity sources combinations cannot be used .other asymmetric combination to maximize the no of o/p level is seriously hampered by the absence of some state with a single voltage sources Vdc2 the sources 2 would lead to short circuiting of sources vdc3 & hence this state cannot be used) however one important advantage that the topology offer is that it uses a single DC link for three phase implementation .

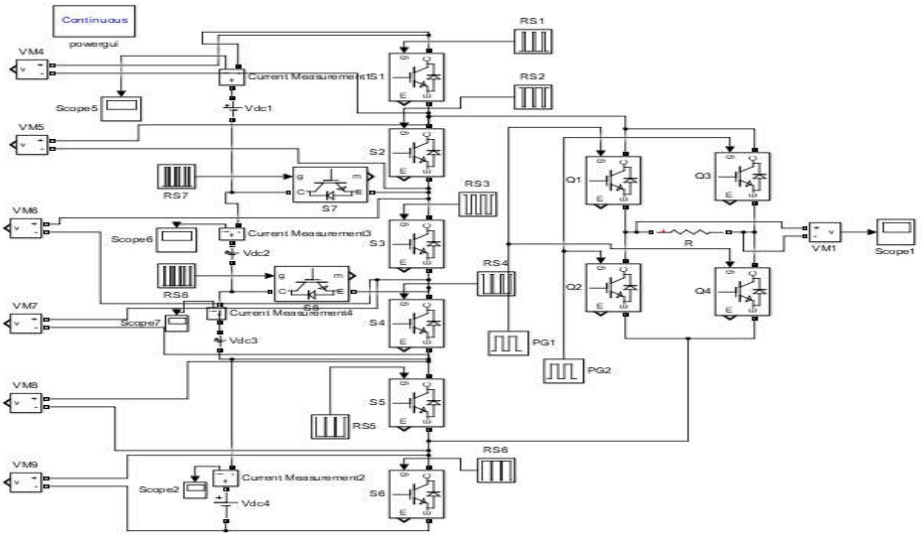

Fig 4 MATLA/ Simulink model of RV topology for nine level inverter

Table -4.1

State	V_{RVS}(t)	Switching in ON State
1	V_{dc1}	S_1,S_2,S_4,S_5,S_7
2	V_{dc2}	S_2,S_3,S_5,S_8
3	$9V_{dc4}$	S_2,S_3,S_4,S_6
4	$V_{dc1}+V_{dc2}$	S_1,S_4,S_5,S_8
5	$V_{dc2}+V_{dc3}$	S_2,S_5,S_7
6	$V_{dc2}+V_{dc4}$	S_2,S_3,S_6,S_8
7	$V_{dc1}+V_{dc4}$	S_1,S_2,S_4,S_6,S_7
8	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1,S_5
9	$V_{dc2}+V_{dc3}+V_{dc4}$	S_2,S_6,S_7
10	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_1,S_6
11	0	S_2,S_3,S_4,S_5

Table -4.2

RV TOPOLOGY BASED MLI		
Blocking Capabilities of RV Based MLI		
S.No	Switch No	Voltage
1	S1=300,S6=100,S7 =100,S8=200V	Different voltage blocking
Conduction switch and Variation switch of MLDCL Based MLI		
S.no	Switch No (conduction duration)	Calculation in (t) sec
1	S1	3.449 x10^{-7} sec
2	S2	3.12 x10^{-3} sec, 3.4206 x10^{-3} sec
3	S3	2.216 x10^{-3} sec, 2.46 x10^{-3} sec
4	S4	1.21 x10^{-3} sec, 1.66 x10^{-3} sec
5	S5	5.55 x10^{-3} sec ,8.57 x10^{-3} sec
6	S6	8.58 x10^{-3} sec
7	S7	8.65 x10^{-4} sec ,9.56x10^{-4} sec
8	S8	1.0339 x10^{-3} ,8.029 x10^{-3} sec

4.1 WAVEFORM

The switching signals shown in Figure 6(b) are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage Vbus for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels, whose voltages are -(V1+V2+.....+ Vn) , -(V1+V2+.....Vn-1).....,-V2, -V1 ,0, V1, V2,.....(V1+V2+....Vn-1), (V1+V2+....Vn). Where V1, V2.....Vn are voltages of cell sources. The desired AC output voltage Van of RV is shown in the Figure

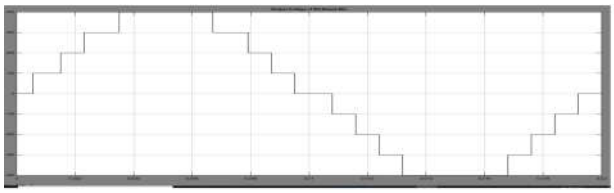

Fig-4.2 waveform of RV topology

4.2 No of Switching Devices

RV topology are consisting the No of DC I/P voltage source of switching devices required =2n+4 & no of voltage levels generated =2n+1.

4.3 Total voltage blocking Capacity

The MOSFET switches are triggered by proper switching signals to produce bus voltage Vbus. Multilevel voltage source consists of 8 switches named S1 –S8. The cell source is bypassed with S1on and S2 off, or adds to the DC link voltage by reversing the switches. Based on this principle the switches in four cells can perform PWM if necessary or switching the switches at twice the fundamental frequency of output voltage. The switching patterns of a controlled switch are given in the Table . to produce DC bus voltage Vbus with the shape of stair case with (n=4) steps, where n is the number of cell sources output voltage

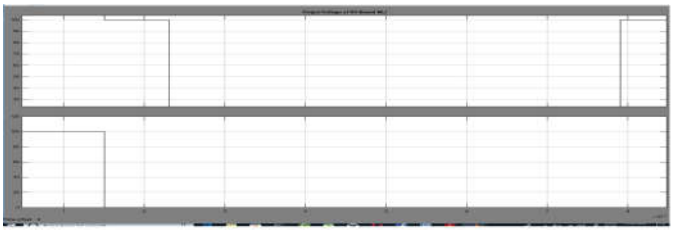

Fig-4.3 waveform blocking capabilities of RV topology

4.4 CONDUCTION DURATION & VARIATION

SWITCHING:- Conduction duration Based on the various modes given in table 1 switching signals are generated for the switches in the half bridge cells. The switching pulses are shown in Figure 4. Table 4.2 gives the sequence of closure and opening of switches. Based on switching sequence of the switches suitable program has written and burned to the AT89c51 microcontroller for producing triggering pulses for the MOSFETs in the rv voltage source.

Fig-4.4 waveform of condu. dutation of variation switch of RV topology

IV. DISCUSSIONS

Multilevel Inverter topologies presented in the previous section, comments can be made on them based on parameters. Based on the qualitative features of these topologies, MLDCL-MLI is a highly modular structure whereas topologies, however, require isolated dc sources. MLM-MLI, and RV topology require non-isolated input dc levels. Also, three-phase configurations with the RV topology can be implemented with a single dc link. is that only four switches need to conduct to obtain a given voltage level across the load terminals. It can be said that when attempts are made to reduce the power switch count, the number of states are reduced and following features may be hampered: even power distribution among the symmetric . To show the feasibility of the proposed multilevel inverter topology, a setup of 9-
level symmetrical topology is considered. The experimental setup consists of two basic blocks connected in series with each block consists of two DC sources with equal magnitude as 100V. A rectifier unit with an isolation transformer and a
capacitor filter forms the DC voltage sources. The diode IN4007 acts as a bridge rectifier unit. To get the constant voltage to the controller, IC7805 acts as a voltage regulator. The gate signals for driving the power switches has been generated with the help of 16-bit digital signal controller dsPIC30F2010. As seen from Table 5 the switches S_{21} and S_{22} were neglected and therefore 10 MOSFET (IRF840N),2,3,4 experimental results for the symmetric 9-level inverter.

V. CONCLUSION

To analyze the performance of the proposed multilevel inverter topology during the symmetric and asymmetric operation, simulation is carried out. A series connected two basic units with a H-bridge as shown in Fig. 1,2,3,,4 is developed using MATLAB/SIMULINK software. The developed model consists of four DC voltage sources and main switches. It achieves 9-level during symmetric operation and. A series RL load with magnitudes R= in Ω are considered as load parameters. In this paper nine level multilevel reduce device count multilevel topologies is presented.

Based on the review, it can be concluded that in the process of reducing the power switch count, various compromises are involved such as:increased voltage rating of semiconductor switches,requirement of bidirectional switches, increased number of sources and/or requirement of asymmetric input dc levels , loss of modularity reduced number of redundant states Complex modulation/control schemes7) difficulty in possibility of charge balance control.

MLIs continue to gain increasing importance for both high power and low power applications, many researchers have pro-posed specific topological solutions for intended applications. Also, newer multilevel topologies have been presented, offering high output resolution with a reduced number of power switches.

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