

Design of a Fast Adder for Signed Bits Using QUATERNARY Number system

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Abstract— With the binary number system, the computation speed is limited by formation and propagation of carry especially as the number of bits increases. Using a quaternary Signed Digit number system one may perform carry free addition, borrow free subtraction and multiplication. However the QSD number system requires a different set of prime modulo based logic elements for each arithmetic operation. A carry free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD). In QSD, each digit can be represented by a number from -3 to 3. Carry free addition and other operations on a large number of digits such as 64, 128, or more can be implemented with constant delay and less complexity. Design is simulated & synthesized using Modelsim6.0, XILINX.

I. INTRODUCTION

One of the primary features that help us determine the computational power of a processor is the speed of its arithmetic unit. An important function of an arithmetic block is addition because, in most mathematical computations, it forms the bulk of the execution time. Thus, the development of fast adders has been a key research area for a long time.

The high performance adders are essential since the speed of the digital processor depends heavily on the speed of the adders used in the system. Adders are most commonly used in various electronic applications e.g. Digital signal processing in which adders are used to perform various algorithms like FIR, IIR etc. In past, the major challenge for VLSI designer is to reduce area of chip by using efficient optimization

techniques. Then the next phase is to increase the speed of operation to achieve fast calculations like, in today's microprocessors millions of instructions are performed per second. Speed of operation is one of the major constraints in designing DSP processors.

The redundancy associated with signed-digit numbers offers the possibility of carry free addition. The redundancy provided in signed-digit representation allows for fast addition and subtraction because the sum or difference digit is a function of only the digits in two adjacent digit positions of the operands for a radix greater than 2, and 3 adjacent digit positions for a radix of 2. Thus, the add time for two redundant signed-digit numbers is a constant independent of the word length of the operands, which is the key to high speed computation. The advantage of carry free addition offered by QSD numbers is exploited in designing a fast adder circuit. Additionally adder designed with QSD number system has a regular layout which is suitable for VLSI implementation which is the great advantage over the RBSD adder. An Algorithm for design of QSD adder is proposed. This algorithm is used to write the VHDL code for QSD adders. VHDL codes for QSD adder is simulated and synthesized and the timing report is generated. The timing report gives the delay time produced by the adder structure. Binary signed-digit numbers are known to allow limited carry propagation with a somewhat more complex addition process requiring very large circuit for implementation. A special higher radix-based (quaternary) representation of binary signed-digit numbers not only allows carry-free

addition and borrow-free subtraction but also offers other important advantages such as simplicity in logic and higher storage density.

It offers the advantage of reduced circuit complexity both in terms of transistor count and interconnections. QSD number uses 25% less space than BSD to store number. So the proposed QSD adder is better than RBSD adder in terms of number of gates, input connections and delay though both perform addition within constant time. Proposed design has the advantages of both parallelisms as well as reduced gate complexity. The computation speed and circuit complexity increases as the number of computation steps decreases. A two step schemes appear to be a prudent choice in terms of computation speed and storage complexity. Quaternary is the base 4 redundant number system. The degree of redundancy usually increases with the increase of the radix. The signed digit number system allows us to implement parallel arithmetic by using redundancy. QSD numbers are the SD numbers with the digit set as: { 3, 2, 1, 0, 1, 2, 3 } where 3, 2, and 1 represent -3, -2, and -1 respectively. In general, a signed-digit decimal number D can be represented in terms of an n digit quaternary signed digit number as

$$D = \sum_{i=0}^{n-1} X_i 4^i$$

Where x_i can be any value from the set { 3, 2, 1, 0, 1, 2, 3 } for producing an appropriate decimal representation. For digital implementation, QSD numbers are B represented using 3-bit 2's complement notation. A QSD negative number is the QSD complement of the QSD positive number [3]. For example, using primes to denote complementation, we have $3' = 3, 3' = 3, 2' = 2, 2' = 2, 1' = 1, 1' = 1$.

II. EXISTING WORK

The Binary Number System

Consider again the example of a child counting a pile of pennies, but this time in binary. He would begin with the first penny: "1." The next penny counted makes the total one single group of two pennies. What number is this?

When the base-10 child reached nine (the highest symbol in his scheme), the next penny gave him "one group of ten", denoted as 10, where the "1" indicated

one collection of ten. Similarly, when the base-2 child reaches one (the highest symbol in his scheme), the next penny gives him "one group of two", denoted as 10, where the "1" indicates one collection of two.

Back to the base-2 child: The next penny makes one group of two pennies and one additional penny: "11." The next penny added makes two groups of two, which is one group of 4: "100." The "1" here indicates a collection of two groups of two, just as the "1" in the base-10 number 100 indicates ten groups of ten.

Upon completing the counting task, base-2 child might find that he has one group of four pennies, no groups of two pennies, and one penny left over: 101 pennies. The child counting the same pile of pennies 3 in base-10 would conclude that there were 5 pennies. So, 5 in base-10 is equivalent to 101 in base-2. To avoid confusion when the base in use is not clear from the context, or when using multiple bases in a single expression, we append a subscript to the number to indicate the base, and write

1025101

Just as with decimal notation, we write a binary number as a string of symbols, but now each symbol is a 0 or a 1. To interpret a binary number, we multiply each digit by the power of 2 associated with that digit's position.

For example, consider the binary number 1101. This number is

$$1101 = 1 \cdot 2^3 + 1 \cdot 2^2 + 0 \cdot 2^1 + 1 \cdot 2^0 = 13_{10}$$

Since binary numbers can only contain the two symbols 0 and 1, numbers such as 25 and 1114000 cannot be binary numbers.

We say that all data in a computer is stored in binary that is, as 1's and 0's. It is important to keep in mind that values of 0 and 1 are *logical* values, not the values of a physical quantity, such as a voltage. The actual *physical* binary values used to store data internally within a computer might be, for instance, 5 volts and 0 volts, or perhaps 3.3 volts and 0.3 volts or perhaps *reflection* and *no reflection*. The two values that are used to physically store data can differ within different portions of the same computer. All that really matters is that there are two different symbols, so we will always refer to them as 0 and 1.

A string of eight bits (such as 11000110) is termed a *byte*. A collection of four bits (such as 1011) is smaller than a byte, and is hence termed a *nibble*. (This is the sort of nerd-humor for which engineers are famous.)

The idea of describing numbers using a positional system, as we have illustrated for base-10 and base-2, can be extended to any base.

For example, the base-4 number 231 is:

$$231 = 2.4^2 + 3.4^1 + 1.4^0 = 45_{10}$$

III. Proposed System

Quaternary Signed Digit (QSD number system).

The QSD is a radix-4 number system that provides the benefit of faster arithmetic calculations over binary computation, as it eliminates rippling of carry during addition. Every number in QSD can be represented using digits from the set $\{-3, -2, -1, 0, 1, 2, 3\}$. Being a higher radix number system it utilizes less number of gates and hence saves on time and reduces circuit complexity. The stages involved in addition of two numbers in QSD are: Stage1: Generation of intermediate carry and sum: When two digits are added in QSD number system, the resulting sum ranges between -6 to +6. Numbers with magnitude higher than 3 are represented by multiple digits with least significant digit representing sum and the next digit corresponds to carry. Also, every number in QSD can have multiple representations. The representation is chosen such that the magnitude of sum digit is 2 or less than 2 and the magnitude of carry digit is 1 or less than 1, the reason for which is explained in the next stage. Stage2: The intermediate sum and carry have a limit fixed on their magnitude because this allows carry free addition in the second step. The result can be obtained directly by adding the sum digit with the carry of the lower significant digit.

Proposed System.

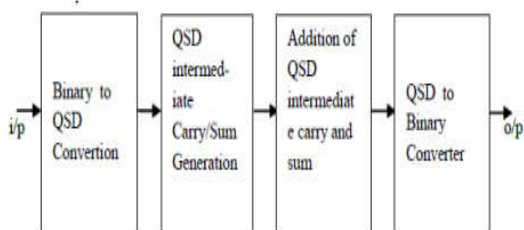


Fig. 1 Block Diagram of QSD Addition.

In QSD number system carry propagation chain are eliminated which reduce the computation time substantially, thus enhancing the speed of the machine. As range of QSD number is from -3 to 3, the addition result of two QSD numbers varies from -6 to +6. Table I depicts the output for all possible

combinations of two numbers. The decimal numbers in the range of -3 to +3 are represented by one digit QSD number. As the decimal number exceeds from this range, more than one digit of QSD number is required. For the addition result, which is in the range of -6 to +6, two QSD digits are needed. In the two digits QSD result the LSB digit represents the sum bit and the MSB digit represents the carry bit. To prevent this carry bit to propagate from lower digit position to higher digit position QSD number representation is used. QSD numbers allow redundancy in the number representations. The same decimal number can be represented in more than one QSD representations. So we choose such QSD represented number which prevents further rippling of carry. To perform carry free addition, the addition of two QSD numbers can be done in two steps

Step 1: First step generates an intermediate carry and intermediate sum from the input QSD digits i.e., addend and augend.

Step 2: Second step combines intermediate sum of current digit with the intermediate carry of the lower significant digit. So the addition of two QSD numbers is done in two stages. First stage of adder generates intermediate carry and intermediate sum from the input digits. Second stage of adder adds the intermediate sum of current digit with the intermediate carry of lower significant digit. To remove the further rippling of carry there are two rules to perform QSD addition in two steps:

Rule 1: First rule states that the magnitude of the intermediate sum must be less than or equal to 2 i.e., it should be in the range of -2 to +2.

Rule 2: Second rule states that the magnitude of the intermediate carry must be less than or equal to 1 i.e., it should be in the range of -1 to +1.

TABLE I
THE INTERMEDIATE CARRY AND SUM
BETWEEN -6 TO +6

Sum	QSD represented number	QSD coded number
-6	$\bar{2}2, \bar{1}\bar{2}$	$\bar{1}\bar{2}$
-5	$\bar{2}3, \bar{1}\bar{1}$	$\bar{1}\bar{1}$
-4	$\bar{1}0$	$\bar{1}0$
-3	$\bar{1}1, 0\bar{3}$	$\bar{1}1$
-2	$\bar{1}2, 0\bar{2}$	$0\bar{2}$
-1	$\bar{1}3, 0\bar{1}$	$0\bar{1}$
0	00	00
1	01, $1\bar{3}$	01
2	02, $1\bar{2}$	02
3	03, $1\bar{1}$	$1\bar{1}$
4	10	10
5	11, $2\bar{3}$	11
6	12, $2\bar{2}$	12

According to these two rules the intermediate sum and intermediate carry from the first step QSD adder can have the range of -6 to +6. But by exploiting the redundancy feature of QSD numbers we choose such QSD represented number 655 which satisfies the above mentioned two rules. When the second step QSD adder adds the intermediate sum of current digit, which is in the range of -2 to +2, with the intermediate carry of lower significant digit, which is in the range of -1 to +1, the addition result cannot be greater than 3 i.e., it will be in the range of -3 to +3. The addition result in this range can be represented by a single digit QSD number; hence no further carry is required. In the step 1 QSD adder, the range of output is from -6 to +6 which can be represented in the intermediate carry and sum in QSD format as shown in table I. We can see in the first column of Table I that some numbers have multiple representations, but only those that meet the above defined two rules are chosen. The chosen intermediate carry and intermediate sum are listed in the last column of Table I as the

QSD coded number. This addition process can be well understood by following examples:

Example: To perform QSD addition of two numbers A = 107 and B = -233 (One number is positive and one number is negative).

First convert the decimal number to their equivalent QSD representation:

$$(107)_{10} = 2 \times 4^3 + 2 \times 4^2 + 3 \times 4^1 + 1 \times 4^0 = (2\ 2\ 31)_{QSD}$$

$$(233)_{10} = 3 \times 4^3 + 3 \times 4^2 + 2 \times 4^1 + 1 \times 4^0 = (33\ 2\ 1)_{QSD}$$

Hence, $(-233)_{10} = (3\ 3\ 21)_{QSD}$

Now the addition of two QSD numbers can be done as follows:

A = 107	$\bar{2}$	$\bar{2}$	3	$\bar{1}$
B = -233	$\bar{3}$	$\bar{3}$	2	$\bar{1}$
Decimal Sum	-1	-5	5	-2
IC	0	$\bar{1}$	1	0
IS	$\bar{1}$	$\bar{1}$	1	$\bar{2}$
S	$\bar{2}$	0	1	$\bar{2}$
C _{out}	0			

The sum output is (2 01 2)QSD which is equivalent to $(-126)_{10}$ and carry output is 0. From these examples it is clear that the QSD adder design process will carry two stages for addition. The first stage generates intermediate carry and sum according to the defined rules. In the second stage the intermediate carry from the lower significant digit is added to the intermediate sum of current digit which results in carry free output. In this step the current digit can always absorb the carry-in from the lower digit.

Logic design and implementation using of single digit QSD adder unit

There are two steps involved in the carry-free addition. The first step generates an intermediate carry and sum from the addend and augend. The second step combines the intermediate sum of the current digit with the carry of the lower significant digit. To prevent carry from further rippling, two rules are defined. The first rule states that the magnitude of the intermediate sum must be less than or equal to 2. The second rule states that the magnitude of the carry must be less than or equal to 1. Consequently, the magnitude of the second step output cannot be greater than 3 which can be represented by a single-digit QSD number; hence no further carry is required. In step 1, all possible input pairs of the addend and augend are considered. The range of input numbers can vary from -3 to +3, so the addition result will vary from -6 to +6 which needs two QSD digits. The lower significant digit serves as sum and most significant digit serves as carry. The generation of the carry can be avoided by mapping the two digits into a pair of intermediate sum and intermediate carry such that the nth intermediate sum and the (n-1)th intermediate carry never form any carry generating pair (3,3), (3,2), (3,1), (3 , 3), (3, 2), (3,1).

If we restrict the representation such that the intermediate carry is limited to a maximum of 1, and the intermediate sum is restricted to be less than 2, then the final addition will become carry free. Both inputs and outputs can be encoded in 3-bit 2's complement binary number. The mapping between the inputs, addend and augend, and the outputs, the intermediate carry and sum are shown in binary format in Table II.

To remove the further carry propagation the redundancy feature of QSD numbers is used. We restrict the representation such that all the intermediate carries are limited to a maximum of 1, and the intermediate sums are restricted to be less than 3, then the final addition will become carry free. The QSD representations according to these rules are shown in Table for the range of -6 to +6. As the range of intermediate carry is from -1 to +1, it can be represented in 2 bit binary number but we take the 3 bit representation for the bit compatibility with the intermediate sum. At the input side, the addend A_i is represented by 3 variable input as A_2, A_1, A_0 and the augend B_i is represented by 3 variable input as B_2, B_1, B_0 . At the output side, the intermediate carry IC is represented by IC_2, IC_1, IC_0 and the intermediate sum is represented by IS_2, IS_1 and IS_0 . The six variable expressions for intermediate carry and intermediate sum in terms of inputs (A_2, A_1, A_0, B_2, B_1 and B_0) can be derived from Table 4.3. So we get the six output expressions for $IC_2, IC_1, IC_0, IS_2, IS_1$ and IS_0 . As the intermediate carry can be represented by only 2 bits, the third appended bit IC_2 is equal to IC_1 so the expression for both outputs will be the same.

Table II
The conversion between the inputs and outputs of the intermediate carry and intermediate sum

INPUT				OUTPUT					
QSD		Binary		Decimal	QSD		Binary		
A_i	B_i	A_j	B_j	Sum	C_i	S_i	C_i	S_i	
3	3	011	011	6	1	2	001	010	
3	2	011	010	5	1	1	001	001	
2	3	010	011	5	1	1	001	001	
3	1	011	001	4	1	0	001	000	
1	3	001	011	4	1	0	001	000	
2	2	010	010	4	1	0	001	000	
1	2	001	010	3	1	-1	001	111	
2	1	010	001	3	1	-1	001	111	
3	0	011	000	3	1	-1	001	111	
0	3	000	011	3	1	-1	001	111	
1	1	001	001	2	0	2	000	010	
0	2	000	010	2	0	2	000	010	
2	0	010	000	2	0	2	000	010	
3	-1	011	111	2	0	2	000	010	
-1	3	111	011	2	0	2	000	010	
0	1	000	001	1	0	1	000	001	
1	0	001	000	1	0	1	000	001	
2	-1	010	111	1	0	1	000	001	
-1	2	111	010	1	0	1	000	001	
3	-2	011	110	1	0	1	000	001	
-2	3	110	011	1	0	1	000	001	
0	0	000	000	0	0	0	000	000	
1	-1	001	111	0	0	0	000	000	
-1	1	111	001	0	0	0	000	000	
2	-2	010	110	0	0	0	000	000	
-2	2	110	010	0	0	0	000	000	
-3	3	101	011	0	0	0	000	000	
3	-3	011	101	0	0	0	000	000	
0	-1	000	111	-1	0	-1	000	111	
-1	0	111	000	-1	0	-1	000	111	
-2	1	110	001	-1	0	-1	000	111	
1	-2	001	110	-1	0	-1	000	111	
-3	2	101	010	-1	0	-1	000	111	
2	-3	010	101	-1	0	-1	000	111	
-1	-1	111	111	-2	0	-2	000	110	
0	-2	000	110	-2	0	-2	000	110	
-2	0	110	000	-2	0	-2	000	110	
-3	1	101	001	-2	0	-2	000	110	
1	-3	001	101	-2	0	-2	000	110	
-1	-2	111	110	-3	-1	1	111	001	
-2	-1	110	111	-3	-1	1	111	001	
-3	0	101	000	-3	-1	1	111	001	
0	-3	000	101	-3	-1	1	111	001	
-3	-1	101	111	-4	-1	0	111	000	
-1	-3	111	101	-4	-1	0	111	000	
-2	-2	110	110	-4	-1	0	111	000	
-3	-2	101	110	-5	-1	-1	111	111	
-2	-3	110	101	-5	-1	-1	111	111	
-3	-3	101	101	-6	-1	-2	111	110	

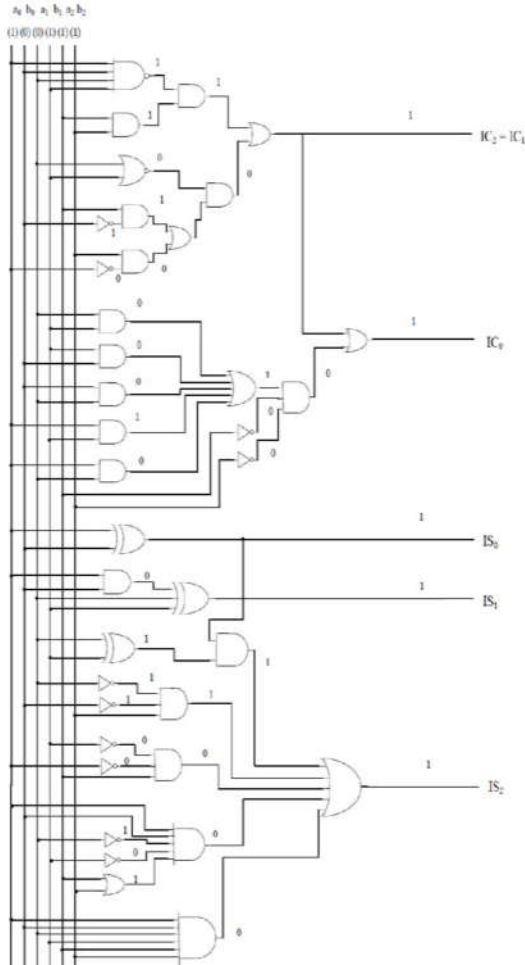
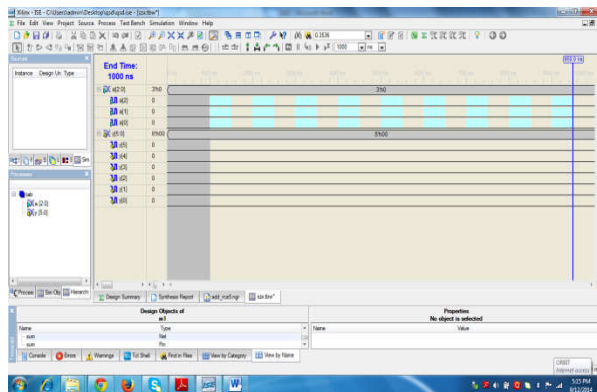


Figure 2: Data Flow of single digit QSD adder cell.

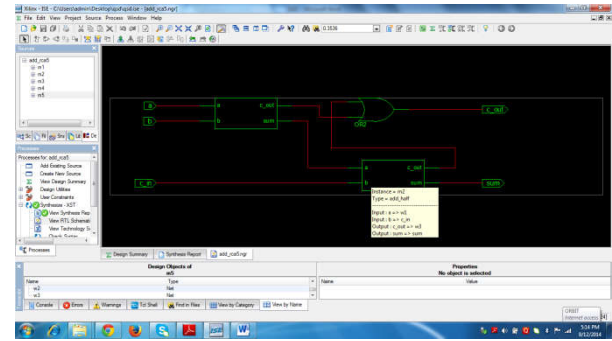
IV RESULTS

The simulation and verified effect are shown, once the realistic verification is done, the RTL mannequin is taken to the synthesis method using the Xilinx ISE instrument. This design is synthesized and its outcome were analyzed as follows.

Simulation.



RTL Schematic.



Design Summary.

- Number of Slices: 6 out of 960 0% .
- Number of 4 input LUTs:10 out of 1920 0% .
- Number of IOs: 17
- Number of bonded IOBs: 17 out of 66 25%.

Timing Summary:

- Minimum period: No path found
- Minimum input arrival time before clock: No path found
- Maximum output required time after clock: No path found
- Maximum combinational path delay: 10.020ns

V CONCLUSION

In the proposed design of Quaternary Signed Digit adder designed for carry free addition implementation for single digit addition, the design is simulated using Modelsim 6.0 and synthesized using Xilinx ISE, power dissipation is obtained using Xilinx. Consequently this design is appropriate to be applied for construction of a high performance multiprocessor which consists of many processing elements.

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