A HIGHLY EFFICIENT AND RELIABLE INVERTER CONFIGURATION BASED CASCADED MULTILEVEL INVERTER FOR PV ENTITIES

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ABSTRACT-This paper introduces an improved cascaded multilevel inverter (CMLI) for efficient and reliable configuration for PV. Proposed paper uses a 9 level cascaded multilevel inverter. It is based on exceptionally effective and dependable configuration for the minimization of leakage current and lessening in size of electromagnetic interference filters. Aside from a diminished switch check, proposed conspire has extra highlights of low switching and conduction losses. Moreover, the augmentation of proposed CMLI alongside the PWM procedure for 2m + 1 levels is additionally introduced, where m speaks to the quantity of photovoltaic (PV) sources, hence due to 9 level here we have used four PV sources where m=4. Proposed topology with the given pulse width Modulation (PWM) procedure diminishes the high frequency voltage advances in terminal and regular mode voltages. A correlation of proposed CMLI with the current PV MLI topologies is likewise exhibited in project. The 9level voltages have been shown by using Matlab software.

Keywords: CMV(common mode voltage),MLI(multi level inverter),PWM(pulse width modulation)

INTRODUCTION

These days, grid-associated PV entities have turned out to be one of quickest developing and most encouraging renewable energy sources on the planet. In 2018 it is assessed an overall PV introduced power of around 321 GW, in most preservationist situation, that is double the introduced power in 2013. MLI topologies are picking up significance because of their favorable circumstances, for example, high proficiency, low switch check, low weight, and decreased size. In any case, evacuation of transformer dispenses with the galvanic isolation between PV array and output load. Expulsion of galvanic isolation builds leakage current bargaining the wellbeing in PV entities. It has prompted the improvement of different wellbeing benchmarks for PV entities, which limit the esteem or greatness of leakage current flow in PV entity [1]– [5]. Aside from leakage current minimization, there is a persistently expanding interest for astounding power output to be bolstered into grid from PV entity. This prerequisite has prompted the utilization of MLI in transformer less PV entities.

In writing, numerous topologies or configurations of MLIs [6], [7] are proposed for the minimization of leakage current for their application in transformerless PV entities. These configurations utilize two techniques for minimization of leakage current [8]. One technique is based on maintaining the basic mode voltage (CMV) constant, while the other strategy is based on the minimization of high-frequency changes in terminal and CMVs. One exquisite arrangement based on maintaining a constant CMV is proposed by Zhang et al. [9]. The given MLI configuration [9] comprises of eight switches for the generation of three levels in output voltage. This topology diminishes the switching losses however has the downside of high conduction losses amid both turn ON and zero voltage states. The given MLI configuration has an uneven operation amid every half-cycle of fundamental component of grid voltage. The characteristic asymmetry in every half-cycle causes a dc offset in MLI output voltage. Moreover, the prerequisite of an extra number of switches for more than three-level operation confines its application.

Islam and Mekhilef [10] have proposed another interesting transformerless PV MLI topology to decrease leakage current by maintaining CMV constant. This MLI topology utilizes six switches for the generation of three levels in inverter output voltage. This circuit configuration results in high switching and conduction losses. Besides, this MLI topology can't be reached out to in excess of three levels in output voltage. Xiao et al. [11] have proposed another proficient three-level MLI for the minimization of leakage current by maintaining CMV constant. The given topology [11] has low conduction and switching losses. In any case, this configuration experiences the drawback of a high number of gadget checks. Another interesting topology with low switching losses based on constant CMV is proposed by Ji et al. [12]. This MLI topology comprises of six switches and two diodes. Aside from bringing about high conduction losses, this topology is less managable for an augmentation to a higher number of levels in output voltage.

Another imperative technique to limit leakage current is by the disposal of high-frequency voltage advances in CMV. One such interesting arrangement is proposed by Buticchi et al. [13]. The creators have proposed a five-level grid-tied PV MLI topology. This MLI topology comprises of eleven switches and four diodes. In this MLI, four switches in low-voltage bridge are worked with high switching frequency, while the remaining switches in high-voltage bridge are worked with the low switching frequency. For an appropriate

operation of this configuration [13], the adjust of flying capacitor voltage Vfc is vital. Moreover, PV terminals in this MLI topology can't be grounded. Based on a comparable idea, another great proposition is given by Hong et al. [14]. In this arrangement, the creators have proposed a solitary inductor dual buck full-bridge inverter for the generation of variable CMV at low frequency. The MLI topology requires six switches and two diodes. The switches in H-bridge are worked at a low switching frequency, while the bidirectional switch is worked at a high switching frequency. Notwithstanding, subtle elements of expanding the topology for a higher number of levels are not clarified in project [14].

From previously mentioned talk, it is clear that there is a requirement for a generalized transformerless PV MLI, with less semiconductor devices to accomplish the goals of high productivity and economy. It ought to likewise be guaranteed that PV MLI ought to have its switching and conduction losses advanced with a lower number of leading switches amid the zero voltage state. Moreover, the augmentation to the higher number of levels ought to be conceivable.

- This project proposes one such answer for the minimization of leakage current in transformerless MLIs associated with PV entities. The pulse width tweak (PWM) entity for proposed MLI is additionally talked about in project. The examination of PV terminal and CMVs utilizing switching function is introduced. This investigation prompts the improvement of proposed PWM strategy, which forestalls high frequency voltage changes in terminal voltage and CMV. Notable highlights of proposed cascaded MLI (CMLI) are as per the following:
- The topology utilizes eight switches for the generation of five levels in output voltage.
- During the zero voltage state just a single switch and one diode lead.
- In proposed topology, four switches are worked at a low switching frequency, which lessens the switching losses.
- The dead band in PWM entity does not influence the CMV.
- Proposed inverter can be effectively cascaded to accomplish in excess of nine levels in output

CASCADED NINE-LEVEL MLI

The schematic circuit diagram of proposed nine-level CMLI for PV entity is aroused in Fig. 1. The given configuration comprises of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter including two switches Sx1 and S x2. The Conv-2 includes an exceedingly productive and dependable inverter configuration [15] with six switches (Sx3– Sx8). Among the six switches, four switches (Sx3– Sx6) in Conv-2 constitute a H-bridge circuit. The remaining two switches Sx7 and Sx8 in Conv-2 are bidirectional switches. The switches in Conv-1 are utilized to create voltage levels of VPV and VPV/2. When switch Sx1 is turned ON, voltage VPV is connected at the terminal n regarding the terminal z. So also, the terminal n accomplishes voltage VPV/2 when switch Sx2 is turned ON. The switches Sx1 and Sx2 are corresponding in nature.

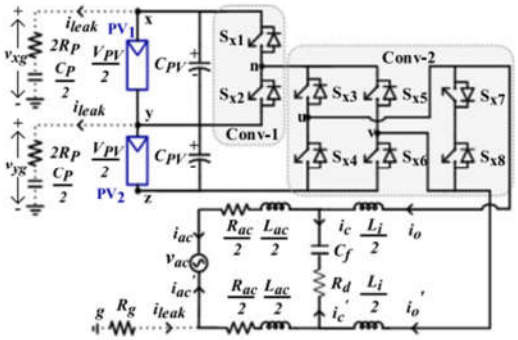

Fig. 1: Proposed nine-level grid-connected CMLI with PV and parasitic elements

The produced voltage levels at the terminal n of Conv-1 are given as a contribution to the Conv-2. The Conv-2 produces the positive, negative, and zero levels of relating input (voltage between the terminals n and z) over the load. The bidirectional switches Sx7 and Sx8 give the free-wheeling way amid zero voltage state. Output of nine-level CMLI is associated with grid through a LCL filter as aroused in Fig. 1 [16]– [18]. It comprises of inverter side inductance Li, capacitance Cf , and grid side inductance L air conditioning. The protection Rd in shunt branch of filter is utilized as a damping resistor. The protection Rac alludes to grid side protection, and protection Rg demonstrates protection in ground way. The variable vac alludes to instantaneous grid voltage. The variables Rp and Cp allude to the parasitic protection and capacitance in PV entity, individually, aroused with dabbed lines in Fig. 1. The parasitic capacitance in PV entity frames a thunderous circuit with the filter inductances [16]. The variables io, ic, and iac indicate output current of nine-level CMLI, current flowing through shunt branch of filter, and present flowing into grid, individually.

The current ileak demonstrates leakage current flowing from PV array into the ground through parasitic capacitance (see Fig. 1). Proposed MLI topology contains four sets of corresponding switches (Sx1, Sx2), (Sx3, Sx4), (Sx5, Sx6), and (Sx7, Sx 8) in proposed configuration. Notwithstanding, to limit leakage current, the correlative switching is utilized just for the two sets of switches (Sx1, Sx2) and (Sx7, Sx8). Maintaining a strategic distance from correlative activity for

alternate sets of switches helps in segregating PV and grid source amid the zero voltage state.

OPERATION OF PROPOSED CASCADED NINE-LEVEL MLI

Fig. 2 demonstrates the operation of inverter in all its switching states. Inverter output voltage vuv at various voltage levels with the relating switching states of all the switches is arosed in Table I. Inverter output voltage vuv achieves voltage levels +VPV or −VPV when switch Sx1 is turned ON alongside other inverter switches (Sx3, Sx6) or (Sx4, Sx5), individually, as arosed in Fig. 2(a) and (e). Additionally, voltage levels +VPV/2 or −VPV/2 are acquired at vuv when switch Sx2 is turned ON with indistinguishable switching combinations from arosed in Fig. 2(b) and (d). The most critical element to be seen amid zero voltage state or free-wheeling stage is the isolation or separation between PV source and grid. The isolation between PV source and grid can be accomplished by killing all the switches of H-bridge inverter as arosed in Fig. 2(c).

TABLE I
SWITCHING STATES WITH THEIR RESPECTIVE OUTPUT VOLTAGE

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	v_{uv}
1	0	1	0	0	1	1	0	$+V_{PV}$
0	1	1	0	0	1	1	0	$+V_{PV}/2$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{PV}/2$
1	0	0	1	1	0	0	1	$-V_{PV}$

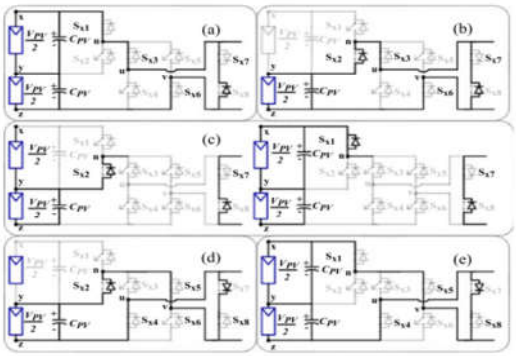

Fig. 2: Single-phase nine-level cascaded MLI for output voltage levels (a) $+V_{PV}$, (b) $+V_{PV}/2$, (c) 0, (d) $-V_{PV}/2$, and (e) $-V_{PV}$.

The kill state of four switches in H-bridge amid the zero voltage state results in isolation of PV source from grid. The bidirectional switches Sx7 and Sx8 give a freewheeling way to the inductor current amid the kill period of a switching cycle. This activity helps in limiting leakage current flowing through the parasitic capacitance. As there is no direct association between the two sources, PV terminal points (hubs x, y, and z) skim and have vague voltages. The buoy or indistinct esteem limits the terminal voltages from getting to be zero. Hence, high-frequency voltage changes at PV terminals are dodged. As such, the likelihood of flow of leakage current can be limited. Additionally, in other intermediate states, for example, switching between VPV/2 to VPV or the other way around, again a similar principle can be utilized. The above activity additionally helps in minimization of leakage current in PV entity. The PWM method for proposed nine-level CMLI is extensively examined in going before area. The articulations for the shaft voltages vuz and vvz is given, individually, as

$$v_{uz} = \left(S_1S_3 + 0.5S_2S_3 - \frac{1}{(S_3+S_4)} + \frac{1}{(S_3+S_4)(S_1+S_2)}\right)V_{PV} \quad (1)$$

$$v_{vz} = \left(S_1S_5 + 0.5S_2S_5 - \frac{1}{(S_5+S_6)} + \frac{1}{(S_5+S_6)(S_1+S_2)}\right)V_{PV} \quad (2)$$

Where, Sa (a = 1, 2, 3, . . .) is the switching state of switch Sxa whose esteem can be either 1 (remains for turn-ON) or 0 (remains for kill).

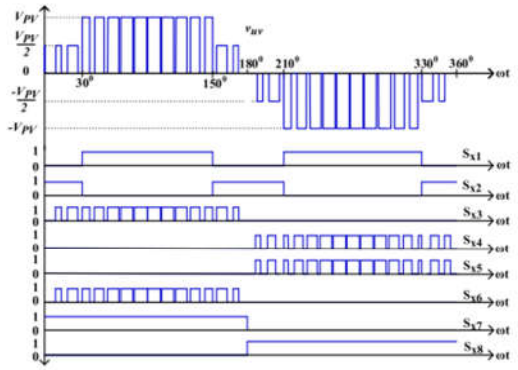

Fig. 3. Gate pulses for the switches corresponding to inverter output voltage.

Fig. 3 demonstrates the switching example of all the switches for the relating inverter output voltage vuv. The switches Sx1 and Sx2 in half-bridge are worked at low switching frequency. With a specific end goal to take out the high switching frequency operation, the switch Sx2 is kept turned ON in zero state amid voltage change between the levels 0 to VPV/2. Also, the switch Sx1 is kept turned ON, amid voltage change between levels 0 to VPV. Inverter switch match (Sx3, Sx6) is worked with a high switching frequency amid positive half-cycle, and it remains at the kill state amid the negative half-cycle of inverter output voltage vuv. A comparative operation is material to the next inverter switch combine (Sx4, Sx5), which is worked with higher

switching frequency amid the negative half-cycle. The switches Sx7 and Sx8 are turned ON amid positive and negative half-cycles of output voltage vuv, separately. The expulsion of integral activity from combine of switches (Sx3, Sx4) and (Sx5, Sx6) encourages finish kill of switches amid every half-cycle of output voltage vuv. Likewise, proposed entity has the upside of lessened switching losses, acknowledging to a very proficient and dependable inverter configuration which may bring about higher effectiveness.

The generalized topology for 2m + 1 levels can likewise be acquired for proposed nine-level CMLI. The quantity of PV sources in CMLI is signified by the term m. Estimation of m is dependably a fundamental different of 2 (i.e., m = 2, 4, . . .). The broadened rendition of proposed CMLI for 2m + 1 levels is introduced in Fig. 4. The generalized topology is acquired by falling the fundamental units comprising of half-bridge and H-bridge. The bidirectional switches are associated in middle of output terminals for the free-wheeling period. Proposed generalized 2m + 1 level MLI is likewise contrasted and half bridge and full-bridge particular MLC. The half bridge secluded MLC requires less number of switches when contrasted with proposed generalized 2m + 1 level MLI. In any case, it is hard to lessen or limit the flow of leakage current in half-bridge measured MLC. Additionally, the quantity of electrolytic capacitors utilized at the info side of half-bridge measured MLC is high contrasted with proposed generalized 2m + 1 level MLI. Proposed MLI has a lesser gadget check when contrasted with the full-bridge particular MLC [19]. Similarly, both can limit leakage current flowing through PV entity

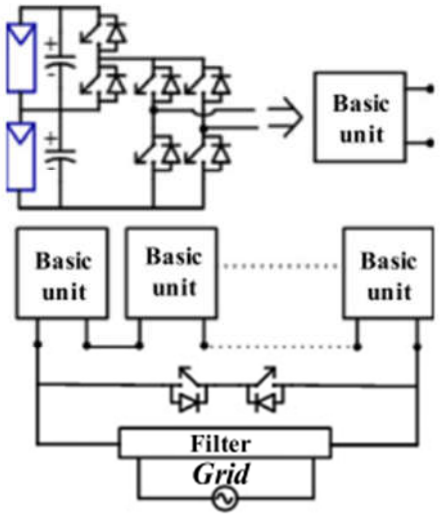

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Fig. 4: Generalized 2m + 1 level MLI topology derived from proposed nine-level CMLI.

PROPOSED PWM STRATEGY ALONG WITH GENERALIZED STRATEGY FOR MINIMIZATION OF LEAKAGE CURRENT

The operation of proposed PWM method is clarified by considering the given nine-level CMLI. The high-frequency advances in terminal voltages vxg and vyg of nine-level CMLI are limited utilizing proposed PWM procedure. Proposed activity can be accomplished by switching from VPV to 0 state or the other way around rather than the switching from VPV to VPV/2 state or the other way around. Also, amid the zero voltage state or free-wheeling period of switching cycle, PV array is secluded from grid. The isolation of PV array and grid amid zero voltage state is like inverter configuration revealed in [15]. The greatness of reference wave vmod is brought down to half of its unique esteem at whatever point the switching is flipped among the levels VPV and 0. The above activity is mainly done to suit estimation of PV voltage VPV. The adjustment in estimation of vmod is done at whatever point the instantaneous greatness of balancing wave vmod surpasses estimation of mama/2, where mama alludes to the balance file. By fusing the coveted change, output voltage incorporates the zero voltage state (i.e., free-wheeling state) in all its switching periods. The articulation for altered reference waveform vref adjusted is given as

$$v_{ref\_modified} = \begin{cases} v_{mod} for\ 0 \le |v_{mod}| < \frac{m_a}{2}\ from\ \frac{V_{PV}}{2}\ to\ 0 \\ \frac{v_{mod}}{2}\ for \frac{m_a}{2} \le |v_{mod}| < m_a\ from\ V_{PV}\ to\ 0 \end{cases} \quad (3)$$

Where, vmod = masinωt gives the extent of vmod. Output voltage of proposed PWM method for the nine-level CMLI is aroused in Fig. 5.

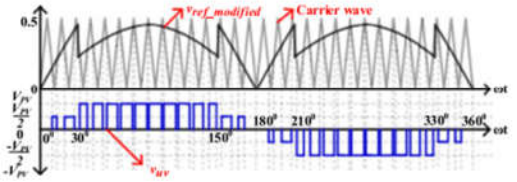


Fig. 5: Waveform of output voltage vuv for proposed PWM technique.

In Fig. 5, the changed reference wave is contrasted and triangular bearer wave. Amid the positive half-cycle of voltage vac, at whatever point the phase edge ωt lies in run 0– 30° and instantaneous greatness of vref adjusted surpasses the bearer wave, when vuv accomplishes voltage level of VPV/2 else, it is changed to the zero voltage state. So also, when ωt lies in range 30–150°, inverter output voltage vuv achieves voltage level of VPV at whatever point the instantaneous size vref altered surpasses the transporter wave or accomplishes zero esteem generally. In a similar positive half-cycle, for the remaining scope of ωt (i.e., in vicinity of 150° and 180°), vuv achieves

voltage levels VPV/2 if the instantaneous greatness of vref altered is more prominent than the bearer wave. A comparative sequence is embraced amid the negative half-cycle of voltage vac. In this manner, in entire cycle if the size of vref altered is not as much as the transporter wave, when vuv accomplishes zero voltage level.

For the usage of proposed PWM to a 2m + 1 level inverter, the waveform of generalized adjusted reference wave vref changed gen is aroused in Fig. 6.

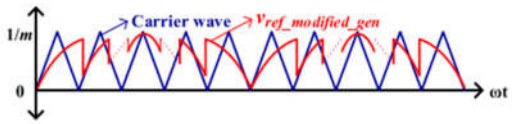


Fig. 6: Waveform of generalized modified reference wave $v_{ref\text{-}modified\text{-}gen}$.

The term m alludes to the quantity of PV sources utilized. At whatever point the instantaneous supreme greatness of vmod surpasses the esteem j(ma/m), the size of vref-changed gen moves toward becoming k(|vmod|/m) where j = 1, 2, . . . , m– 1, m and k = 1, 2, . . . , m– 1. The articulation for vref-adjusted gen is given as

$$v_{ref_{modified\_gen}} = \begin{Bmatrix} v_{mod} for\ 0 \le |v_{mod}| < \frac{m_a}{m}\ from\ \frac{V_{PV}}{2}\ to\ 0 \\ \frac{v_{mod}}{2}\ for \frac{m_a}{m} \le |v_{mod}| < \frac{2m_a}{m}\ from\ \frac{2V_{PV}}{m}\ to\ 0 \\ \frac{v_{mod}}{m} for\ \frac{(m-1)m_a}{m} \le |v_{mod}| < m_a from\ V_{PV}\ to\ 0 \end{Bmatrix} \quad (4)$$

INTEGRATION OF MPPT FOR PROPOSED NINE-LEVEL CMLI

The notable perturb and observe calculation [20] is utilized for the two PV sources (thinking about nine-level operation) individually to track MPP. In this manner, each MPPT calculation tracks the MPP for particular PV sources. To track the MPP, the required data of 1) the normal estimations of two PV source voltages (VPV1 and VPV2 for PV sources PV1 and PV2, individually) and 2) the currents (IPV1 and IPV2 for PV sources PV1 and PV2, separately) are detected and after that given to their particular MPPT calculations. The MPPT calculations when utilize the detected estimations of PV voltages and currents for the count of individual estimations of tweak records ma1 and ma2 for the two PV sources PV1 and PV2, separately. Outputs of two MPPT calculations are then used for estimation of general regulation list mama . The articulation for mama is given as

$$m_a = m_{a1}\frac{V_{PV1}}{V_{PV1}+V_{PV2}} + m_{a2}\frac{V_{PV2}}{V_{PV1}+V_{PV2}} \quad (5)$$

The ascertained tweak list mama is then utilized by the PWM methodology as depicted in previously mentioned area to create the PWM pulses for proposed nine-level CMLI.

ANALYTICAL EXPRESSIONS OF PV TERMINAL VOLTAGE AND COMMON-MODE VOLTAGE FOR PROPOSED CASCADED NINE-LEVEL INVERTER

The examination of leakage current can be done from declaration of terminal voltages vxg, vyg, and vzg. The articulation for PV terminal voltages can be gotten from switching function examination [21]. From Fig. 1, utilizing the superposition hypothesis, PV terminal voltages vxg and vyg are communicated as takes after:

$$v_{xg} = S_1 v_{x1g} + S_2 v_{x2g} \quad (6)$$

$$v_{yg} = S_1 v_{y1g} + S_2 v_{y2g} \quad (7)$$

The terms vx1g and vy1g are voltages at terminals x and y, separately, when switch Sx1 is turned ON. Correspondingly, vx2g and vy2g are voltages at terminals x and y, individually, when switch Sx2 is turned ON. The articulation for voltage vzg when switch Sx1 is turned ON is given as

$$v_{zg} = v_{x1g} - V_{PV} \quad (8)$$

Correspondingly, the articulation for terminal voltage vzg when switch Sx2 is turned ON is given as

$$v_{zg} = v_{y2g} - \frac{V_{PV}}{2} \quad (9)$$

With the utilization of switching function examination, voltages vug and vvg (from Figs. 1 and 2) communicated regarding vx1g and vzg are aroused, separately, as

$$v_{ug} = S_1 S_3 v_{x1g} + S_4 v_{zg} \quad (10)$$

$$v_{vg} = S_1 S_5 v_{x1g} + S_6 v_{zg} \quad (11)$$

Thus, voltages vug and vvg (from Figs. 1 and 2) communicated as far as vy2g and vzg utilizing switching functions are aroused, individually, as

$$v_{ug} = S_2 S_3 v_{y2g} + S_4 v_{zg} \quad (12)$$

$$v_{vg} = S_2 S_5 v_{y2g} + S_6 v_{zg} \quad (13)$$

Presently communicating voltages vug and vvg as far as grid voltage vac, voltage drop in filter inductors (Li and Lac) and protections (Rac and Rg) [21] can be given by

$$v_{ug} = \frac{L_i}{2}\frac{di_o}{dt} + \frac{L_{ac}}{2}\frac{di_{ac}}{dt} + v_{ac} + \frac{R_{ac}}{2}i_{ac} - R_g i_{leak} \quad (14)$$

$$v_{vg} = \frac{L_i}{2}\frac{di_{o'}}{dt} + \frac{L_{ac}}{2}\frac{di_{ac'}}{dt} + \frac{R_{ac}}{2}i_{ac'} - R_g i_{leak} \quad (15)$$

Presently, with the expansion of (14) and (15), and by overlooking voltage drop in protections Rg and Rac/2 with presumptions of iac = −iac and io = −io, [21] gives

$$v_{ug} + v_{vg} = v_{ac} \quad (16)$$

Substituting estimations of vug and vvg from (10) and (11) into (16) and improving those utilizing (8)

gives the articulation for the terminal voltage vx1g as

$$v_{x1g} = \frac{v_{ac} + V_{PV}(S_4 + S_6)}{(S_1S_3 + S_1S_5 + S_4 + S_6)} \quad (17)$$

Presently, the other terminal voltage vy1g (when switch Sx1 is ON) can be figured by subtracting vx1g and VPV/2. So also, substituting (12) and (13) into (16) and streamlining for terminal voltage vy2g utilizing (9) results in

$$v_{y2g} = \frac{v_{ac} + \frac{V_{PV}}{2}(S_4 + S_6)}{(S_2S_3 + S_2S_5 + S_4 + S_6)} \quad (18)$$

The other terminal voltage vx2g can be computed by including vy2g and VPV/2. Presently by utilizing (6) and (7), the total articulation for terminal voltages vxg and vyg is given, individually, as

$$v_{xg} = v_{ac}S_{W1} + V_{PV}S_{W2} + v_{ac}S_{W3} + \frac{V_{PV}}{2}S_{W4} + \frac{V_{PV}}{2}S_2 \quad (19)$$

$$v_{yg} = v_{ac}S_{W1} + V_{PV}S_{W2} + v_{ac}S_{W3} + \frac{V_{PV}}{2}S_{W4} - \frac{V_{PV}}{2}S_1 \quad (20)$$

The terms SW1, SW2, SW3, and SW4 in (19) and (20) are given by

$$S_{W1} = \frac{S_1}{(S_1S_3 + S_1S_5 + S_4 + S_6)}$$

$$S_{W2} = \frac{S_1(S_4 + S_6)}{(S_1S_3 + S_1S_5 + S_4 + S_6)}$$

$$S_{W3} = \frac{S_2}{(S_2S_3 + S_2S_5 + S_4 + S_6)}$$

$$S_{W4} = \frac{S_2(S_4 + S_6)}{(S_2S_3 + S_2S_5 + S_4 + S_6)}$$

Substituting the qualities S3 = 0, S4 = 0, S5 = 0, and S6 = 0 in voltage state results in vague esteem (0/0) in terminal voltages vxg, vyg, and vzg. The unclear esteem (0/0) amid a zero voltage state is mainly a direct result of disengaging PV source and grid. The isolation of PV source and grid can likewise be observed in Fig. 2(c). The CMV vcm is gotten by taking the normal of post voltage vuz and vvz given in (1) and (2), individually. The articulation for vcm is

$$v_{cm} = \left((S_1 + 0.5S_2)(S_3 + S_5) + \left(\frac{1}{(S_3 + S_4)} + \frac{1}{(S_5 + S_6)}\right) \times \left(\frac{1}{(S_1 + S_2)} - 1\right)\right)\frac{V_{PV}}{2} \quad (21)$$

Table II gives estimations of shaft voltages (vuz, vvz) and CMV vcm at various levels in output voltage vuv. Amid the kill period in a switching cycle, all the switches in H-bridge are in a cut-off state with the goal that the switching states S3, S4, S5, and S6 are equivalent to zero esteem. Substituting the relating estimations of S3, S4, S5, and S6 in (21) results in a vague esteem (i.e., vcm = 0/0) amid the zero voltage state. The CMV accomplishes the esteem VPV/2 for both positive and negative levels of output voltage VPV and achieves the esteem VPV/4 for both positive and negative levels of output voltage VPV/2.

TABLE II

VALUES OF COMMON-MODE VOLTAGE AND POLE VOLTAGES FOR CORRESPONDING OUTPUT VOLTAGE

v_{uv}	v_{uz}	v_{vz}	v_{cm}
$+V_{PV}$	V_{PV}	0	$V_{PV}/2$
$+V_{PV}/2$	$V_{PV}/2$	0	$V_{PV}/4$
0	Undefined	Undefined	Undefined
$-V_{PV}/2$	0	$V_{PV}/2$	$V_{PV}/4$
$-V_{PV}$	0	V_{PV}	$V_{PV}/2$

The articulations for terminal and CMVs can be checked with MATLAB programming utilizing simulink block-set. The parameters VPV = 400 V, switching frequency of bearer wave fsw = 1 kHz, vac = 220 V (rms), and grid frequency fg = 50 Hz are considered for the simulation. The transporter wave frequency is confined to 1 kHz. This is done to show the indistinct states obviously. Fig. 7 demonstrates the waveforms of terminal voltages vxg, vyg, vzg, and CMV vcm.

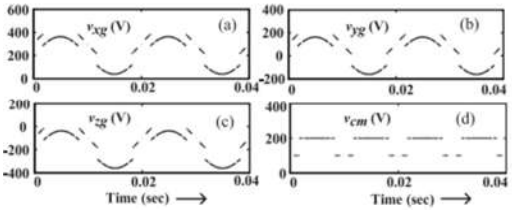


Fig. 7: Analytical results of proposed nine-level CMLI showing the waveforms of (a) terminal voltage v_{xg} ; (b) terminal voltage v_{yg} ; (c) terminal voltage v_{zg} ; and (d) common-mode voltage v_{cm} .

The irregularity in waveforms happens when PV source and grid are detached. The isolation of grid and PV array results in a vague incentive in terminal and CMVs (brokenness in waveform). Since estimation of terminal and CMVs is indistinct amid the zero voltage state, they can be thought to be confined to the past esteem. In this manner, advances in voltage waveform can be limited. As it were, it results in limiting the high-frequency voltage advances in terminal and CMVs. Minimization or decrease of high-frequency voltage advances in terminal voltage additionally helps in diminishing leakage current in PV entity. PV array parasitic capacitance [18] offers high impedance for the low-frequency advances in terminal voltage. Likewise, the size of leakage current flowing through the parasitic capacitance is less. At the end of day, proposed PWM entity limits leakage current by diminishing the high-frequency advances in terminal and CMVs

SIMULATION RESULTS

To help the switching function investigation given in past area, proposed nine-level CMLI is reenacted utilizing POWERSIM blocks in MATLAB/SIMULINK programming. The PWM entity clarified in Section III is utilized for proposed nine-level CMLI configuration. Table III gives estimation of different parameters utilized for mimicking proposed nine-level CMLI.

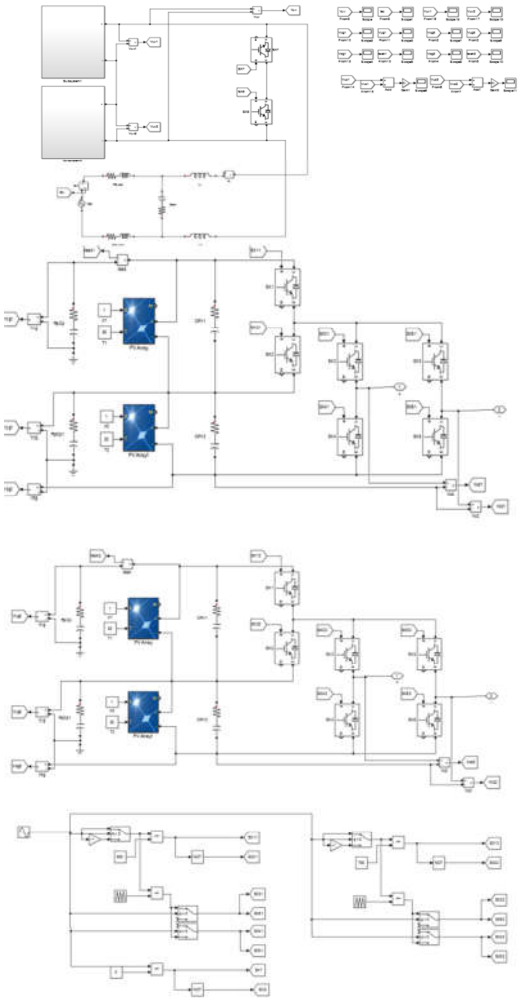


TABLE III
PARAMETERS CONSIDERED FOR THE SIMULATION OF PROPOSED NINE-LEVEL CMLI

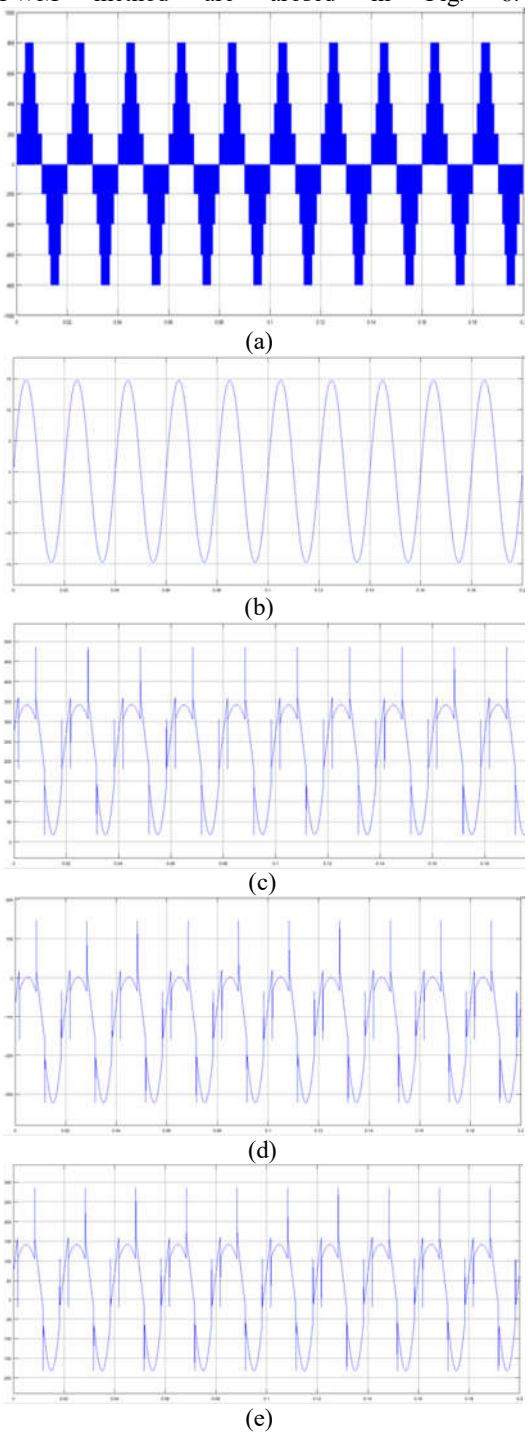
Parameter	P	V_{dc}	f_{sw}	v_{ac}	f_{ac}
Value	2.5 kW	400 V	25 kHz	220 V	50 Hz
Parameter	L_{ac}	R_{ac}	R_g	L_i	C_f
Value	4 mH	0.01 Ω	0.1 Ω	4 mH	0.1 μF
Parameter	R_d	C_p	R_p		
Value	50 mΩ	200 nF	1 Ω		

Proposed nine-level CMLI needs to produce a voltage Vinv having a phase δinv [16] to nourish the required measure of active power P into grid

$$\delta_{inv} = \arctan\left(\frac{2\pi f_{ac}(L_{ac}+L_i)P}{v_{ac}^2 + R_{ac}P}\right) \quad (22)$$

$$V_{inv} = \left(v_{ac} + \frac{R_{ac}P}{v_{ac}}\right)\frac{1}{\cos\delta_{inv}} \quad (23)$$

For a power of P = 2.5 kW, estimation of δinv = 0.117 rad and Vinv = 323 V is figured by substituting the parameters from Table III in (22) and (23), separately. The simulation waveforms of proposed nine-level CMLI utilizing proposed PWM method are aroused in Fig. 8.



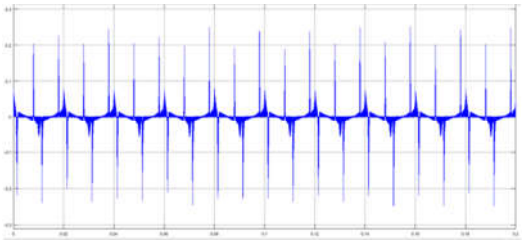
(a)

(b)

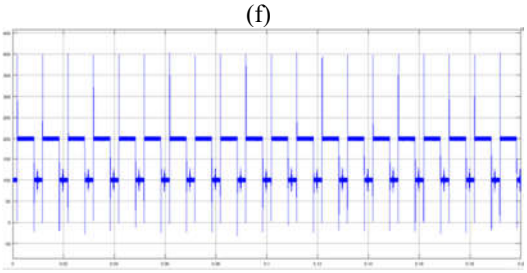
(c)

(d)

(e)



(f)



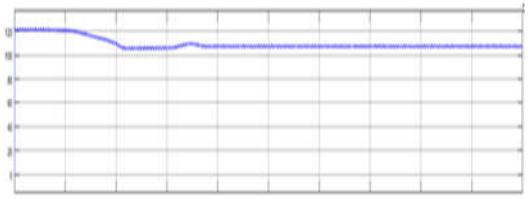
(g)

Fig. 8: Simulation results of proposed nine-level CMLI showing the waveforms of (a) output voltage v_{uv} ; (b) grid current i_{ac} ; (c) terminal voltage v_{xg} ; (d) terminal voltage v_{yg} ; (e) terminal voltage v_{zg} ; (f) leakage current i_{leak} ; and (g) common-mode voltage v_{cm} .

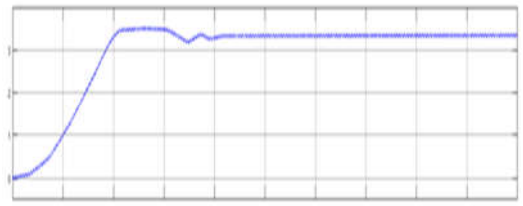
Fig. 8(a) demonstrates output voltage of nine-level CMLI. The nearness of zero voltage state in all voltage changes of vuv can be unmistakably seen from plot. Grid current iac is aroused in Fig. 8(b). Grid current is about sinusoidal. The total harmonic distortion of grid current iac is around 1.76% and meets the prerequisite of standard IEEE 1547. The waveform of terminal voltages vxg, vyg, and vzg are aroused in subplots (c), (d), and (e) of Fig. 8, individually. The significant perception produced using these subplots is the nonattendance of high-frequency voltage advances. Likewise, these waveforms coordinate with the outcome got utilizing the switching function investigation (see Fig. 7). This legitimizes the examination given in past area. Fig. 8(f) demonstrates the waveform for leakage current ileak flowing through the parasitic capacitor. Proposed PWM entity diminishes estimation of leakage present as can be observed in Fig. 8(f). This is a direct result of low-frequency voltage advances in terminal voltages vxg, vyg, and vzg. The spikes in leakage current are observed when there is a sudden voltage change in terminal voltage. The rms estimation of ileak is under 20 mA which is according to the standard VDE0126-1-1 [13]. Fig. 8(g) demonstrates the waveform of CMV vcm. The high-frequency voltage advances in CMV are likewise maintained a strategic distance from. This further cuts down the size, weight, and cost of electromagnetic interference (EMI) filter to be utilized in grid-associated entity [22].

Another simulation is completed with proposed configuration to exhibit the MPPT operation. Proposed nine-level CMLI is worked utilizing two MPPT calculations to separate the maximum power from individual PV arrays. As clarified in Section IV, the two individual MPPT calculations are utilized for the two PV sources PV1 and PV2 which are indistinguishable (having same array configuration). Simulation is finished considering a resistive load associated with output of inverter by means of a LC filter. PV modules with an opencircuit voltage of 21.05 V and short out current of 3.74 An at STC are decided for the array simulation. The electrolytic capacitors of 5000 µF are utilized as a cushion between PV sources and inverter as arosed in Fig. 1. Inverter is associated with a load of 20 Ω through a LC filter with the inductor and capacitor estimations of 4 mH and 2 µF, separately. The two PV arrays PV1 and PV2 have an open-circuit voltage of 126.90 V and a short out current of 3.8 An at an insolation of 1.0 sun and temperature of 50 °C.

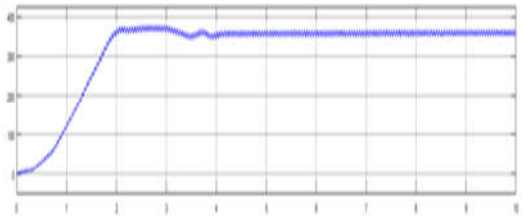
Fig. 9 demonstrates the simulation results of MPPT execution for proposed nine-level CMLI. The subplots [see Fig. 9(a) and (b)] demonstrate the waveforms of PV voltages VPV1 and VPV2 for PV1 and PV2 sources, individually. Estimations of working voltages VPV1 and VPV2 of two PV arrays are about equivalent PV currents IPV1 and IP V 2 are arosed in subplots Fig. 9(c) and (d), separately. Voltage– current (v-I) attributes of PV array can be observed with the expanding estimation of current by diminishing voltage or the other way around. The power PPV1 and PPV2 from PV sources PV1 and PV2 are arosed in subplots Fig. 9(e) and (f), individually. The operation of two PV sources close MPP can be affirmed with the low estimation of swell in PV power and little motions in tweak list mama, which can be observed in zoomed some portion of Fig. 9(g). The waveform of output power crosswise over resistive load Pload is arosed in subplot Fig. 9(h). It can be observed that the power crosswise over output load is about equivalent to the total of individual PV powers PPV1 and PPV2. The waveforms of vref adjusted and vuv are likewise arosed in subplots Fig. 9(i) and (j). Integration of MPPT for proposed nine-level CMLI makes inverter reasonable for PV entities.



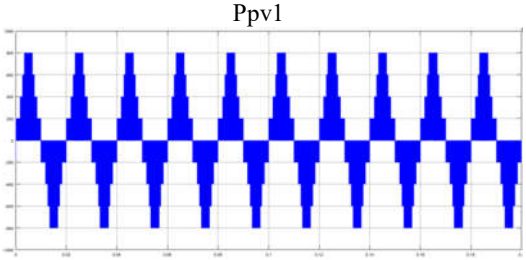
Vpv1



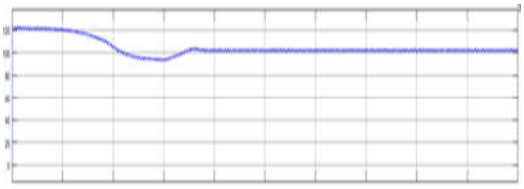
Ipv1



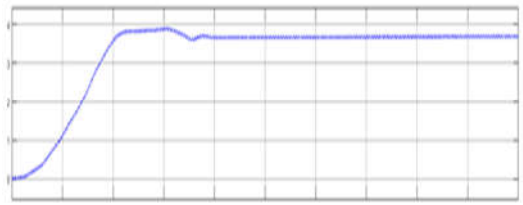
Ppv1



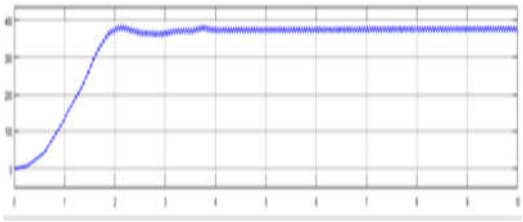
Vuv



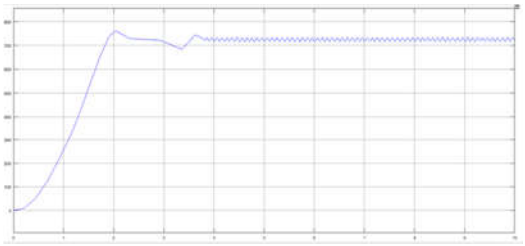
Vpv2



Ipv 2



Ppv2



Pload

Fig. 9: Proposed nine-level CMLI integrated with MPPT. The subplots give waveforms of (a) voltage V_{PV1} ; (b) voltage V_{PV2} ; (c) current I_{PV1} ; (d) current I_{PV2} ; (e) power P_{PV1} ; (f) power P_{PV2} ; (g) resultant modulation index ma ; (h) output power PO U T ; (i) modified reference wave $v_{ref\text{-}modified}$; and (j) inverter output voltage v_{ab} .

CONCLUSION

In this paper, an improved nine-level CMLI for PV entity was proposed. Proposed CMLI limited leakage current by wiping out the high-frequency advances in terminal and CMVs with low switch mean the minimization of leakage current. It likewise diminished conduction and switching losses which made it conceivable to work the CMLI at high switching frequency. Besides, the answer for generalized 9 levels CMLI was likewise introduced in project. The given PWM method required just a single bearer wave for the generation of 9 levels. The operation, examination of terminal and CMVs for the CMLI was likewise introduced in project. The simulation and test results approved the investigation completed in this project. The MPPT calculation was likewise incorporated with proposed nine-level CMLI to remove the maximum power from PV panels. Proposed CMLI was likewise contrasted and other existing MLI topologies in Table V to demonstrate its favorable circumstances.

REFERENCES

[1] Y. Tang, W. Yao, P.C. Loh, and F. Blaabjerg, “Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination,”IEEE Trans. Ind. Electron., vol. 63, no. 2, pp. 1016–1026, Feb. 2016.

[2] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, “Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression,” IEEE Trans. Ind. Electron., vol. 62, no. 7, pp. 4537–4551, Jul. 2015.

[3] J. Ji, W. Wu, Y. He, Z. Lin, F. Blaabjerg, and H. S. H. Chung, “A simple differential mode EMI suppressor for the LLCL-filter-based single-phase grid-tied transformerless inverter,”IEEE Trans. Ind. Electron., vol. 62, no. 7, pp. 4141–4147, Jul. 2015.

[4] Y. Bae and R. Y. Kim, “Suppression of common-mode voltage using a multicentral

photovoltaic inverter topology with synchronized PWM," IEEE Trans. Ind. Electron., vol. 61, no. 9, pp. 4722–4733, Sep. 2014.

[5] N. Vazquez, M. Rosas, C. Hernandez, E. Vazquez, and F. J. Perez-Pinal, "A new common-mode transformerless photovoltaic inverter,"IEEE Trans. Ind. Electron., vol. 62, no. 10, pp. 6381–6391, Oct. 2015.

[6] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems,"IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 906–918, Mar. 2013.

[7] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application,"IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[8] M. Cavalcanti, K. De Oliveira, A. M. de Farias, F. Neves, G. Azevedo, and F. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 4, pp. 1360–1368, Apr. 2010.

[9] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 730–739, Feb. 2013.

[10] M. Islam and S. Mekhilef, "H6-type transformerless single-phase inverter for grid-tied photovoltaic system," IET Power Electron., vol. 8, no. 4, pp. 636–644, 2015.

[11] H. F. Xiao, K. Lan, and L. Zhang, "A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage,"IEEE Trans. Power Electron., vol. 30, no. 6, pp. 3122–3132, Jun. 2015.

[12] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 2104–2115, May 2013.

[13] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A five-level grid-connected converter topology for single-phase transformerless PV systems," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3951–3960, Aug. 2014

. [14] F. Hong, J. Liu, B. Ji, Y. Zhou, J. Wang, and C. Wang, "Single inductor dual buck full-bridge inverter,"IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4869–4877, Aug. 2015.

[15] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems,"IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[16] O. Lopez, R. Teodorescu, and J. D. Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," inProc. 32nd Annu. Conf. IEEE Ind. Electron. Soc., Nov. 2006, pp. 5191–5196.

[17] O. Lopez, R. Teodorescu, F. Freijedo, and J.D. Gandoy, "Leakage current evaluation of a single-phase transformerless PV inverter connected to the grid," inProc. 22nd IEEE Annu. Appl. Power Electron. Conf., Mar. 2007, pp. 907–912

[18] O. Lopez et al., "Eliminating ground current in a transformerless photovoltaic application," IEEE Trans. Energy Convers., vol. 25, no. 1, pp. 140–147, Mar. 2010.

[19] G. Vazquez, P. R. M. Rodriguez, G. Escobar, J. M. Sosa, and R. M. Mendez, "A PWM method for single-phase cascade multilevel inverters to reduce leakage ground current in transformerless PV systems," Int. Trans. Elect. Energy Syst., vol. 26, no. 11, pp. 2353–2369, Nov. 2016.

[20] M. Killi and S. Samanta, "Modified perturb and observe MPPT algorithm for drift avoidance in photovoltaic systems,"IEEE Trans. Ind. Electron., vol. 62, no. 9, pp. 5549–5559, Sep. 2015.

[21] M. Hedayati and V. John, "Filter configuration and PWM method for single phase inverters with reduced conducted EMI noise,"IEEE Trans. Ind. Appl., vol. 51, no. 4, pp. 3236–3243, Jul./Aug. 2015.

[22] D. Barater, G. Buticchi, E. Lorenzani, and C. Concari, "Active commonmode filter for ground leakage current reduction in grid-connected PV converters operating with arbitrary power factor,"IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3940–3950, Aug. 2014.

[23] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 184–191, Jan. 2011.

[24] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, and M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies," IEEE Trans. Power Electron., vol. 24, no. 9, pp. 2202–2211, Sep. 2009.

[25] T. K. S. Freddy, N. A. Rahim, W. P. Hew, and H. S. Che, "Modulation techniques to reduce

leakage current in three-phase transformerless H7 photovoltaic inverter,"IEEE Trans. Ind. Electron., vol. 62, no. 1, pp. 322–331, Jan. 2015.

[26] M. Islam and S. Mekhilef, "Efficient transformerless MOSFET inverter for grid-tied photovoltaic system,"IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6305–6316, Sep. 2016. [27] F. Wu, X. Li, F. Feng, and H.B.Gooi, "Modified cascaded multilevel gridconnected inverter to enhance european efficiency and several extended topologies," IEEE Trans. Ind. Electron., vol. 11, no. 6, pp. 1358–1365, Oct. 2013.

[28] S. Clemente, "A simple tool for the selection of IGBTs for motor drives and UPSs," inProc. 10th Annu. Appl. Power Electron. Conf. Expo., Mar. 1995, pp. 755–764

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