A NINE-LEVEL INVERTER EMPLOYING ONE VOLTAGE SOURCE AND REDUCED COMPONENTS IN AC POWER SOURCE

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Abstract—Increasing demands for power supplies have contributed to the population of high-frequency ac (HFAC) power distribution system (PDS), and in order to increase the power capacity, multilevel inverters (MLIs) frequently serving as the high-frequency (HF) source-stage have obtained a prominent development. Existing MLIs commonly use more than one voltage source or a great number of power devices to enlarge the level numbers, and HF modulation (HFM) methods are usually adopted to decrease the total harmonic distortion (THD). All of these have increased the complexity and decreased the efficiency for the conversion from dc to HF ac. In this paper, a nine-level inverter employing only one input source and fewer components is proposed for HFAC PDS. It makes full use of the conversion of series and parallel connections of one voltage source to realize nine output levels, thus lower THD can be obtained without HFM methods.

Index Term – Nine – Level Inverter, one voltage sources.

I. INTRODUCTION

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility application require medium voltage and MW power level. For a medium voltage grid, it is troublesome to connect one power semiconductor switch directly. High power and medium voltage inverter has recently become a research focus so far as known there are many problems in conventional two level inverter in the high power application. Multilevel inverters have been gained more attention for high power application, which can operate at high switching frequencies while producing lower order harmonic components. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for a high power application. There are several topologies available such as neutral point or diode clamped inverter, flying capacitor based multilevel inverter, cascaded H-bridge multilevel inverter and hybrid H- bridge multilevel inverter. The main disadvantage still exists in diode clamped multilevel inverter topology, which restricts the use of it to the high power range of operation. In flying capacitor multilevel inverter large numbers of capacitors are needed. The first topology

introduced is the series H-bridge design in which several configurations have been obtained. This topology consists of series power conversion cells which form the cascaded H- bridge multilevel inverter and power levels will be scaled easily.

An apparent disadvantage of this topology is large number of isolated voltage required to supply each cell. The proposed topology for multilevel inverter has a high number of steps associated with a low number of power switches. In addition for producing all the levels (odd and even) at the output voltage, a procedure for calculating required DC voltage source is proposed .In this topology Pulse width modulation technique is employed. However, the number of power devices and input dc sources multiplies when outputting more voltage levels. Several simplified topologies have been proposed in recent years to overcome the shortcomings of the traditional ones. However, they have the common disadvantage that symmetric or asymmetric dc inputs are needed. A single phase grid-connected inverter was proposed. However, the limited five output levels will lead to more output harmonics. A seven-level pulse width modulation inverter was proposed in which three capacitors are connected in series and then paralleled with the dc source to obtain extra ±1/3Vdc and ±2/3Vdc voltage levels. However, the capacitor voltages are in unbalancing conditions, thus increasing the control complexity. Meanwhile, both topologies in adopt the multicarrier modulation method to decrease the THD of the staircase outputs. The high switching frequency makes them unsuitable for HFAC PDS. A grid-connected converter topology was proposed with only one voltage source, a FC and eight switches. It can output nine levels exactly when the HFM strategy keeps the capacitor voltage at a desired level such as 1/3Vdc , which is indeed difficult to be realized without any auxiliary charging circuit, and the literature merely presents the experimental results from a seven-level prototype. Moreover, the HFM has limited the proposed topology to low-frequency (LF) occasions only. A series of step-up multilevel topologies was proposed based on switched-capacitor (SC) techniques. They can be used as HF power sources. However, more dc sources or more components are required to accomplish higher number of output voltage levels. The power switches in the backend H-bridges bear the sharply cumulative voltage levels from the SC frontends, and the extremely high-voltage stress has limited their applicability to low-input occasions only.

II. EXISTING SYSTEM

The general structure of cascaded multilevel inverter for single phase consists of three voltage sources as shown in fig. 1. Each voltage source V_{s1}, V_{s2} and V_{s3} is connected in cascade with other sources via a special H-bridge circuit. Each H-bridge consists of four active switching elements in order to make the output voltage source in positive or negative polarity or simply zero volts depending on the switching condition of the switches. A conventional multilevel power inverter topology employs multiple/link voltage of equal magnitudes. It is fairly easy to generalize the number of distinct levels The number of sources S or H-bridges and the associated number output level can be written as follows

$N_{level} = 2S+1$

For example if S=3, the output wave form has 7

levels (±3, ±2, ±1 and 0). The voltage on each stage can be calculated by using the equation below,

$V_{si} = 1V_{dc}$ ($i=1, 2, 3\ldots\ldots$) The number of switches used in this topology is expressed as,

$N_{switch} = 4S$

The advantages of cascaded multilevel inverter are modularized layout of series H-bridges and packaging. This will enable the manufacturing process to be done more quickly and cheaply. Drawbacks of this topology are requirement of a separate DC source for each of the H-bridges and involvement of high number of semiconductor switches.

Fig. 2 shows the output voltage waveform of a seven level cascaded inverter with three separate DC sources.

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PWM technique is extensively used for eliminating harmful low-order harmonics in input, output voltage and current of static power. In PWM control, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. In this proposed multilevel inverter multiple pulse width modulation is used. This involves several number of pulses for each half cycle.

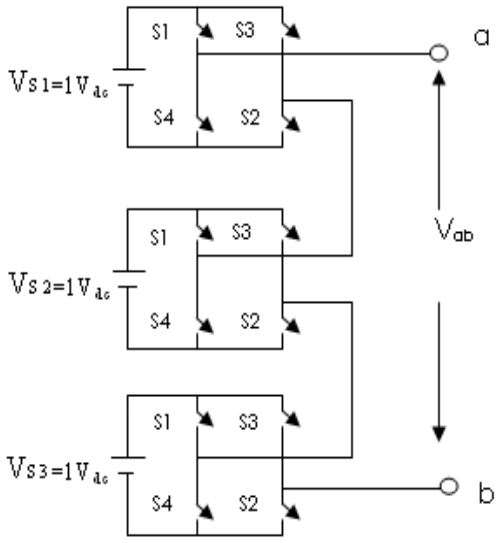

Fig .1.Topology for Cascaded H-bridge Multilevel Inverter

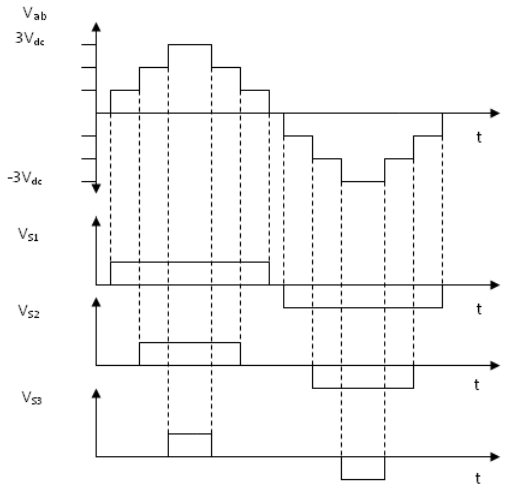

Fig. 2. Typical output waveform for cascaded multilevel inverter

III. PROPOSED NINE-LEVEL INVERTER

A. Circuit Topology

Fig. 3 shows the proposed nine-level inverter, which consists of two stages. The circuit in the frontend is a developed SC circuit (DSCC), which is different from the basic SC cells in that it can output more voltage levels with relatively fewer components. An H-bridge circuit (HBC) is used in the backend to change the polarity of the frontend output. In ideal circumstance, the proposed inverter has nine output voltage levels: 9,7, 5 , 3 and 0, and to achieve this goal, only one dc voltage source, four capacitors, and seven power switches are needed.

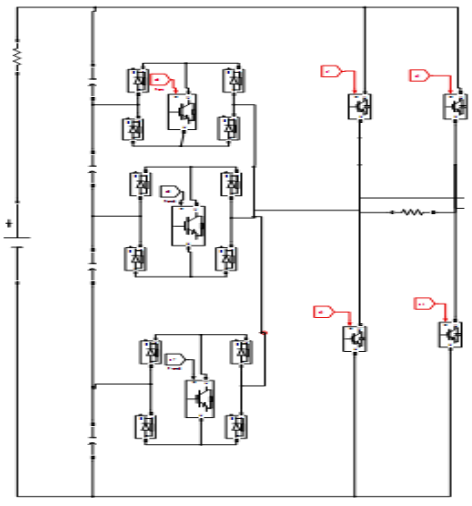

Fig. 3 Developed SC circuit (DSCC)

B. Structure of HFAC using MLI

HFAC PDS is usually composed of two stages: a high- frequency (HF) multilevel inverter (MLI) or a resonant inverter as the source side and several ac/ac or ac/dc voltage-regulation modules as the load side. In order to raise the power capacity, one of the most popular methods of the source side is to con- nect multiple resonant inverters in series or in parallel, while the control for the HF synchronizations of both amplitudes and phases will become extremely complicated. In contrast, using a HF MLI as the power source is a preferable solution with larger power capacity and lower switch stress. In HFAC PDS as shown in Fig. 3, a HF MLI is employed to transform the dc voltage source from the batteries, fuel cells, or photovoltaic cells into a HF staircase output, and the more number of voltage levels is significant to decrease the total harmonic distortion (THD) and electromagnetic interference, thus simplifying the design of output filters. However, the level number is restricted by the complexity of the MLI. The output frequency of the HF inverter usually ranges from 400 Hz to 50 kHz . As a result, the HF modulation (HFM) methods represented by multicarrier phase disposition are no longer suitable, as the excessively high switching frequency and so-caused switching loss are un- bearable for HF applications. In other words, the fundamental- frequency modulation (FFM) methods will have to be adopted in HF fields, and the further discussions are necessary to customize a HF MLI that can output sufficient number of voltage levels with a simplified structure to increase the efficiency and decrease the THD for HF applications.

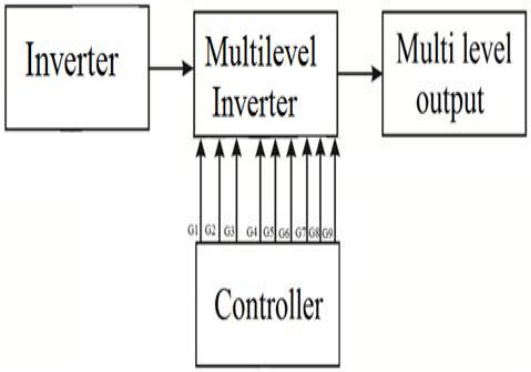

Fig.4 Structure of HFAC Using MLI

More levels can be obtained by increasing the number of power devices. However, both the circuit configurations and their controls will become extremely complicated along with the increasing number of voltage levels. Additionally, the capacitors' imbalance is another problem needed to be solved. The CHB inverter increases the output voltage levels and simplifies the modulation by the combination of H-bridge cells. From Table I and Fig. 3 the four capacitors are charged and discharged in series at levels ±Vdc and ±2Vdc , respectively, and in these intervals, they share the same charging or discharging currents. At levels ±Vdc /2 and ±3Vdc /2, the four capacitors are connected in parallel. As a result, the voltages on them get balanced. At level 0,

the four capacitors' voltages remain un- changed. Overall, the proposed nine-level inverter is equipped with the self-voltage balancing ability, thus simplifying the driving circuits and modulation algorithms . When the load is inductive, the current will flow in the opposite direction, and Fig. 3 show the reverse current paths for each voltage level in the positive half cycle. It can be found that the output voltage levels remain the same regardless of the directions of the load. It can be observed from Table I that the proposed nine-level inverter needs only one voltage source and the fewest components, which means less installation space and higher

Table.1 Switching operation of Multilevel Inverter

Level	S1	S2	S3	S4	S5	S6	S7
9	1	0	0	1	0	0	0
7	0	0	0	1	1	0	0
5	0	0	0	1	0	1	0
3	0	0	0	1	0	0	1
0	1	0	1	1	0	0	0
0	0	1	0	0	0	0	0
-3	0	1	0	0	1	0	0
-5	0	1	0	0	0	1	0
-7	0	1	0	0	0	0	1
-9	0	1	1	0	0	0	0

Here, symbols of 1 or 0 in the switches column indicate that the switches are turned ON or turned OFF; symbols of 1 or 0 in the diodes column indicate that the diodes are forward passed or reverse biased.

conversion efficiency. The PIV of the proposed inverter is merely half of those in single-input-source topologies proposed in which has broadened its application range. It is notable that the topology in range. It is notable that the topology is unable to supply inductive loads, although it needs eight switches only, and to address this deficiency, at least ten switches are needed. In other words, the proposed MLI also has the greatest advantage in terms of the switch number.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Power simulation (PSIM) simulation is conducted to verify the performance of the proposed nine-level inverter, and the de- tailed simulation parameters are shown in Table I. The output frequency is set to 1 kHz, which is the optimized frequency for HFAC. Fig. 5 shows the simulation waveforms of output voltages and load currents when supplying different types of loads.

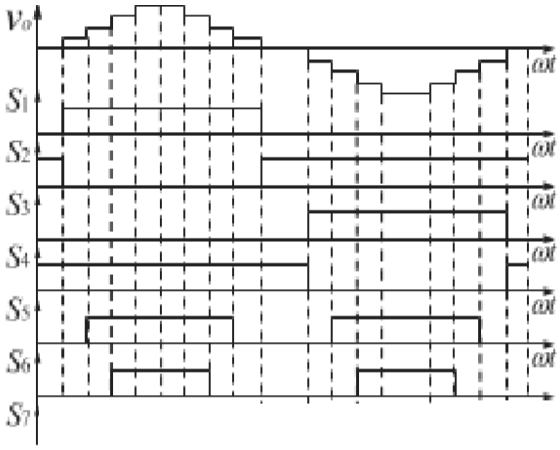

Fig. 5 Simulation output

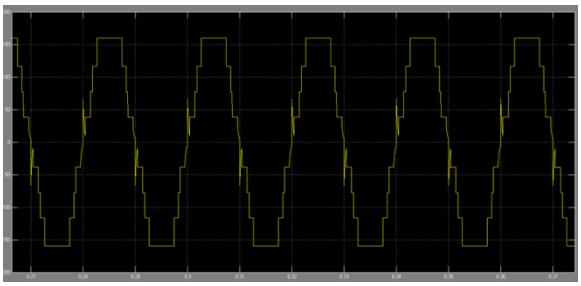

Fig.6 Matlab Waveform

Fig.5 & 6 shows the experimental waveforms of the voltages over switches. The maximum PIV is approximately 160 V, which is twice the voltage of the input dc source. The less voltage stress indicates that the proposed inverter has larger application range than the topologies listed in Table I. Overall, the proposed HF inverter can output nine levels using only one voltage source and fewer components. The staircase output has less harmonics, although FFM method is adopted, thus the switching loss is decreased greatly. Moreover,

the proposed inverter with two capacitors is equipped with the self-voltage balancing ability, which simplifies the control algorithms. Consequently, the proposed nine-level inverter is a better choice of HFAC power source.

V. CONCLUSION

In this paper, a novel nine-level inverter is proposed for HFAC PDS. Compared with the existing topologies, the proposed topology can achieve nine-level staircase output with only one voltage source, fewer power devices and relatively less voltage stress. All these have enlarged its application scopes. Voltage balance problem is avoided by the inherent self-voltage balancing ability, which has simplified the modulation circuits or algorithms, and the lower THD of 3.13% is realized without using HFM methods. As a result, the switching loss is significantly reduced

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