DESIGN OF DIGITAL CONTROLLED SMPS

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ABSTRACT - A power supply is an essential part of almost every electronic device and the current trend is towards the miniaturization of these devices. It is thus desirable to also attempt to reduce the size of the power supply and it is possible to achieve this objective by increasing the power density which is attainable by decreasing the size of the passive/energy storage components such as the inductors, capacitors and the transformer. The size of these components can also be decreased by increasing the switching frequencies. Linear power supplies use bulky line frequency transformers and heat sinks and are thus not capable of providing a significant opportunity to reduce their size and weight. Switch Mode Power Supplies (SMPS) use higher switching frequencies, which replaces the bulky line frequency magnetic by smaller high frequency magnetic, which are then able to offer significant size and weight reductions. The efficiency and size of the SMPS depends on a suitable switching frequency. Previously, the SMPS were implemented using bipolar power devices and their switching frequency range was limited to a range of a few kHz. With the availability of modern and efficient power MOSFETs, it is possible to switch the SMPS from several kHz to a MHz range. In addition, core based transformers were previously used in SMPS. frequency and power efficient isolated converters.

Keywords: Switched Mode Power Supply, Power Factor Correcting, Phase-Shifted Full Bridge converter, Digital Signal Processing.

I. INTRODUCTION

In recent years, the switching mode power supply (SMPS) system have been achieved the high power density and high performances by developed power semiconductor devices such as IGBT, MOS-FET and SiC. However, using the switching power semiconductor in the SMPS system, the problem of the switching loss and EMI/RFI noises have been closed up. This course produced the EMC limitation like the International Special Committee on Radio Interference (CISPR) and the harmonics limitation like the International Electro technical Commission (IEC). For keeping up with the limitation, the SMPS system must add its system to the noise filter and the metal and magnetic component shield for the EMI/RFI noises and to the PFC converter circuit and the large input filter for the input harmonic current. On the other hand, the power semiconductor device technology development can achieve the high frequency switching operation in the SMPS system. The increase of the switching losses have been occurred by this high frequency switching operation. Of course, the inductor and transformer size have been reduced by the high frequency switching, while the size of cooling fan could be huge because of the increase of the switching losses.

Our research target is to reduce the EMI/RFI noises and the switching losses in the SMPS system by only one method. The solution method is the soft switching technique. Using LC resonant phenomenon, this technique can minimize the switching power losses of the power semiconductor devices, and reduce their electrical dynamic and peak stresses, voltage and current surge-related EMI/RFI noises under high frequency switching strategy.

Thus, a new conceptual circuit configuration of the advanced forward type soft switching DC-DC converter which has the neutral point inductor connected auxiliary. The new advances in IC technology and a focus on digital power conversion from silicon providers have lead to the rapid development of Digital Signal Controller (DSC) for digital power applications. DSCs combine the control capability of a Microcontroller and the performance of a digital signal processor (DSP) in a single silicon chip and target applications in advanced digital control. DSC has adequate execution speed and advanced peripherals. For example, PWM peripherals must generate PWM signals with high resolution and support phase-shifted control. ADC peripherals must have high precision of conversions and support synchronized control. DSCs are beginning to play a major role in digital control of power electronics.

LINEAR REGULATED POWER SUPPLY

To make a simple linear power supply, use a transformer to step down the 120VAC to a lower voltage. Next, send the low voltage AC through a rectifier to make it DC and use a capacitor to smooth out the ripples in the DC. Finally, add a voltage regulator to regulate the output voltage

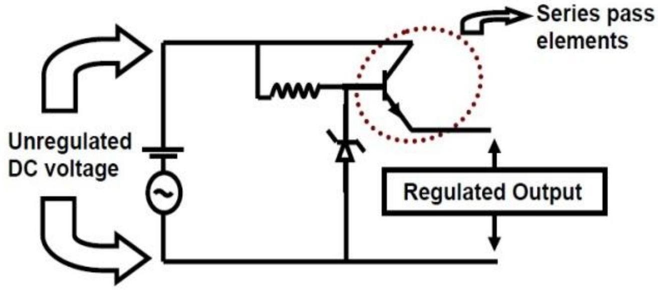

Fig.1 Linear regulated power supply

FORWARD TYPE SOFT SWITCHING DC-DC CONVERTER

The typical switching mode power supply circuit configuration of our research target is shown in Fig.1.a. We have modified the part of DC-DC converter to achieve the complete soft switching operation in active power semiconductor devices of the forward converter. Fig.1.b shows the schematic configuration of the modified forward type soft switching DC-DC converter with a neutral point inductor connected auxiliary resonant snubber (NPC-ARS) circuit. The proposed NPC-ARS circuit consist of an active power semiconductor devices; Sa, a resonant capacitor Crl, two power diode Da1 and Da2. Using this NPC-ARS circuit, the zero voltage soft switching (ZVS) turn off or the zero current soft switching (ZCS) turn on can be achieved in main switching device S1 and ZCS turn on and turn off be in auxiliary switch Sa. So that, the switching losses in each active power semiconductor device will be zero completely.

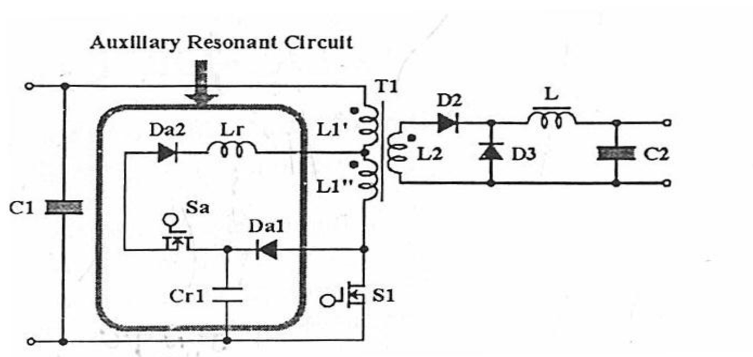

Fig.1.b Forward type soft switching DC-DC converter with a neutral point inductor connected auxiliary resonant snubber (NPC-ARS) circuit

II. TOPOLOGY STRUCTURE OF SWITCHING POWER CONVERTER

The topology structure of switching power converter is mainly composed of single-ended feedback high frequency transformers, switching power tube, output rectifier filter circuit, etc. In this paper, the switching power converter is designed to be an interrupted and discontinuous conducting energy transmission converter. The process of the power transmission includes two aspects: energy storage and transmission.

Digital arithmetic of PFC control

To accomplish the preceding tasks, a new PFC arithmetic has been developed, consisting of three parts: 1) Outer voltage loop, which regulates the output voltage; 2) Reference arithmetic, which generates the sinusoidal current reference and implements input voltage feed forward ; 3) Inner current loop, which regulates the input current to follow the current reference. Digital arithmetic structure of PFC control

In conventional analog implementation, current reference is proportional to the input voltage, and the squared value of input voltage is introduced as reciprocal in order to make the constant power feed forward. Equation describes the generation of the current reference, in which, Km is the proportion coefficient, Vvo is the output of voltage regulator, Vs is the amplitude of the input voltage, Vff is the RMS value of input voltage.

In analog arithmetic, since the input voltage is used to generate the current reference the ripple of input voltage is introduced to the current control, which deteriorates the control performance. In addition, function of division-and square increases computation time.

OPERATION OF THE DESIGNED CIRCUIT

A complete schematic of the SMPS designed to meet the required specifications is shown in figure 4-1. The design will be discussed by dividing the complete circuit into its building blocks constituent components .Figure 2 (a) shows the input voltage and filtering circuit. The choke is used to stop fast rise time transients from the car electrical system from disturbing the circuit and also prevent the switching noise generated from interfering with other stuff in the car like to radio and engine management computer in the car. The capacitor and choke combination form a low pass filter hence regulating the input. Figure 4-2 (b) shows the power stage of the design a single MOSFET and the pairs' drive requirements can be optimized using less control circuitry. The MOSFETs' source is connected to the ground to allow the MOSFET s to be driven directly by the control circuitry without isolation to permit a wide range of pulse width for control of the output. Q1, Q2 and Q3, Q4 drive the transformer T1 with combined duty cycle of 96% leaving 4% dead time to prevent power loss and component stress due to overlapping on times.

The control circuitry is shown in figure 4-3. The heart of this circuit is an UCC38C$X pulse width modulator IC whose outputs are ideally suited to driving power MOSFETs while providing the necessary oscillator, amplifier and voltage reference. The IC directly drives the MOSFETs while incorporating the feedback amplifier and soft start control. RT and CT set the oscillation at 100KHz. Due to the push-pull attributes, the transformer runs at 50 KHz. Because the gates of power MOSFETs can be damaged by voltages exceeding +20V, the supply voltage for the output stage of the IC is limited. This function is performed by the zener diode D1, C9 and C10. When the voltage exceeds 15V the zener diode is reverse biased thus pulling VCC and VC to ground, switching off the outputs.

Capacitor Css is connected to the soft start input pin of the IC. This circuit reduces stress on the supply s' components by gradually increasing the pulse width during turn on from zero to 40% duty cycle. Figure 4-5 shows the secondary of the transformer and its associated rectifiers and capacitors. C1, C2, C5, C6 are high ripple current capacitors capable of handling current ripples from T1 and the ripples currents created by the load. A small capacitance C3,C4 is placed in shunt to these to filter the output.

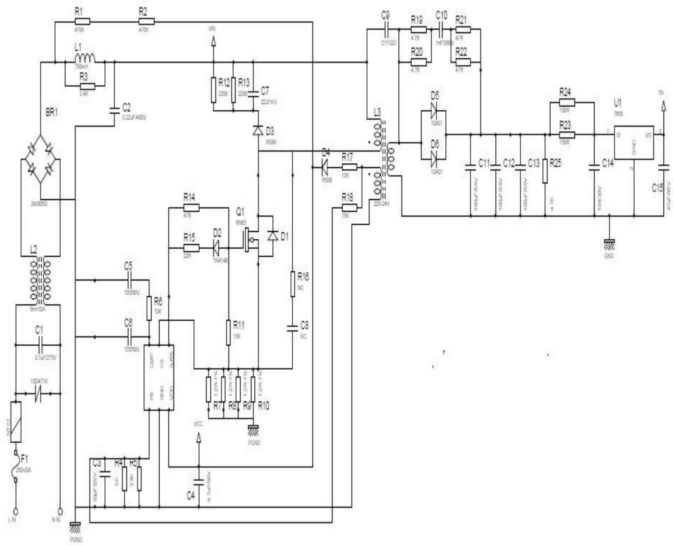

Fig. 2 The complete power supply schematic

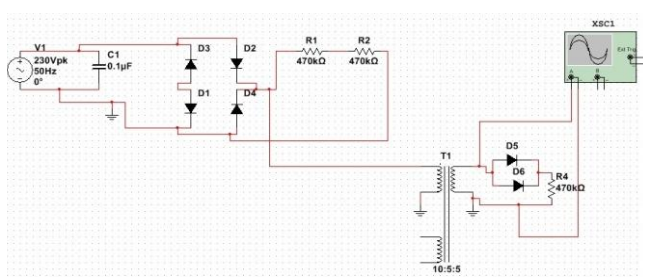

Fig. 2 (a)The power stage

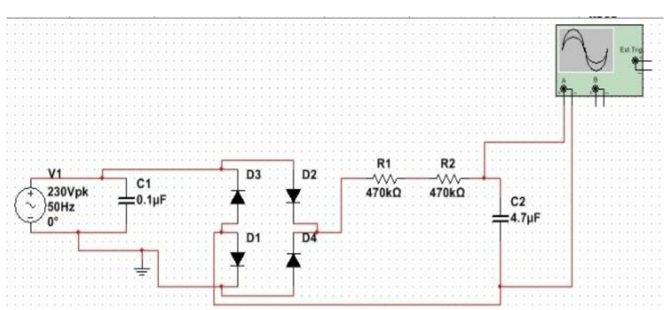

Fig. 2 (b) The input circuit

III. RESULTS AND ANALYSIS

A simulation of the complete design was done using emulator software (Multisim 14.1) since at the time of presenting the report not all the components had been acquired. Thus results from the simulation were used in the analysis. The load was varied in random steps and the output voltage and current recorded.

A simulated output of the output load against the output voltage was then drawn. As seen from these waveforms, the output of the power supply remains relatively constant with increased loading giving a voltage difference of about two volts between minimum loading and maximum load.

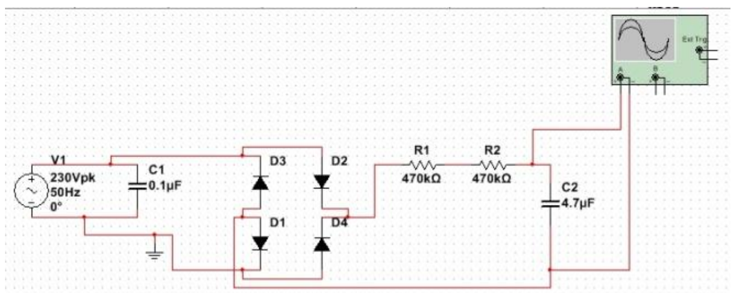

Fig. 3 circuit path – I

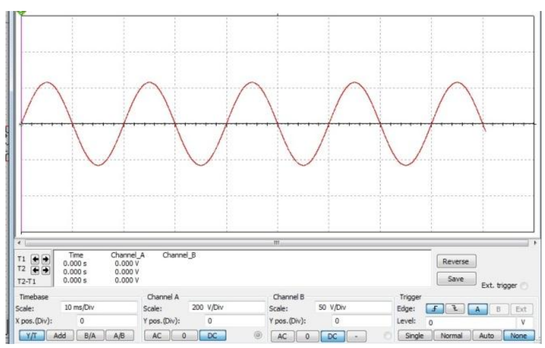

Fig. 5 Input Waveform

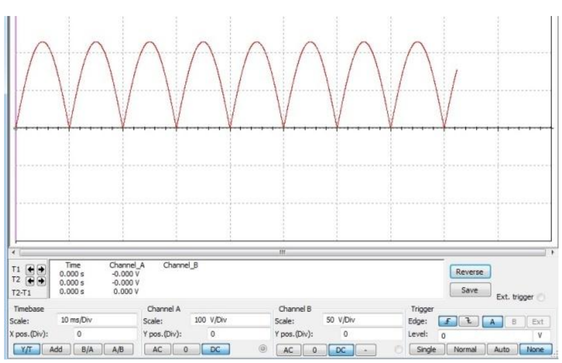

Fig. 6 FWR waveform

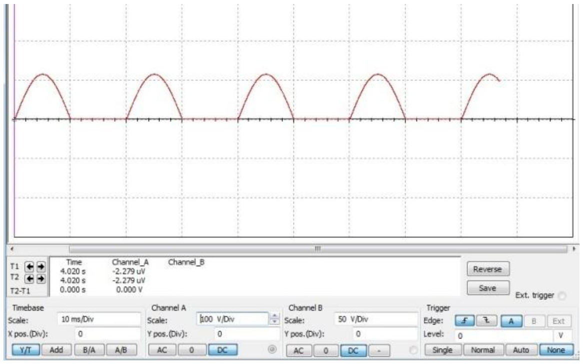

Fig. 7 Output of step down transformer

IV. CONCLUSION

The results obtained in the simulation show that the efficiency of the power supply depends on the loading. The system was found to have an average efficiency of 90.41% which meets the design objectives of a high efficiency converter. The supply should be operating a load between 50-100% of the rated load to achieve maximum efficiency. Since in the simulation ideal conditions were used the system efficiency is expected to slightly drop when implemented on the physical board due to impedances introduced by the tracks on the printed circuit board as well as coupling reactance

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