CONCEDE THRESHOLD ANALYSIS FOR LOGIC GATE DESIGNS

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ABSTRACT: In this paper, an automatic test pattern generation approach is utilized to detect delay defects in a circuit which consisting of current mode threshold logic gates. Current mode is a popular CMOS-based implementation of threshold logic functions, where the gate delay is based on the sensor size. A new implementation of current mode threshold functions for improving gate delay and switching energy is presented in this paper. The proposed design consists of Pass Transistor Logic-Gate Diffusion Input (PTL-GDI) circuit. Experimental results show the efficiency of the proposed method. This design does not compromise for the speed, as the delay of the proposed system is minimized thus the overall delay becomes less. By using proposed system, the constant threshold values are obtained for different input voltages.

Keywords: Current mode, operating speed, sensor sizing, and threshold logic gates (TLGs)

I. INTRODUCTION

Threshold logic gates (TLG) are an alluring option for executing computerized circuits. Procedures for execution of circuits utilizing TLG end up accessible and in this way the union of effective TLG based circuits winds up possible. A current issue is to streamline the execution of a TLG Gate by choosing fitting transistor sizes. A choice to tedious thorough Zest recreations is introduced and assessed. It depends on an investigative technique equipped for giving close ideal sensor sizes to the circuit executing the TLG. It is likewise equipped for giving the normal door delay without tedious recreation steps; in this way enhancing the execution of TLG based blend philosophies.

It is normal that the exponential funds in execution of advanced circuits because of parameter scaling will vanish soon. Elective advancements, for example, different esteemed rationale, limit rationale entryways, and others, can expand parallel preparing capacities.

Monostable-Bistable Change Rationale Component (Portable), neuron MOS, single electron innovation are couple of precedents of edge rationale door executions. An Edge Rationale Door (TLG) is a N-input gadget which computes the weighted aggregate of data sources. An essential TLG comprises of N-inputs, a weight an incentive for each info, and a limit weight. The entirety of the information weights is contrasted and the limit weight. On the off chance that it is more noteworthy than the edge weight, at that point the computerized yield of TLG is rationale high, and in the event that it is less it will be rationale zero. In the CMOS based execution considered in this paper, when the whole of the information weights is equivalent to the limit weight, at that point the logic gate is in unclear state. Weights are chosen with the goal that this case is kept away from.

This paper considers executions of edge rationale capacities utilizing current mode. This is a prominent CMOS-based methodology. All present mode usage techniques considered in this paper comprise of the differential part. The quantity of transistors in the differential

part is steady and does not rely upon the actualized work. The quantity of transistors in the differential part relies upon the total of information weights and the limit weight. There exist two methodologies for actualizing current mode TLGs: the current mode Threshold Logic Gate (CMTLG) and the Differential current mode logic (DCML).

II.EXISTED SYSTEM

Current mode Threshold Logic Gate (CMTLG) is a CMOS based usage of TLG appeared in Figure 1. The CMTLG can be the differential part. The differential part can be subdivided into two sections, the threshold part and the input part. In the threshold part and the input part all the transistors are associated in parallel. The transistors in the threshold part are dependably ON and the aggregate current moving through the threshold part is represented as Threshold current. The number of PMOS active (ON) in the input part depends on the input pattern applied. The total current passing through the input side for a particular input pattern is represented as the Active Current. The nodes connecting the differential part on the input side and the threshold side are M1 and M2, respectively and nodes O and OB are the output nodes and are shown in Figure 1.

The nodes connecting the differential part on the input side and the threshold side are M1 and M2. Output voltages and their difference in the two clock phases for CMTLG respectively. The part has three Pmos transistors P1, P2, P3, and four nMOS transistors N1, N2, N3, and N4 as shown in Fig. 1.

The operation of the current mode Threshold Logic Gate (CMTLG) is classified into two phases: the equalization phase and the evaluation phase. When the applied clock (clk) to the CMTLG is high, then the circuit is in the equalization phase. When clk is low, then the circuit is in the evaluation phase. In the equalization phase, transistors N1 and N2 are ON, nodes M1 and M2 have the same voltage because of transistor N1, and nodes O and O B have the same voltage because of transistor N2. In the evaluation phase, transistorsN1 and N2 are OFF, and if the threshold current is less than the active current, then the voltage at node O rises faster than that at node O B. If during the evaluation phase the threshold current exceeds the active current, then the voltage at node O B rises faster than that at node O.

$$O = \begin{cases} 1 & \text{if } \sum_{i=1}^{n} w_i x_i \geq w_o \\ 0 & \text{otherwise} \end{cases}$$

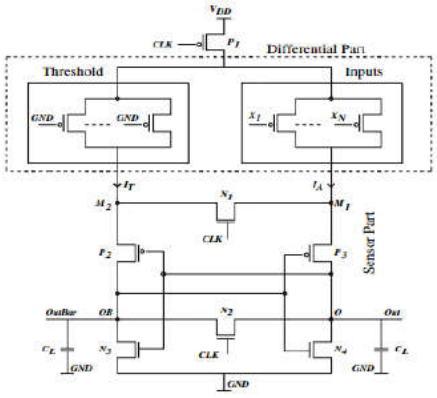

Figure 1: Current Mode Threshold Logic Gate

An alternative differential clock threshold logic implementation is presented and it is referred to as the differential current mode

logic (DCML) approach. The block diagram of DCML is shown in Fig.2. It is the differential part. The differential part consists of four pMOS transistors, denoted as P1–P4 and six nMOS transistors, denoted as N1–N6. The load capacitance CL is applied to both the output nodes O and OB.

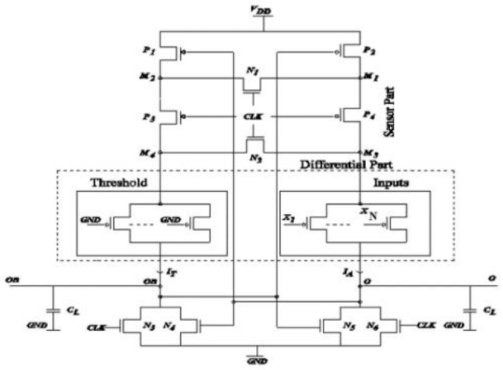

Fig. 2: Block diagram of differential current mode logic.

The applied clock is divided into two phases: when the clock is high the TLG is in the equalization phase and when it is low it operates on the evaluation phase. In the equalization phase, nMOS transistors N1, N2, N3, and N6 are active. Transistor N1 equalizes the voltage at nodes M1 and M2. Similarly, transistor N2 equalizes the voltage at nodes M3 and M4. In the equalization phase, transistors N6 and N3 are active and there exists a discharge path for nodes O and OB of Fig. 2. If there is a voltage difference at nodes O and OB, during the evaluation phase, then it will identify the voltage difference and it will boost the voltage at the output nodes O and OB to a desired voltage. When the active current is greater than the threshold current, then the voltage at the output node O rises faster than the voltage at node OB. As a result, high voltage is obtained at node O and low voltage is obtained at node OB. When threshold current is greater than active current, then the voltage at OB rises faster than the voltage at O and low voltage results at OB.

The CMTLG assumes that all inputs have minimum weights. If a TLG requires weight wi >1 (greater than minimum weight) for some input i, then as an alternative we can implement the function with wi minimum weight inputs for CMTLG of Figure 1.We consider an N-input CMTLG that can be used to implement different TLG functions for a given value of N and T. This section shows how to identify optimum size for the N-input CMTLG, so that the delay of any TLG implemented by the N-input CMTLG is minimized.

A new TLG implementation is proposed. It is called Dual Clock based Current Mode Logic (DCCML). As the name indicates, two clocks are used to achieve low power consumption and high speed. The approach consists of two steps. First, the set of functions that can be implemented using CMTLG for a given input configuration (number of inputs N and threshold T) are grouped in to equivalent classes. We show that when T+1 input are active on the input side then the TLG exhibits its worst delay. The block diagram DCCML is shown in Figure 3. The differential block is further divided into four blocks: the positive threshold, the negative inputs, the negative threshold, and the positive inputs.

All the transistors in the differential block are equalized pMOS transistors and are connected in parallel, as shown in Fig. 3. The differential block consists of six

pMOS transistors P1⋯P6 and three nMOS transistorsN1, N2, and N3. The gates of transistors P1 and N1 are connected to Clk1 and the gates of transistors P2, P5, and P6 are connected to Clk2. Transistor N1 acts as an equalizing transistor and it equalizes the voltage at nodes OP and OPB. Transistors P5 and P6 isolate the differential block. The transistors in the positive threshold and negative threshold are always active. Transistors in the positive and negative inputs blocks are active depending upon the input pattern applied. The input pattern applied for the positive inputs block is denoted by {x1, x2, . . . , xI . Let N denote the number of inputs, and I denote the number of positive inputs. Then the number of negative inputs is N–I. The input pattern applied for the negative inputs block is denoted by {xI+1, xI+2, . . . , xN.

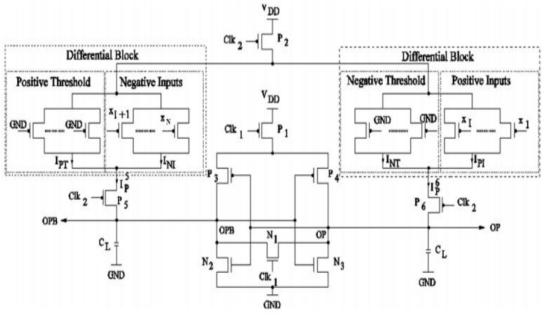

Fig. 3: Block diagram of DCCML TLG

Consider a function f, with a possible weight configuration {w1, w2: wT, w3, w4} = {2, 2:3, −1, −1}.In the given weight configuration, we have two positive weights w1 and w2 and two negative weights w3 and w4. Weights w1 and w2 are implemented in the positive inputs section and weights w3 and w4 are implemented in the negative inputs section. The threshold weight wT is implemented in the positive threshold.

The current through the four blocks (positive threshold, negative inputs, negative threshold, and positive inputs. Nodes OP and OPB are the output nodes. The load capacitance is denoted by CL. The operation is divided into three phases: the equalization phase, the pre-evaluation phase, and the final-evaluation phase. When clocks Clk1 and Clk2 are high, then the circuit is in the equalization phase. When clocks Clk1 and Clk2are low, then the circuit is in the pre-evaluation phase. When Clk1 is low and Clk2 is high, then the circuit is in the final evaluation phase. It is noted that when the two clocks are not completely aligned the operation of the gate is not affected.

III. PROPOSED SYSTEM

The low power VLSI design is significant because of portable electronic products. The efficient way for reducing the power consumption is by reduce the threshold voltage and reduction in supply voltages. The performance of digital circuits is improved by enhancing the performance of circuits hence; it is attracting much attention of researchers.

The various techniques have been reported and they all concentrated on reducing the area, power dissipation and delay. The transistor count will largely affect the complexity of many designs like ALU, multiplier and processors. The area and complexity can be minimized by reducing the transistor count. The speed is based on transistor size, delay in the critical path and parasitic capacitance. Different researchers utilized various techniques for reducing the delay, power and area. Although they perform the similar function, each technique has their own benefits and disadvantages. Some of them

used one logic style for the whole full adder and others used a combination of different logic styles.

Today all the VLSI circuits operates on low power with high speed. The Gate Diffusion Input (GDI) technology and Pass Transistor Logic (PTL) technology are used achieve low power operation with minimum area consumption. In this project PTL-GDI logic, which consists of 10 transistor. The ALU is basic unit of central processing unit which performs all the arithmetic and logical operations. Thus ALU is used in the microprocessor and act as critical component of the microprocessor mostly all the digital circuits uses ALU. Since the digital design is amazing and broad field. Achieving of low power with high speed in digital design is the challenging task makes digital design as the future growing business. The applications of digital design present in our daily life like computer, calculator, camera, mobile phone, etc.

Large gains, in terms of performance and silicon area, have been made for digital processors, microprocessors, DSPs (Digital Signal Processors), ASICs (Application Specific integrated circuits), etc. In general, "small area" and "high performance" are two constraints for any design. The IC designer's activities have been involved in trading off these constraints. In fact, power considerations have been the ultimate design criteria in special portable applications such as wrist watches and pacemakers for a long time. The objective in these applications is minimum power for maximum battery life time. The explosive growth in laptop and portable systems and in cellular network has identified the research effort in low power electronics. High power system may often lead to several circuit damages .Low power leads smaller power supplies and less expansive batteries. Low power is not only needed for portable application but also to reduce power of high performance system. Generally the PTL GDI structure includes two types; they are static and dynamic types. The static type is more reliable and consumes less power. Dynamic circuit is fast, some times more compact then static and suffering from charge sharing problem.

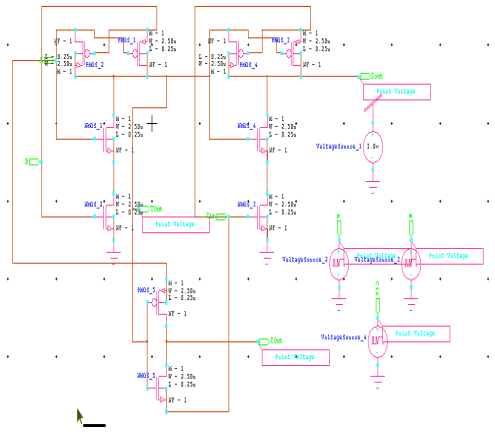

Fig 4: PTL- GDI CIRCUIT

The figure 4 shows the Pass Transistor Logic Gate Diffusion Input (PTL GDI) circuit. The sum output is obtained using the PTL logic and the carry output is obtained by GDI logic. It is a low power circuit design. It allows reducing power consumption. It reduces propagation delay and reduces area of digital circuit. It maintains low complexity of logic design

IV. RESULTS

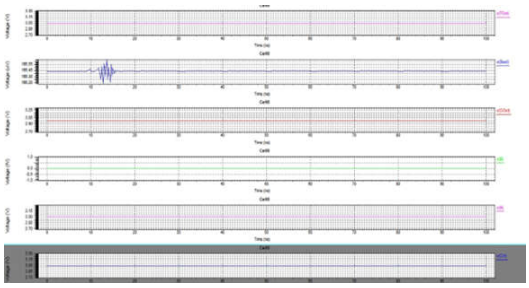

Fig.5: Output waveform

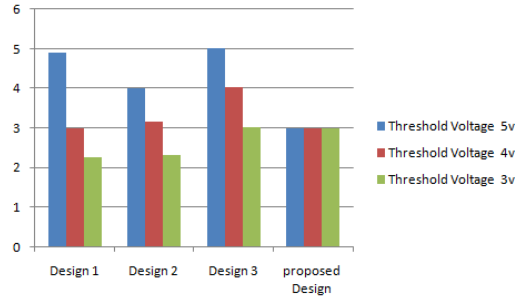

Fig.6: Comparison Graph for threshold voltage

TABLE I
Comparison of the threshold values and delay with the proposed system

DESIGN	VOLTAGES	THRESHOLD VALUE	DELAY
1	5V	4.9V	1.81S
	4V	3V	2.12S
	3V	2.25V	1.59S
2	5V	4V	1.69S
	4V	3.15V	1.57S
	3V	2.30V	1.34S
3	5V	5.015V	2.29S
	4V	4.015V	1.84S
	3V	3.015V	1.51S
PROPOSED DESIGN	5V	3V	1.98S
	4V	3V	1.61S
	3V	3V	1.75S

V.CONCLUSION

In this paper, we exhibited a present mode threshold logic gate circuits which are composed utilizing CMOS innovation. The proposed PTL-GDI configuration gives huge decrease in power utilization. The schematics are drawn and recreated. The defer result demonstrates that proposed circuit gives less deferral. The outcome demonstrates that the speed for the proposed configuration is high and diminishes the postponement than the existed outline. It has been seen that the defer increments to the quantity of contributions of current mode TLG. This came about to the plan of current mode TLGs with vast number of information sources whose deferral is altogether not as much as conventional CMOS. Our proposed framework is steady because of the consistent limit voltage at various voltages. The outcomes demonstrates that proposed framework is high productive by steady threshold voltages.

VI.REFERENCES

[1] S. Bobba and I. N. Hajj, ―Current-mode thresholdlogic gates,‖ in Proc. IEEE ICCD, Sep. 2000, pp. 235–240.

[2] T. Ogawa, T. Hirose, T. Asai, and Y. Amemiya,―Threshold-logic devices consisting of subthresholdCMOS circuits,‖ IEICE Trans. Fundam. Electron.,Commun. Comput. Sci., vol. E92-A, no. 2, pp. 436–442, 2009.

[3] S. Muroga, Threshold Logic and Its Applications.New York, NY, USA: Wiley, 1971.

[4] W. Prost et al., ―Manufacturability and robustdesign of nanoelectronic logic circuits based onresonant tunnelling diodes,‖ Int. J. Circuit TheoryAppl., vol. 28, no. 6, pp. 537–552, Nov./Dec. 2000.

[5] S. Leshner, K. Berezowski, X. Yao, G.Chalivendra, S. Patel, and S. Vrudhula, ―A low power,high performance threshold logic-based standard cellmultiplier in 65 nm CMOS,‖ in Proc. IEEE Comput.Soc. Annu. Symp. VLSI, Lixouri, Greece, Jul. 2010,pp. 210–215.

[6] M. Sharad, D. Fan, and K. Roy. (2013). ―Ultra-lowenergy, highperformance dynamic resistive thresholdlogic.

[7] P. Celinski, J. F. López, S. Al-Sarawi, and D.Abbott, ―Low power, high speed,

charge recyclingCMOS threshold logic gate,‖ Electron. Lett., vol. 37,no. 17, pp. 1067–1069, Aug. 2001.

[8] S. Leshner and S. Vrudhula, ―Threshold logicelement having low leakage power and highperformance,‖ WO Patent 2009 102 948, Aug. 20,2009.

[9] C.B.Dara, T. Haniotakis, and S. Tragoudas, "Delay analysis for an N-input current mode threshold logic gate," in proc. IEEE Comput. Soc. Annu. Symp. VLSI(ISVLSI), Aug. 2012,pp. 344-349.

[10] A. Neutzling, J. M. Matos, A. Mishchenko, R. Ribas, and A. I. Resis,"Threshold logic synthesis based on cut pruning," in Proc. ICCAD, Nov. 2015 , pp.2004.

[11] A. K. Palaniswamy, T. Haniotakis, and S. Tragoudas, "ATPG for delay defects in current mode threshold logic circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. PP, no. 99, pp. 1–1.

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