4-2 COMPRESSOR STRATEGY THROUGH INNOVATIVE XOR-XNOR MODULE

G. Manasa*, T. Pradeep**

PG SCHOLAR*,ASSISTANT PROFESSOR**

DEPARTMENT OF ECE, VAAGDEVI ENGINEERING COLLEGE, BOLLIKUNTA, WARANGAL

ABSTRACT:

Imprecise computing is an attractive model for digital processing at nano metric scales. Inexact computing is particularly interesting for computer arithmetic designs. This work deals about the design and analysis of two new inaccurate 4-2 compressors for utilization in a multiplier. These designs rely on different features of compression, such that imprecision in computation is measured by the error rate and the so-called normalized error distance can meet with respect to circuit-based figures of merit of a design in terms of number of transistors, delay and power consumption. The proposed approximate compressors are proposed and analyzed in Dadda multiplier. Extensive simulation results are provided and an application of the approximate multipliers to image processing is presented. The results proposed designs shows that reduced power dissipation, delay and transistor count.

INTRODUCTION:

Commonly used multimedia applications have Digital Signal Processing (DSP) blocks as their backbone. Most of these DSP blocks implement the image and video processing algorithms, where the ultimate output is either an image or a video for human consumption [1]. The limited perception of human vision allows the outputs of these algorithms to be numerically approximate rather than accurate. This relaxation on numerical exactness provides some freedom to carry out imprecise or approximate computation. The freedom can be taken advantage of to come up with low-power designs at different levels of design abstraction, viz. logic, architecture, and algorithm. Methodologies for inexact computing rely on the feature that many applications can tolerate some loss of precision and therefore, the solution can tolerate some degree of uncertainty. However, inexact computing applications are mostly implemented using digital binary

logic circuits, thus operating with a high degree of predictability and precision. A framework based on a precise and specific implementation can still be used with a methodology that intrinsically has a lower degree of precision and an increasing uncertainty in operation [4]. Addition and multiplication are widely used operations in computer arithmetic for addition full-adder cells have been extensively analyzed for approximate computing. The paradigm of inexact computation relies on relaxing fully precise and completely deterministic building blocks such as a full adder when for example, implementing the bio-inspired systems. This allows nature inspired computation to redirect the existing design process of digital circuits and systems by taking advantage of a decrease in complexity and cost with possibly a potential increase in performance and power efficiency

EXACT COMPRESSOR

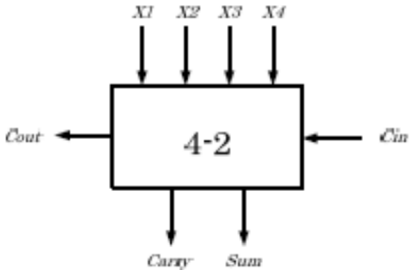

Fig.1. General Structure of 4-2 compressor

The following equation gives the outputs of 4-2 compressor, which table 1 show its truth table. The common implementation of a 4-2 compressor is accomplished by utilizing two full adders are shown in Fig. 3.3.

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus c_{in} \ldots\ldots (1)$$

$$C_{out} = (x1 \oplus x2)\, x3 + (x1 \oplus x2)'\, x1 \ldots (2)$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)\, c_{in} + (x1 \oplus x2 \oplus x3 \oplus x4)'\, x4 \ldots\ldots (3)$$

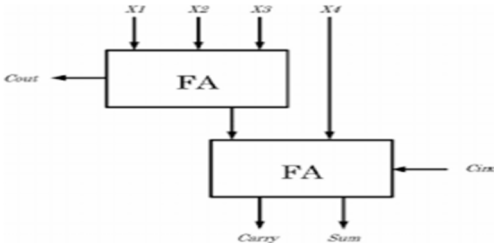

Fig.2. Implementation of 4-2 compressor

This design is not efficient because it produces at least 17 incorrect output of 32 possible combination that is error rate of this exact compressor design is above 53%.

Table 1: Truth table of exact 4-2 compressor

C_{in}	X4	X3	X2	X1	C_{out}	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

3. PROPOSED COMPRESSOR

3.1. Design 1

In Design 1, the carry is simplified to cin by changing the value of the other 8 outputs.

$$Carry` = C_{in} \quad \ldots\ldots (4)$$

$$Sum` = c_{in}` ((x1 \oplus x2)` + (x3 \oplus x4)`) \quad \ldots\ldots (5)$$

$$C_{out}` = ((x1\ x2)` + (x3\ x4)`) \quad \ldots\ldots (6)$$

Eqs. (4) - (6) are the logic expressions for the outputs of the first design of the approximate 4-2 compressor proposed in this manuscript. The gate level structure of the first proposed design (Fig.3) shows that the critical path of this compressorhas still a delay of 3Δ, so it is the same as for the exact compressor of Fig.2.

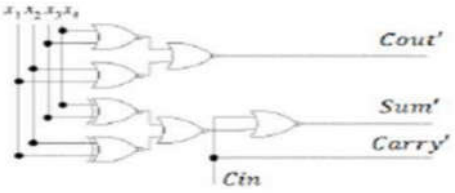

Fig.3. Gate level implementation of design 1

Table 2: Truth table of design 1 compressor

Cin	X4	X3	X2	X1	Cout	Carry	Sum
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
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1	0	1	1	0	1	1	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	0

However; the propagation delay through the gates of this design is lower than the one for the exact compressor. Therefore, the critical path delay in the proposed design is lower than in the exact design and moreover, the total number of gates in the proposed design is significantly less than exact compressor.As shown in Table 1, the carry output in an exact compressor has the same value of the input cin in 24 out of 32 states. Therefore, an approximate design must consider this feature. Table 2 shows the truth

table of the first proposed approximate compressor. The proposed design 1 has 12 incorrect outputs out of 32 outputs thus yielding an error rate of 37.5%. This is less than the error rate using the best [2] approximate full-adder cell.

3.2 Design 2

A second design of an approximate compressor is proposed to further increase performance as well as reducing the error rate can be ignored in the hardware design.

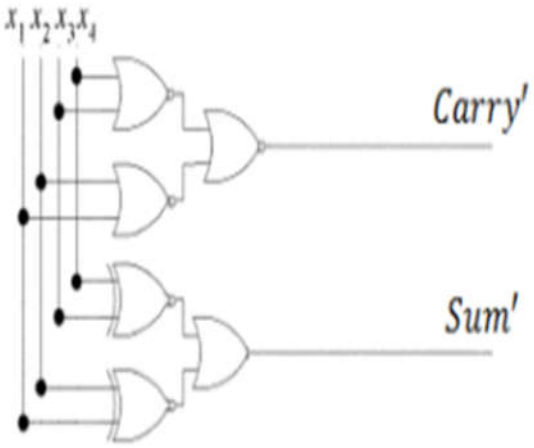


Fig.4. Gate level implementation of design-2

In this new design, carry uses the right hand side of (3) and cout is always equal to cin; since c in is zero in the first stage, cout and c in will be zero in all stages. So, cin and c out can be ignored in the hardware design.

Table 3: Truth Table of Design-2

X4	X3	X2	X1	Carry'	Sum'
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Fig.4. Shows the gate level implementation of design 2 compressor and the expressions below describe its outputs. The delay of the critical path of this approximate design is 2Δ,so it is 1Δ less than the previous designs; moreover, a further reduction in the number of gates is accomplishedMultipliers are one of the most large blocks in computer mathematics and are generally utilized in distinct digital sign processors. There is developing needs for excessive pace multipliers in unique packages of computing systems, collectively with pc snap shots, medical calculation, image processing and so forth. Speed of multiplier determines how rapid the processors will run and architects are truely more focused on immoderate speed with low electricity intake. The multiplier shape consists of a partial product generation level, partial product discount

level and the final addition level. The partial product reduction diploma is accountable for a huge a part of the total multiplication postpone, energyand place. Therefore in order to build up partial products,compressors usually put in force this degree because of the fact theycontribute to the discount of the partial products and moreover contribute to lessen the vital path this is critical to keep the circuit's standard overall performance.First all the eight inputs are fed as enter to the AND gates which shape sixteen products as established within the fig and shape a tree like shape. Then the ones inputs are further fed to ½ adders, whole adders and compressors to reduce the partial merchandise.

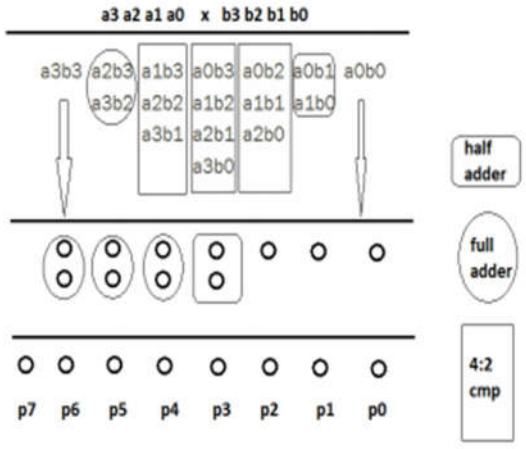


Fig.1.

This is accomplished with the aid of the use of 3-2, 4-2 compressor systems. A three-2 compressor circuit is likewise called complete adder cell. Since those compressors are used again and again in big systems, so improved design will make a contribution masses closer to standard tool performance. The inner structure of compressors is essentially composed of XOR-XNOR gates and multiplexers. The XOR-XNOR circuits are also constructing blocks in numerous circuits like mathematics circuits, multipliers, compressors, parity checkers, and many others. Optimized format of those XOR-XNOR gates can improve the overall performance of multiplier circuit. In gift work, a XOR-XNOR module has been proposed and 4-2 compressor has been applied the usage of this module. By the usage of partial product accumulation in proposed circuit reduces electricity consumption. Following circuit shows compressor circuit is fashioned by using manner of xor-xnor gates

COMPRESSOR CIRCUIT BUILDING BLOCKS

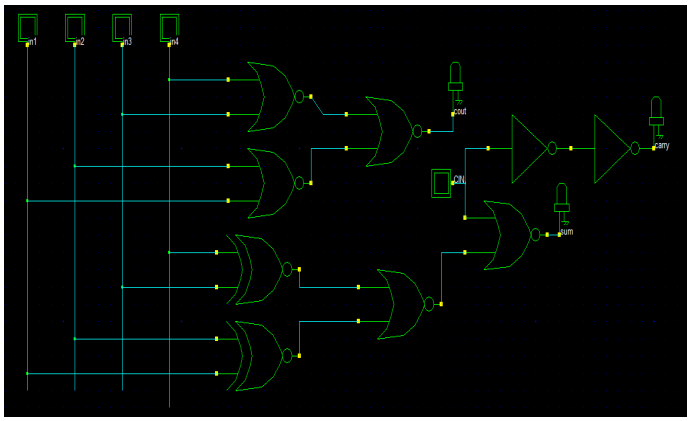
There are different architectures and designs of 4-2 compressor circuits reported in literature. These are mainly composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX). Complementary CMOS uses the dual networks to implement

a given function. One part consists of complementary pull-up PMOS network while other part consists of pull-down NMOS networks. This technique requires more numbers of transistors and large layout area. Static CMOS XOR and XNOR [3] gate is shown in figure 1(a). Another implementation of XOR-XNOR circuit with 12 transistors is shown in figure 1(b) [4]. Further in figure 1(c) two pull-up PMOS-transistors and two pull-down NMOS–transistors are added to restore full swing operation. The circuit performs successfully at low supply voltages but this comes at the expense of increased area and number of transistors. Another disadvantage of the circuit is that each of the inputs drives four gates instead of two gates doubling the input load. This will cause slow response when this circuit is cascaded added together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressor is also known as full adder. It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder

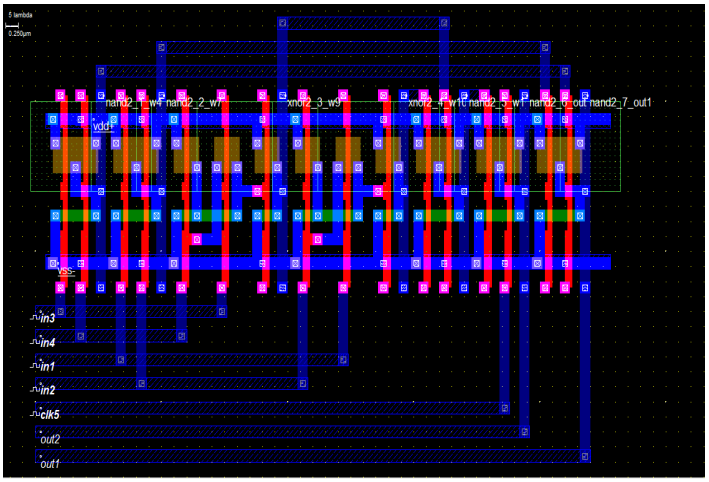
SIMULATION RESULTS:

RESULTS:

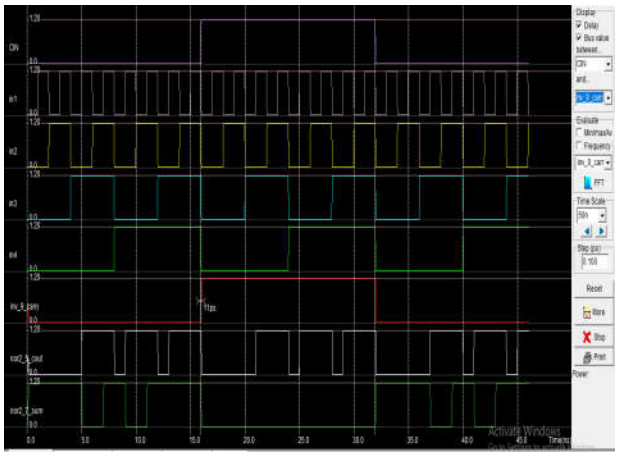
Design 1:



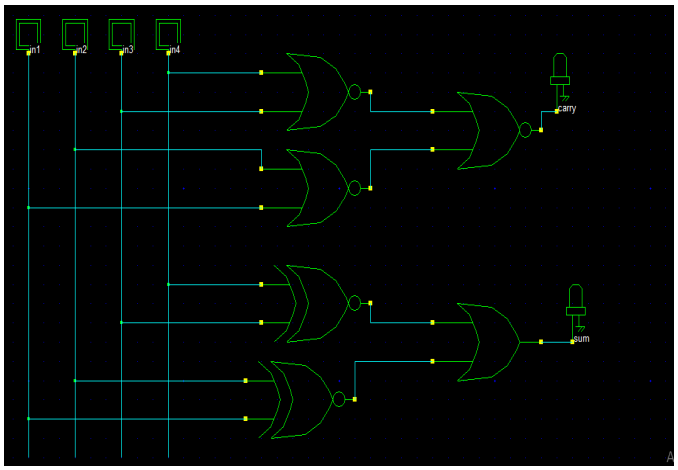
Design 1 layout

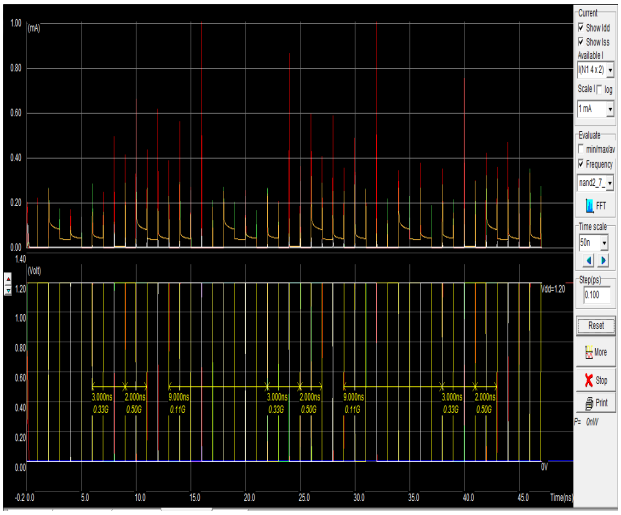


Design1 otput:

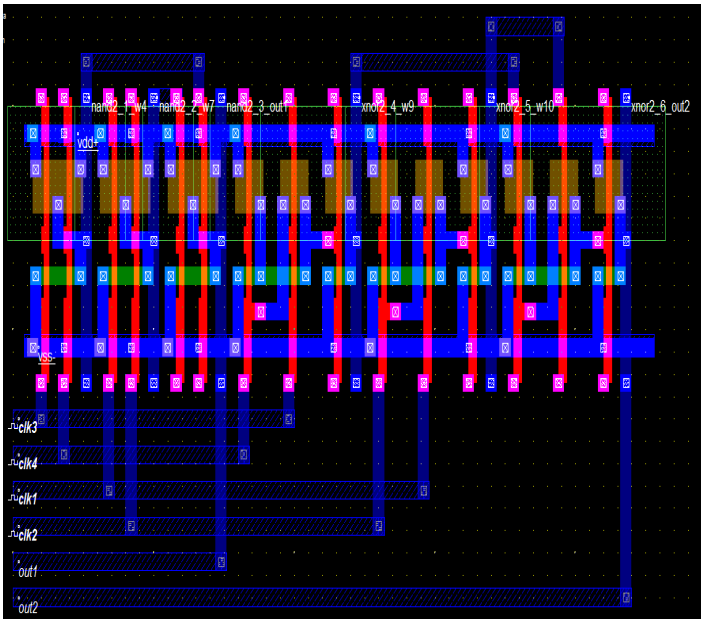


Design 2:

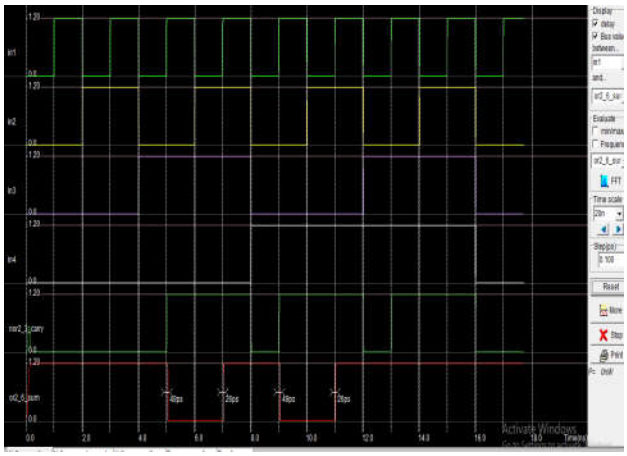


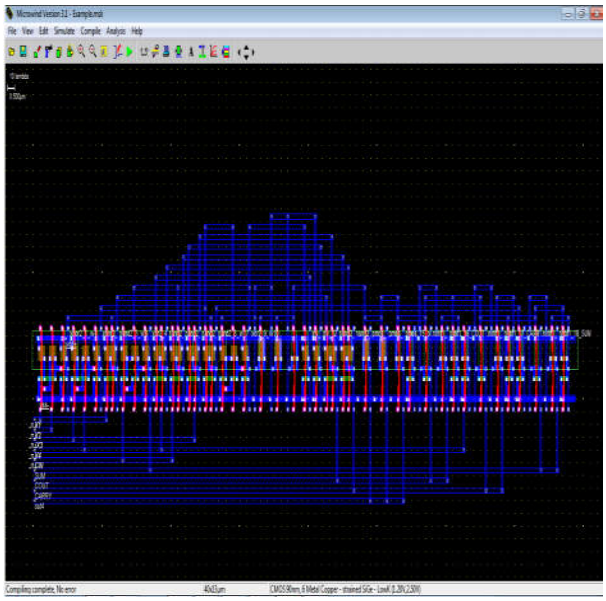


Design 2 layout:

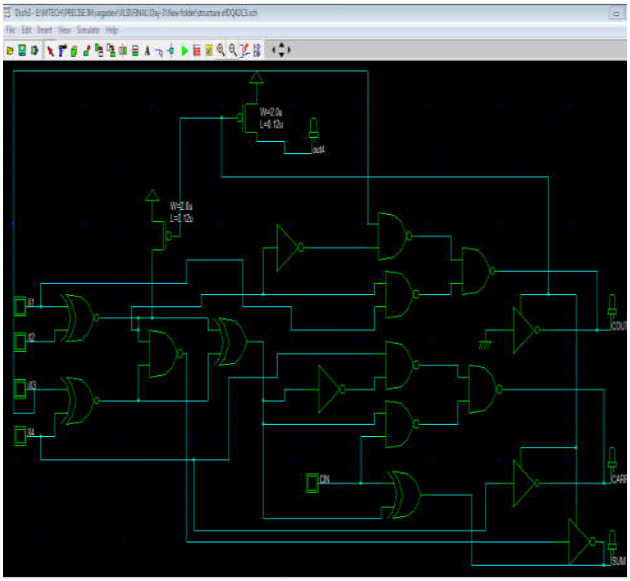


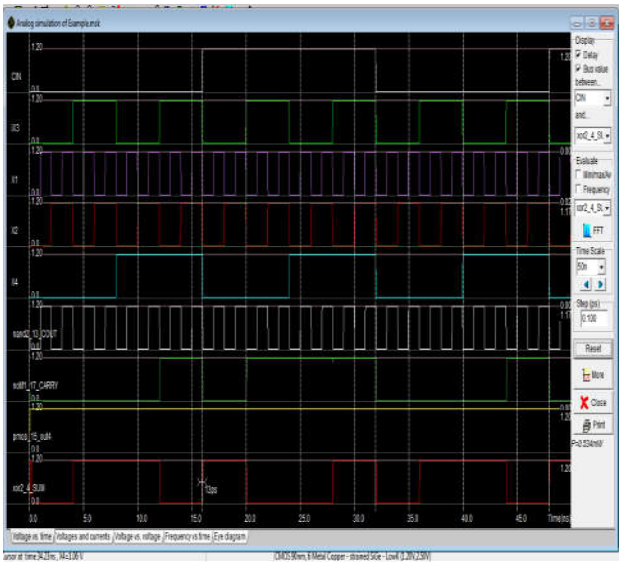
Design2 output:



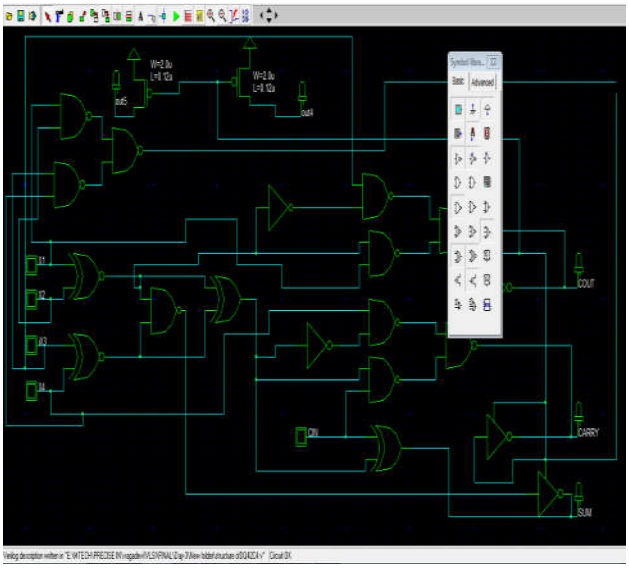


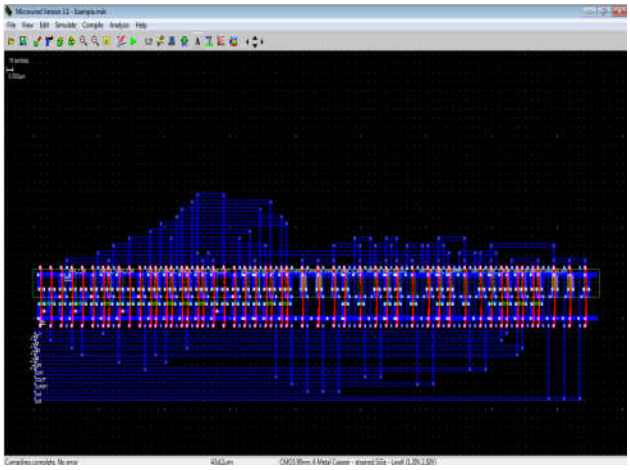
Design 3:

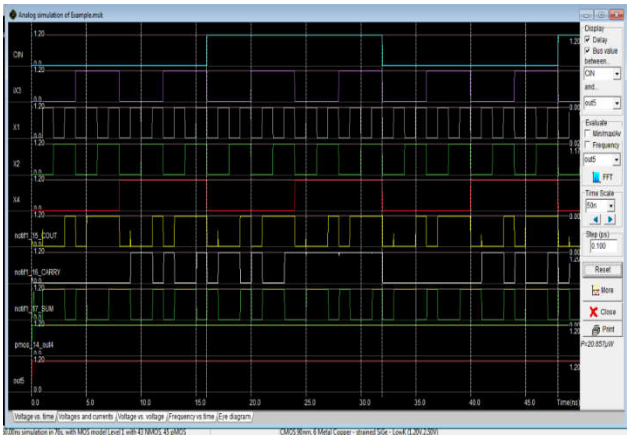




Design 4:







CONCLUSION

The compressors are utilized in the reduction module of four approximate multipliers. The approximate compressors show a significant reduction in transistor count, power consumption and delay compared with an exact design. In terms of transistor count, the first design has a 46% improvement, while the second design has a 49% improvement. In terms of power dissipation, the first design has a 57% improvement and the second design has a 60% improvement over CMOS implementation at feature sizes of 32 nm. In terms of delay, the second design has a 44% improvement compared to the exact compressor and 35% improvement compared to the first design on average at CMOS feature sizes of 32 nm. The proposed multipliers show a significant improvement in terms of power consumption and transistor count compared to an exact multiplier**.**

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