

POWER QUALITY IMPROVEMENT IN PARALLEL FEEDER DISTRIBUTION SYSTEM USING INTERLINE UNIFIED POWER-QUALITY CONDITIONER (I-UPQC)

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Abstract

This paper deal with power quality improvement in parallel feeder distribution system using interline unified power-quality conditioner (I-UPQC). The I-UPQC consists of two interline unified power-quality conditioner (IUPQC) that are connected to a common dc-link, one of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor. The advantage of the proposed design when power quality problems occurs in any one of the feeder (fault feeder), the other feeder (or healthy feeder) can supply the required active power using dc-link capacitor. In IUPQC the shunt active power filter (SHAPF) is used to mitigate current harmonics and the series active power filter (SEAPF) is used to maintain voltage at a certain level. The structure and control is discussed in this paper. Simulation of the distribution system model is verified with MATLAB/Simulink to validate the proposed system.

Keywords: Interline unified power-quality conditioner (I-UPQC), unified power-quality conditioner (UPQC), shunt active power filter (SHAPF), series active power filter (SEAPF) and Power Quality (PQ).

1. INTRODUCTION

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, power-quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In addition, lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation [1]. In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering [2]. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation [3]. In recent years, solutions based on flexible ac transmission systems (FACTS) have appeared. The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A unified power quality conditioner (UPQC) [4] is the extension of the unified power-flow controller (UPFC) [5]

concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply feeder [6]–[8].

Recently, multiconverter FACTS devices, such as an interline power-flow controller (IPFC) [9] and the generalized unified power-flow controller (GUPFC) [10] are introduced. The aim of these devices is to control the power flow of multilines or a subnetwork rather than control the power flow of a single line by, for instance, a UPFC. When the power flows of two lines starting in one substation need to be controlled, an interline power flow controller (I-PFC) can be used. An IPFC consists of two series VSCs whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization. The GUPFC combines three or more shunt and series converters. It extends the concept of voltage and power-flow control beyond what is achievable with the known two-converter UPFC. The simplest GUPFC consists of three converters—one connected in shunt and the other two in series with two transmission lines in a substation. The basic GUPFC can control total five power system quantities, such as a bus voltage and independent active and reactive power flows of two lines. The concept of GUPFC can be extended for more lines if necessary. The device may be installed in some central substations to manage power flows of multilines or a group of lines and provide voltage support as well. By using GUPFC devices, the transfer capability of transmission lines can be increased significantly. Furthermore, by using the multiline-management capability of the GUPFC, active power flow on lines cannot only be increased, but also be decreased with respect to operating and market transaction requirements. In general, the GUPFC can be used to increase the transfer capability and relieve congestions in a flexible way.

This concept can be extended in this paper to design multiconverter configurations for PQ improvement in adjacent feeders i.e the interline unified power-quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in [11]–[13]. The I-UPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-VSC. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

PROPOSED INTERLINE UPQC (I-UPQC) SYSTEM

2.1 I-UPQC Structure

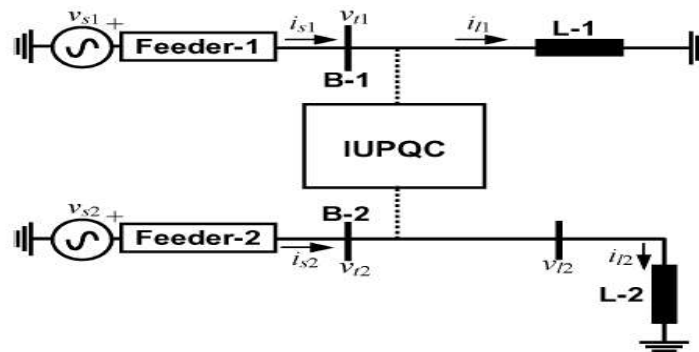


Fig 3.1 Single-line diagram of an I-UPQC-connected distribution system

The I-UPQC shown in Fig.1 consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor. Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2. The schematic structure of a VSC is shown in Fig.1 In this structure, each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig. All the inverters are supplied from a common single dc capacitor and each inverter has a transformer connected at its output.

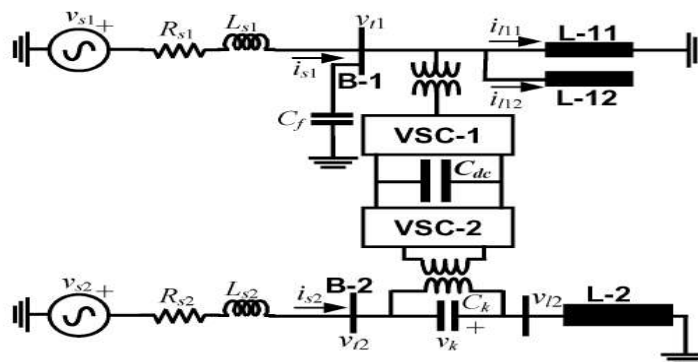


Fig 2 Typical connection of I-UPQC in distribution system

The complete structure of a three-phase IUPQC with two such VSCs is shown in Fig. 2. The secondary (distribution) sides of the shunt-connected transformers (VSC-1) are connected in star with the neutral point being connected to the load neutral. The secondary winding of the series-connected transformers (VSC-2) are directly connected in series with the bus B-2 and load L-2. The ac filter capacitors and are also connected in each phase (Fig. 3) to prevent the flow of the harmonic currents generated due to switching. As shown in Fig.2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in

series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The aims of the I-UPQC shown in Fig. 1are:

- 1) To regulate the load voltage against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2.
- 2) To compensate for the reactive and harmonic components of nonlinear load current.

In order to achieve these goals, series VSCs (i.e., VSC 2) operate as voltage controllers while the shunt VSC (i.e.VSC2) operates as a current controller.

In order to attain these aims, the shunt VSC-1 is operated as a voltage controller while the series VSC-2 regulates the voltage across the sensitive load. The system parameters used in the study are given in Table I. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no I-UPQC is connected to the distribution system, are shown in Fig.2.

CONTROL STRATEGY

As shown in Fig.2, the I-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the method [12], will be discussed later.

3.1 Switching Control of Shunt Active Power Filter

After optimal selection of PI regulator components to design the switching control of shunt active power filter to compensate current harmonics and the reactive component of load L₁ current. The proposed SRF-based shunt APF generates reference source-current signals by using source voltages and source currents and voltages at dc-capacitor. The block diagram for the controlled SRF-based shunt APF is shown in fig.3. The measured source-current are transformed to d-q-0 coordinates by using the transformation matrix (equ.1).

$$i_{s,dq0} = T_{abc}^{dq0} i_{s,abc} \tag{1}$$

$$i_{s,d} = \overline{i_{s,d}} + \tilde{i_{s,d}} \tag{2}$$

$$i_{s,q} = \overline{i_{s,q}} + \tilde{i_{s,q}} \tag{3}$$

($\tilde{i_{s,d}}$ and $\tilde{i_{s,q}}$) are oscillating components.

($\overline{i_{s,d}}$ and $\overline{i_{s,q}}$) are average components.

(i_{sd}) is the positive-sequence average component in the d-axis (i_{s0} and i_{sq}) are the zero-sequence and negative-sequence component in the 0 axes and q-axes of the source currents, the load unbalances and when $i_{sq}=0$, harmonic are compensated.

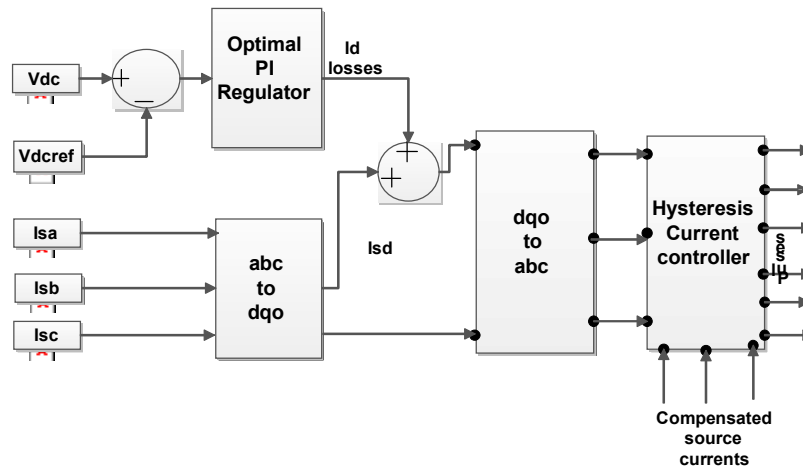


Fig.3. SRF Based Controlled Shunt Active Power Filter

The new reference current is result of output of the optimal PI regulator and d-component (i_{sd}) of the shunt-VSC reference current.

$$i_{sd}^{ref} = \bar{i}_{sd} + i_{d_{losses}} (= \Delta i_d) \tag{4}$$

The reference current in (26) is then transformed back into the abc reference frame. By using hysteresis current control, the output-compensating currents in each phase are obtained.

$$\begin{bmatrix} i_{sa}^{ref} \\ i_{sb}^{ref} \\ i_{sc}^{ref} \end{bmatrix} = T_{dco}^{abc} \begin{bmatrix} i_{sd}^{ref} \\ 0 \\ 0 \end{bmatrix} \tag{5}$$

3.2. Switching Control of Series Active Power Filter

The proposed Series APF control strategy is aimed to controlled voltage source and generates mainly to obtain constant load terminal voltage at the desired point at require level. The difference of the supply voltage and the ideal load voltage is compensate by injecting voltage by the series APF. These injected voltages cancel out the distortions in supply voltages. Detect source voltage ($v_{s_{abc}}$) to transformed dco components ($v_{s_{dco}}$) by using the transformation matrix (equ.6).

$$v_{s_{dco}} = T_{abc}^{dco} v_{s_{abc}} \tag{6}$$

The desired load voltage in the synchronous dco reference frame ($v_{l_{dco}}^{des}$) assume to be constant.

$$v_{l_{dco}}^{des} = T_{abc}^{dco} v_{l_{abc}}^{des} \tag{7}$$

Now generate the compensating reference voltage ($v_{cf_{dco}}^{ref}$) and given by

$$v_{cf_{dco}}^{ref} = v_{sdco} - v_{sdco}^{des} \tag{8}$$

By using sinusoidal PWM voltage control technique dqo compensating reference voltage is then transformed back into the abc reference frame.

SIMULATION STUDIES

The system parameters for the simulation studies for the proposed analysis i.e. I-UPQC with SWPM switching is realized using SWPM controller strategy is done in MATLAB/SIMULINK and shown in Table 4.1.

System Parameters	
System Parameters	Values
System frequency (f)	50HZ
Rated voltage	380V(rms, Phase-Phase)
Source Impedance	0.6Ω and $0.1mH$
Nonlinear Load	An Universal bridge consisting of resistor (10Ω) and R-L Load(10Ω and $3mH$)
Linear Load-1	A three-phase resistive Load (10Ω)
Linear Load-2	A three-phase R-L Load (10Ω and $10mH$)
VSC-2 Series T/F	4kva,200/180,50Hz,10% leakage reactance
Power losses in VSC-1,VSC-2,	$R_{f1}=0.1\Omega, R_{f2}=0.1$
Filter capacitors	$C_{f1}=10\mu F$ and $C_{f2}=10\mu F$
DC Capacitor(C_{DC})	$2,000\mu F$
Kp	13.2466
Ki	0.4778

Case 1 - Voltage Sag Occurs on Feeder 2

In this case a sag 30 % with phase-angle jump of -10° is created at feeder 2 at time $t = 0.02s$ and it is cleared at time $t = 0.04s$.The source voltages and load voltages without I-UPQC are shown in Fig. 3 (a) and (b).

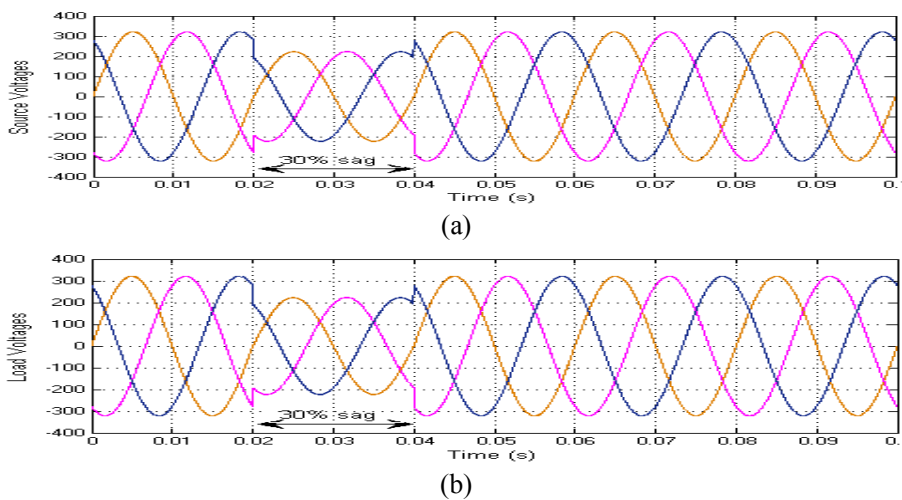


Fig.3 (a) Three phase source voltages at feeder 2, (b) Three phase load voltages at feeder 2.

When the compensating device i.e., I-UPQC is considered the analysis for same duration of sag is studied. The reference injected voltages required for SEAPF are calculated by using equation (8). The waveforms for injected voltages are shown in Fig.4

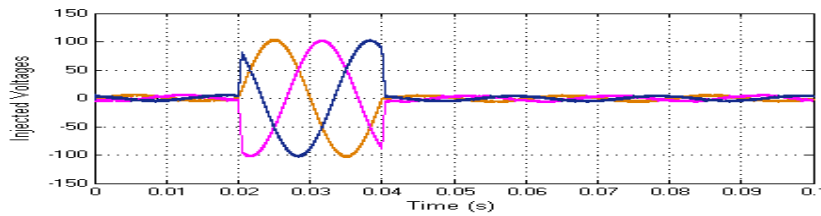


Fig.4 Injected Voltages on SEAPF₁

At this angle of injection the actual injected voltages tracks the desired reference injected voltages accurately. The DC-link voltage is shown in Fig.5. At the period of sag DC link voltage drops, this initial drop is due to the sudden power change in the feeder-2, to nullify this effect the extra power is supplied from the dc-link energy storage as real power controller of feeder-2. Now load voltages are resorted to normal value which are shown in Fig.6 and real power (P) exchange at feeder 2 is shown Fig.6.

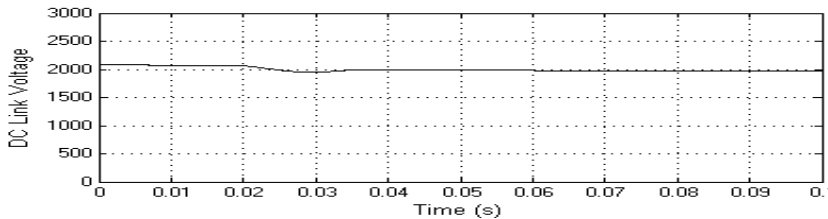


Fig.5. DC link Voltage (V_{DC})

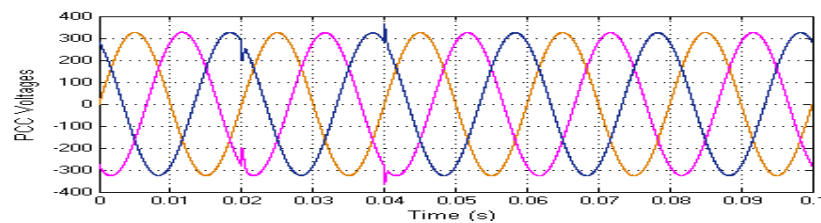


Fig.5 Balanced three phase PCC/load voltages in feeder2

Case 2 – Current Harmonic Compensation on Feeder-1

In feeder 1 contains nonlinear load I-UPQC compensate current harmonics in feeder 1 through SHAPF. The PCC voltages (v_{ta}, v_{tb}, v_{tc}) and load currents (i_{la}, i_{lb}, i_{lc}) are shown in Fig.6 (a) and (b) respectively. **THDs** for load currents in each phases are 14.68%, 16.71% and 17.79% as shown in Table.4.2. First set the $V_{dc\ ref}$ value of 800 V (i.e., $1.5V_{lm}$) and C_{dc} of 3300 μF in I-UPQC topology for the load compensation and using PI regulator to maintain the DC link (v_{dc}) is around 800 V as shown in Fig. 6(c). The injected filter currents (i_{fa}, i_{fb}, i_{fc}) and compensated source currents (i_{sa}, i_{sb}, i_{sc}) are shown in Fig. 6 (d) and (e). The voltage across inductor ($v_{ind\ a}$) as shown in Fig. 6(f). After compensation source currents THDs are 3.19%, 2.665% and 2.42% as shown in the Table 4.2.

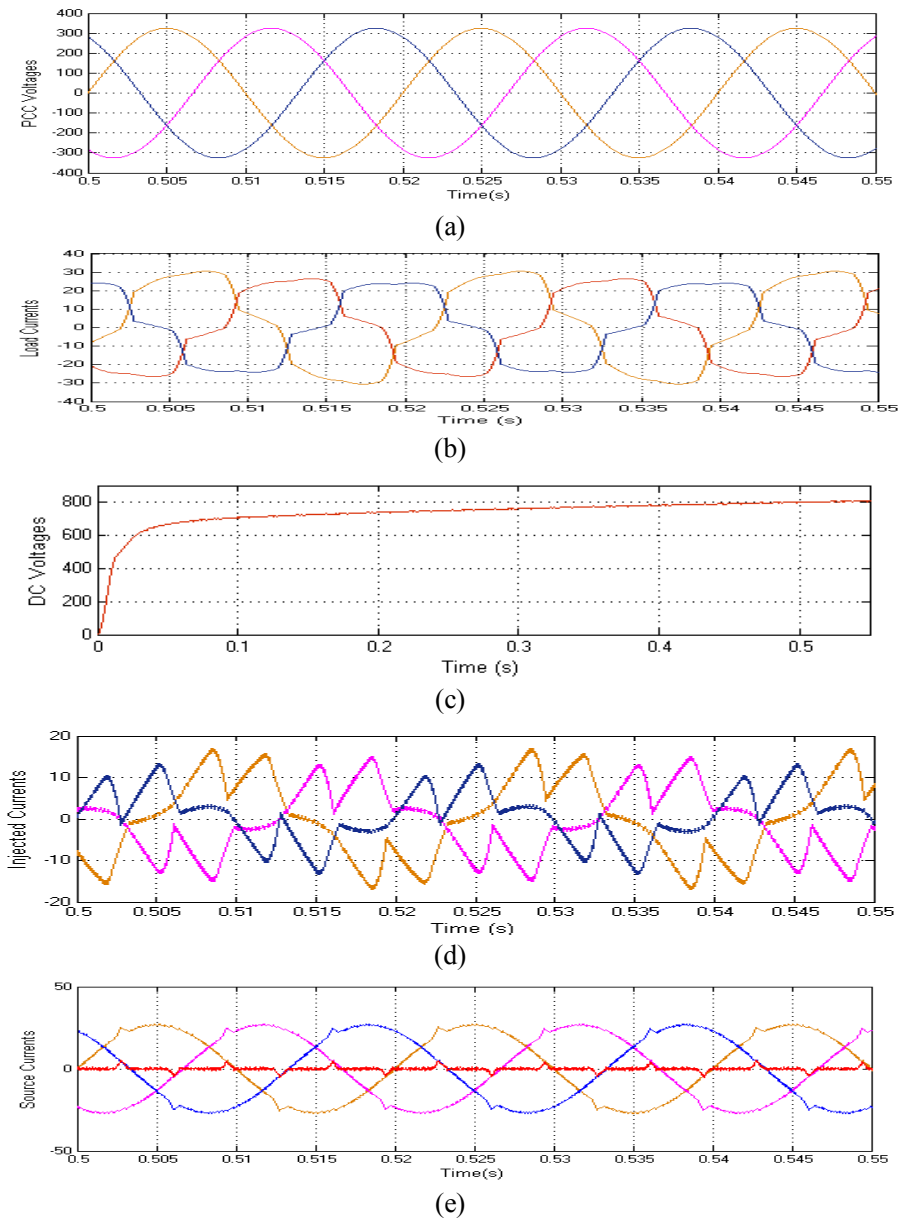


Fig.6 Simulation results using I-UPQC topology (a) PCC voltages, (b) Load currents, (c) voltage across the DC link voltage, (d) filter currents, (e) source currents.

Table 4.2 % THDs of source currents

Source Currents	THD (%)	
	Without Compensation	With Compensation
I_{sa}	13.68	2.198
I_{sb}	17.71	2.665
I_{sc}	14.79	2.42

5. Conclusion

The interline UPQC (I-UPQC) discussed in this paper is capable of handling system in which the loads are unbalanced and distorted. The proposed device can mitigate various power quality problems like sag, harmonics, noise, etc. It has been observed that an I-UPQC is able to protect the distribution system from various disturbances occurring either in Feeder-1 or in Feeder-2. As far as the common dc-link voltage V_{dc} is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage constant. Therefore, even for voltage sag or a fault in Feeder-2, VSC-1 passes real power through the dc capacitor onto VSC-2 to regulate the load voltage. The simulated results shows that PI controller of the shunt filter (current control mode), series filter (voltage control mode) compensates of all types of interruptions in the load current and source voltage, and bring the Total Harmonic Distortion (THD) after compensation is to be less than 5%.

6. References

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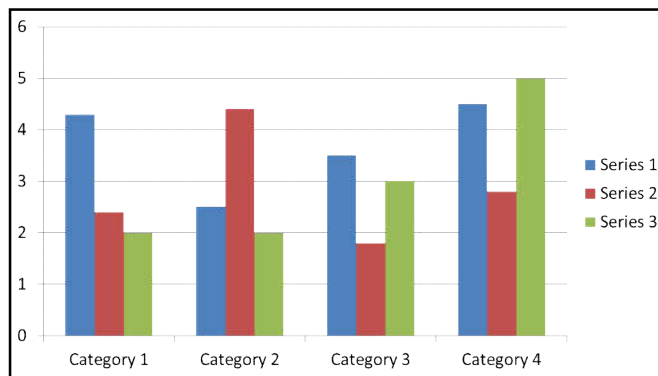


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$$\varphi_{\mu\nu}(z) = \frac{\|k_{\mu\nu}\|^2}{\sigma^2} e^{-\frac{\|k_{\mu\nu}\|^2 \|z\|^2}{\sigma^2}} [e^{ik_{\mu\nu}z} - e^{-\frac{\sigma^2}{2}}] \tag{1}$$

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Appendix

An appendix, if needed, should appear before the acknowledgments.

Acknowledgments

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- [2] H. S. Nalwa, Editor, “Magnetic Nanostructures”, American Scientific Publishers, Los Angeles, (2003).

11.3. Chapter in a Book

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11.4. Conference Proceedings

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11.5. Patent

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