A HIGH SPEED VOLTAGE LEVEL SHIFTER DESIGN FOR DUAL-SUPPLY APPLICATIONS

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ABSTRACT : This paper introduces a level shifter in digital electronics, also called a logic-level shifter, is a circuit used to translate signals from one logic levelor voltage domain to another, allowing compatibility between ICs with different voltage requirements, such as TTL and CMOS. Level shifter used in multiple voltage digital circuits and this is capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit.The proposed system of the voltage level shifter for dual supply application has been developed in a 45nm CMOS technology with the input frequency of 1MHZ with low input voltage VDDL as 0.4V and high input voltage VDDH as 1.8V.The proposed architecture of this paper is analyzed using the tanner tool and compared with area, power and delay.

Index Terms: Voltage Level Shifter, low power devices, dual supply applications, pull-up and pull-down devices

I. INTRODUCTION

To achieve high performance and high integration density, the transistor dimensions are aggressively scaled down in ultra-deep submicron process while low power dissipation is achieved by scaling down the supply voltage. With the wide applications of battery supplying devices, such as portable PC, cellar phones and PDA, power consumption has become a critical design concern in today's VLSI circuit and system designs. In addition, approximately millions of transistors have been packed into a single chip in nanometer technologies. So the heat dissipation caused by huge power consumption becomes a problem that can adversely affect reliability and packaging cost of a design. These factors have attracted much attention on low power design of CMOS circuits and driven numerous research efforts to address various kinds of power reduction techniques. Multiple supply voltages techniques have been proposed for low power design. With the use of two different supply voltages, it is possible that a low voltage gate is made to drive a high-voltage one.

This leads to the high output of the low-voltage gate cannot fully turn off the PMOS part of the high-voltage gate, so it forms a DC leakage path from the power source to ground. The DC leakage can lead to substantial power loss. There are two types ofpower consumption: static power and dynamic powerconsumption. The static power dissipation is due to theleakage current of reverse biased p-n junction diode ofMOSFET. Dynamic power dissipation is mainly due tothe charging and discharging of the load capacitor. Theeffective way to lowering the dynamic power and shortcircuitspower consumption of a circuit is lowering thevalue of the power supply voltage. Lowering the supplyvoltage drastically increases the propagation delay of thecircuits. In digital circuits dual-supply voltages are usedin which low voltage(VDDL) is applied for the blocks onthe noncritical paths while a high supply voltage(VDDH) isapplied to the analog and high-speed digital blocks.The level shifter is a key circuit component in multi-voltage circuits and

has important implementation. For a chip-level DVS system, level Shifters are required between core circuits and I/O circuits interface where low voltage logic signals from chip core are shifted to high voltage level at which pad Ring is working.Level shifter is to be designed with low powerconsumption, minimum propagation delay, and siliconarea

II. EXISTING SYSTEM

In moderate-speed mixed signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., VDDL) is supplied for the blocks on the noncritical paths while a high supply voltage (i.e., VDDH) is applied to the analog and the high-speed digital blocks. The architecture of conventional level shifter is shown in Fig.1(a).

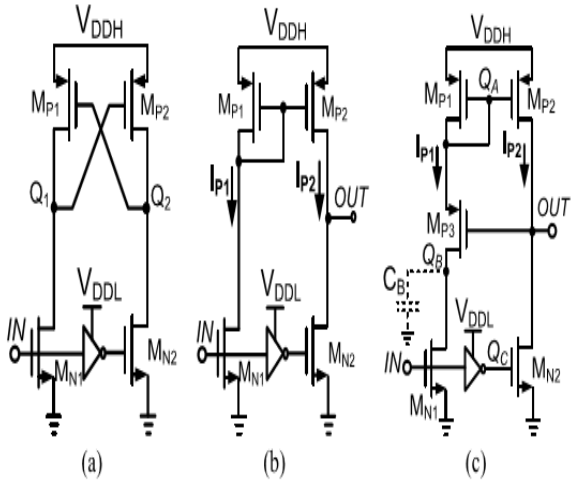

Fig. 1. Schematic of the (a) Conventional level Shifter, (b) level shifter with a semi-static current mirror, and (c) level shifter with a dynamic current mirror

The circuit consisting of two cross-coupled pMOSFETs (MP1 and MP2) and two nMOSFETs (MN1 andMN2) followed by complementary input signals IN and INB. The circuit has voltage contrast between high supply voltage VDDH becomes larger than low supply voltage VDDL. At the point when the voltages of IN and INB are Low and High, MN1 and MN2 are Off and On, respectively. MN2 then pulls Q2 node to down, causing MP1 to turn On. Because node Q1 then increases to VDDH, MP2 turns off, and Q1 drops to the GND level. Note that the voltage at node Q2 is determined by the drive currents of pull-down transistorMN2 and pull-up transistor MP2. Therefore, if the drive current of MP2 islarger than that of MN2, Q2 cannot be discharged.Consider the case, extremely low-voltage subthresholdLevel shifter, because the on-current of MN2becomes low, the drive currents of the nMOSFETs are significantly smaller than those of the pMOSFETs, which operate in the strong inversion region. Thus, Q2 node cannot be discharged. As a result, a conventional level shifter circuit cannot correctly operate in this situation. Let us consider, employing week pull-up devices using high-Vth transistors and/or strong pull down networks by using low-Vth transistors. Another way is to use strong pull-down devices increase in both the delay and the power consumption and enlarging their width.The last arrangement is to decrease the strength of the pull-up device when the pull-down device is pulling down the output node. The structure outlined in Fig. 1(b) utilizes a semi-static current mirror to confine the current and strength of the pull-up device (i.e., MP2) when the pull-down is pulling down the out node. The semi-static current mirror experiences the static current coursing through MN1 and MP1 amid the "High" logic levels of the input signal. With a specific end goal to diminish the static power utilization, a dynamic current generator, which turns on just amid the change times, can be utilized. The structure shown in Fig. 1(c) employs a dynamic current generator implemented by MP3. In this circuit, when the input signal IN goes from “Low” to “High,” MN1 turns On and MN2 turns Off and pulls the node QB down. OUT node had been “Low” (before the transition), during the time interval in which OUT node is not corresponding to the logic level of the

input signal IN, MP3 will be turned on. Subsequently, a transition current flows through MN1, MP3, and MP1. This current is reflected to MP2 (i.e., IP2) leading to the node OUT up. At last, when OUT is pulled up to VDDH, MP3 is turned off and subsequently no static current moves through MN1, MP3, and MP1.This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

Nevertheless, IC design becomes rather difficult when it comes to low-voltage and low power operation. On the other side, to achieve comparable gain of simple stages in comparison to cascade structures, it is possible to connect multiple simple stages in series (into cascade). However, multi-gain stage topologies may represent a stability problem due to the location of their dominant poles. Subsequently, clever compensation techniques have to be used to ensure stability of circuits.

DISADVANTAGES

- More power consumption
- More silicon area
- More propagation delay
- Not fixed the sub threshold level properly

III. PROPOSED SYSTEM

The proposed system explains the concept of high speed and power efficient voltage level shifter that are used in dual supply application. The voltage level shifter has capable of converting, extremely low level input voltage to high level output voltage. The schematic of proposed technology of this paper includes the auxiliary circuit. The disadvantage of existing system is, it will not properly convert the output voltage level, when the input voltage is in sub-threshold condition. But the proposed system of voltage level shifter even works for sub-threshold input voltage by using the auxiliary circuit.

In order to reduce the existing contention at the high-to-low transition of the structure shown in Fig. 1(c), the transition current of IP1 and therefore IP2 must be suppressed when MN2 is pulling down the output node. For this purpose, the structure shown in Fig. 2. is proposed. The operation of the proposed circuit, shown in Fig. 2(a), is as follows. When the input signal changes from “Low” to “High,” MN1 is turned on and MN4 is turned off.

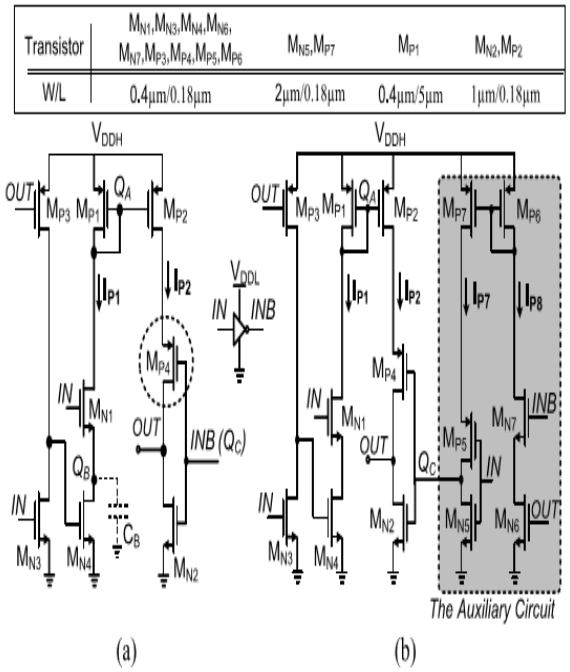

Fig. 2. (a) Principle of the proposed level shifter. (b) Schematic of the proposed level shifter.

During the transition time in which OUT is not corresponding to the logic level of the input, MN4 will be turned on, because the overdrive voltage of MP3 (i.e., VDDH) is larger than that of MN3 (i.e., VDDL). Therefore, a transition current flows through MN4, MN1, and MP1 (i.e., IP1). This current is mirrored into MP2 (i.e., IP2) and tries to pull up the output node. Finally, when OUT is pulled up, MP3 is turned off and consequently the gate of MN4 is pulled down by MN3 meaning that no static current flows through MN4, MN1, and MP1. It should be noted that in order to minimize the power consumption, the

aspect ratio of MP1 is chosen smaller than that of MP2.

As for the high-to-low transition of the input signal, MN2 is turned on trying to pull down the output node. At the same time, MN1 is turned off meaning that, in contrast to the structure shown in Fig. 1(c), roughly no transition current flows through MP1 (i.e., IP1 ≈ 0) reducing the strength of MP2 when MN2 is pulling down the output node. However, it should be noted that the node QA is pulled up just to VDDH − |Vth|, where Vth is the threshold voltage of MP1. This means that the current of MP2 (i.e., IP2) is not completely close to zero and consequently a weak contention still exists.In order to further reduce the value of IP2, another device, i.e., MP4 in Fig. 2(a) is used. For more details, when MN2 is pulling down the output node, the gate of MP4 is "High" with the value of VDDL and therefore the drain–source voltage of MP2 is decreased. As a result, as shown in Fig. 3, the propagation delay and therefore the power dissipation of the circuit will be decreased. It should be noted that if the gates of MN2 and MP4 are driven with a voltage higher than VDDL, not only the current of the pull-up device (i.e., IP2) is drastically reduced, but also the strength of the pull-down device (i.e., MN2) is increased. Thus, the contention and therefore the delay and the power (especially the power consumption of the next stage) are significantly reduced. Moreover, the level shifter will be able to operate correctly even for sub-threshold input voltages. In order to apply this technique to the proposed structure, as shown in Fig. 2(b), an auxiliary circuit (i.e., MP5, MP6, MP7, MN5, MN6, and MN7) is used.

This auxiliary circuit turns on only in the high-to-low transition of the input signal to pull up the node QC to a value larger than VDDL. The operation of this part of the circuit is as follows. When IN changes from "High" to "Low" and OUT is not still corresponding to the input logic level, MN6, MN7, and MP6 are turned on and MN5 is turned off. Therefore, a transition current flows through MN6, MN7, MP6, and mirrors to MP7 (i.e., IP7) pulling up the node QC.

This means that MP4 is turned off and MN2 is turned on with a voltage higher than VDDL, as shown in Fig. 3(b), leading to a significant reduction in the aforementioned contention. Finally, when OUT is pulled down, MN6 is turned off and consequently no current flows through MN6, MN7, and MP6 meaning that the auxiliary circuit is turned on only during the high-to-low transition of the input signal, as shown in Fig. 3(e) It should be noted that since it is not needed to charge QC up to the exact value of VDDH, the auxiliary circuit is designed such that the current flowing through MP7 (i.e., IP7) is very small.

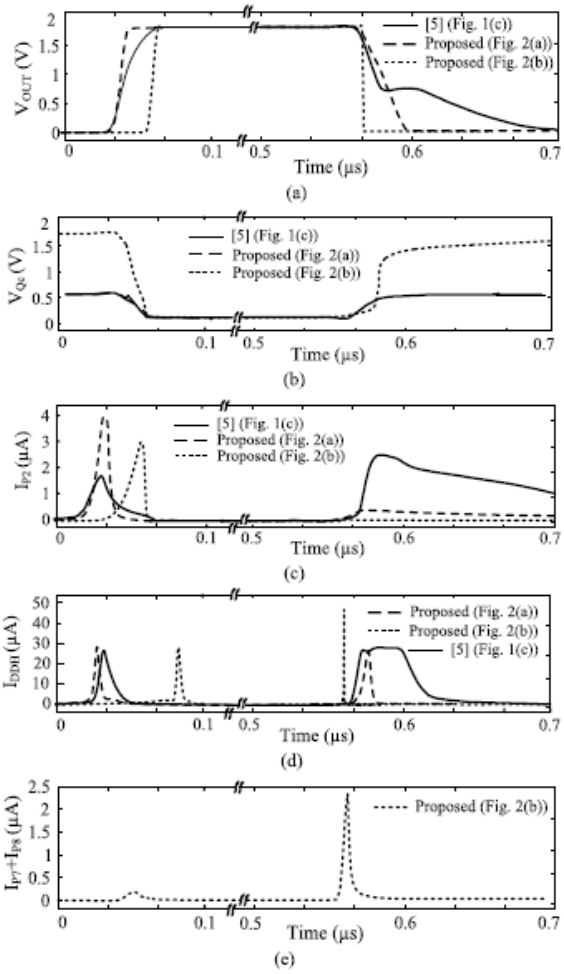

Fig. 3. Simulated waveforms of the level-shifter structures for low-to-high and high-to-low

transitions of the input signal. (a)Voltage of the output node (i.e., VOUT). (b) Voltage of the node QC. (c) Current of the output branch (i.e., I P2). (d) Entire current of the level shifter supplied by VDDH (i.e., IDDH). (e) Current of the auxiliary circuit (i.e., IP7 + IP8) of the proposed structure. The values of VDDH and VDDL are 1.8 V and 0.4 V, respectively.

This means that the existing contention in this branch will be negligible, reducing the propagation delay and the power consumption of the auxiliary circuit. As a result, using the auxiliary circuit, as shown in Fig. 3(c), the power consumption of the main circuit including the output load circuit (an inverter is added as a load circuit to all the structures) is considerably decreased such that the entire power consumption of the proposed structure is only about 30% of that of the structure without the auxiliary circuit (see Fig. 2(a)). It can be concluded that the efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Finally, in order to reduce the short-circuit power of the required inverter (i.e., MP3 and MN3), instead of the output signal, the input is used to drive the gate of MN3. In other words, in the conventional inverter, both low-to-high and high-to-low short-circuit currents exist whereas in the proposed structure, only a small current at the low to-high transition exists. Moreover, this current is reduced due to the fact that the gate of MN3 is driven by VDDL not VDDH.

IV. SIMULATION RESULTS

The proposed system, A High-Speed and Power-Efficient Voltage Level Shifterfor Dual-Supply Applications, implemented in a 45-nm CMOS process is designed and simulated in Tanner EDA Tool. The schematic diagrams of proposed system are first presented, followed by the Test Bench structure of the proposed system. The waveforms of proposed system are observed in W Edit and the results of Power consumption and simulation time are given in T-Spice.

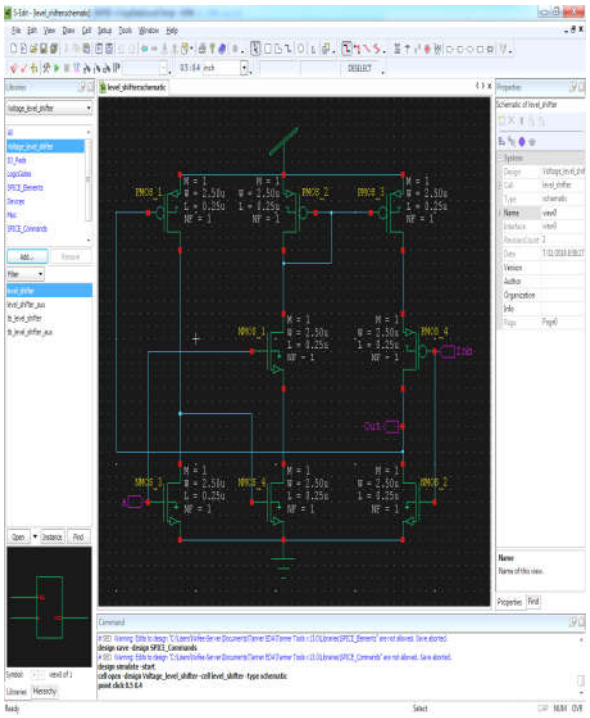

Fig. 4. Principle of proposed Level Shifter

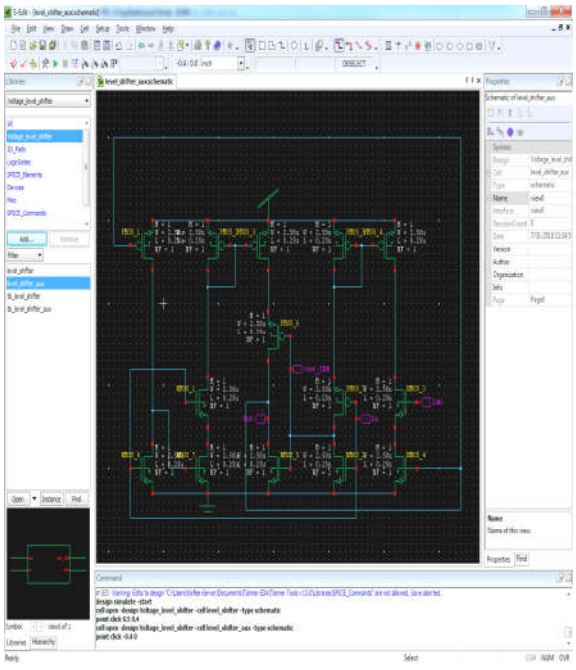

Fig. 5. Schematic of proposed Level Shifter

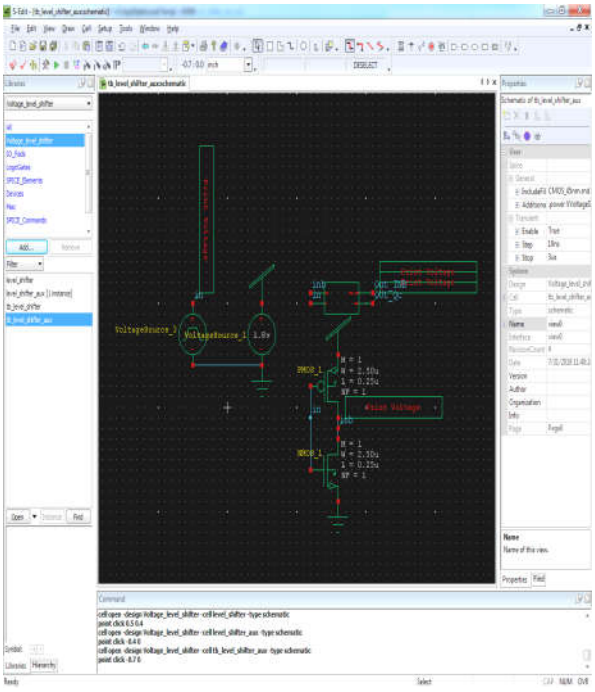

Fig. 6. Testbench of proposed Level Shifter

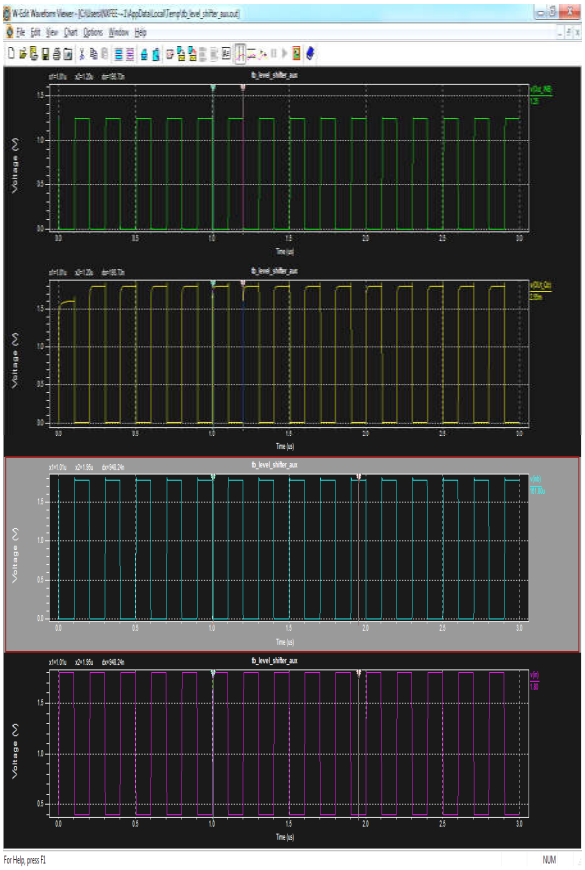

Fig. 7. Output Waveforms of Proposed System

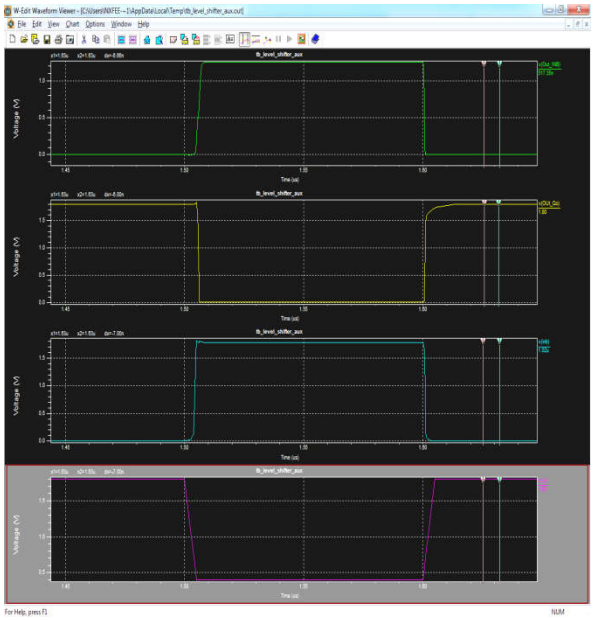

Fig. 8. Representation of Level Shifting in single clock cycle

COMPARISON BETWEEN EXISTING AND PROPOSED SYSTEMS

	Average Power (watts)	Simulation Time	Technology
Existing system	9.8 x10^-5	3.45	180nm CMOS
Proposed system	4.59x10^ -5	1.59 sec	45nm CMOS

Table 1: Comparison

V. CONCLUSION

In this paper, dual-voltage supply scheme is presented and level-conversion is developed. In which the fast and low-power voltage level-shifting architecture is designed nwhich is able to convert extremely low-input voltages.It is found in theory, that the lower supply voltage should be set at 0.4v and higher supply voltage at 1.8v to minimize chip power dissipation. In this system, the efficiency of the proposed circuit is due to the fact that not only the current of the pull-up device

is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased. Postlayout simulation results verified the efficiency of the proposed circuit compared with other works, especially from the power consumption view point.

This knowledge aids designers in deciding on the optimal supply voltages, which is essential for short design time. Further we studied both level shifting actions based on feedback in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. The circuits were optimized and simulated at 45nm CMOS technology using Tanner EDA tool, and the shifting in voltage levels is observed based on SPICE simulations. The popwer results obtained in the Tanner EDA T-SPICE is evident of significant savings on power consumption of up to 58% and the delay savings up to 77%. This level converter could be used and can produce lower power consumption in spite of the overhead, based on the data obtained from the simulations as discussed in this work.

VI. REFERENCES

[1] A. Wang and A. P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[2] K. Usami et al., "Automated low-power technique exploiting multiple supply voltages applied to a media processor," IEEE J. Solid-State Circuits, vol. 33, no. 3, pp. 463–472, Mar. 1998.

[3] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-µm CMOS for medical implant devices," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[4] P. Corsonello, S. Perri, and F. Frustaci, "Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology," in Proc. IEEE Int. Conf. Comput. Design (ICCD), Oct. 2015, pp. 499–504.

[5] S. Lütkemeier and U. Ruckert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[6] S.-C. Luo, C.-J.Huang, and Y.-H. Chu, "A wide-range level shifter using a modified Wilson current mirror hybrid buffer," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 6, pp. 1656–1665, May 2014.

[7] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 2, pp. 388–391, Feb. 2015.

[8] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1776–1783, Jul. 2012.

[9] S. R. Hosseini, M. Saberi, and R. Lotfi, "A low-power subthreshold to above-threshold voltage level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 10, pp. 753–757, Oct. 2014.

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