COMPARATIVE STUDY OF FINFET WITH MOSFET AND CMOSFET

Dr. R. Prakash Rao
Associate Professor, ECE Department, Matrusri Engineering College,
Saidabad, Hyderabad. India.
prakashiits@gmail.com

Abstract—In Process technology, FinFETs are achieved many ways to control leakage current, dynamic current, short channel effects (SCE) and delay over MOSFET and CMOS. FETs are promising substitutes to tackle short channel effects (SCEs) better than the conventional planar MOSFET's at deeply scaled technology nodes and thus enable continued transistor scaling. In this paper, reviewed the comparative study of FinFET with different parameter related to Channel Length, Leakage current, power and delay over MOSFET and CMOS.

Index Terms— MOSFET, CMOS, FINFET.

I. INTRODUCTION

Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path towards both denser and faster integration. As the size of the transistors is deceased, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, which gives rise in device performance. The CMOS scaling of the devices is facing challenges due to shrinking geometries, lower supply voltage, and higher frequencies, this have negative impact on the device by increasing short channel effect due to which leakage (gate leakage and sub-threshold leakage) in the device is increasing constantly [9]. The enhancement in the scaling technology has increased the need of low power based circuits. In nanometer regime, CMOS based circuit are not be used due to problem in its fundamental material, short channel effect and high leakage. The better technologies are needed for handling the various effects of MOSFET technology [1].As the planar MOSFETs shows a significant SCE (Short Channel Effect) and the designers are concentrate to FinFETs, which have negligible SCE for the same channel length [17]. FinFETs have attracted increasing attention over the past decade because of the degrading short-channel behavior of planar MOSFETs. While the planar MOSFET channel is horizontal, the FinFET channel (also known as the fin) is vertical. With multiple fons and smaller fin heights leads to more flexible and width of the channel can be increased, which in turn leads to more silicon area. On the other hand, taller fins lead to less silicon footprint, but may also result in structural instability. Although FinFETs implemented on SOI wafers are very popular. FinFETs have also been implemented on conventional bulk wafers extensively. In [24] authors are carried out their work on reduction of short channel

effects in FinFET. The results reveal that leakage current due to DIBL is well suppressed and roll-off of a FinFET is well controlled. Authors in [9] designed a 6T SRAM cell using the FinFET and compared SRAM with conventional structure by varying Sub-threshold leakage current and gate leakage current of internal transistors with self-controllable voltage level technique. The simulation was carried using Cadence Virtuoso Tool at 45nm Technology and the simulation results shows that total leakage reduces up to 34% under the self-controllable voltage level technique.

II. PROCESS TECHNOLOGY

A. MOSFET Devices

Metal Oxide Semiconductor FET is very different from that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge

carriers, through the semi conductive drain-source channel. In fig 1, shows that the gate electrode is placed on the top of a very thin insulating layer and there are a pair of small regions of n-types just under the drain and source electrodes.

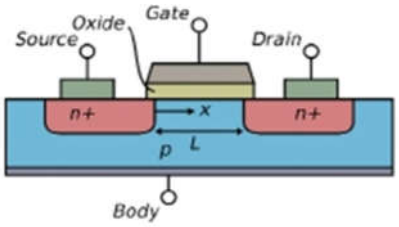

Fig 1: 2D view of MOSFET

In [26] authors have concluded that reducing the gate dielectric thickness raises the MOSFET drain current or allows the supply voltage to be reduced while maintaining an acceptable drain current and facilitates the reduction of gate length by the suppression of short-channel effects. Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide (SiO2) gate dielectric thickness. Major causes for concern in further reduction of the SiO2 thickness include increased poly-silicon (poly-Si) gate depletion, gate dopant penetration into the channel region, and high direct-tunneling gate-leakage current, which leads to questions regarding dielectric integrity, reliability, and stand-by power consumption. As well recognized in increased gate leakage current in MOSFET is a challenge to continue in the scaling. In [18] authors reveal that scale down the MOSFETs to the nanometer regime leads to short channel effects, which degrades the system performance and reliability.

B. CMOS

CMOS circuits are constructed in such a way that all PMOS transistors have an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors have an input from ground or from another NMOS transistor. Fig 2 shows the composition of a PMOS transistor, when low voltage is applied which creates a low resistance between its source and drain and creates high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor, when a low gate voltage is applied creates high resistance between source and drain and low resistance at a high gate voltage.

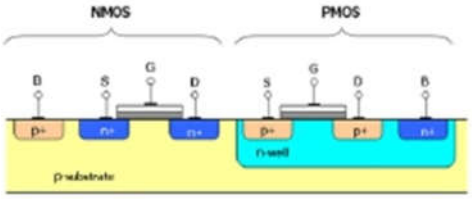

Fig 2: 2D view of CMOS

CMOS achieve current reduction by emphasize their qualities of every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates, which will turn on the nMOSFET and pMOSFET will be in off state, while a low voltage on the gates will causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time of the gate voltage goes from one state to another state, both MOSFETs conduct briefly. This give rise to an abrupt spike in power consumption and arise a serious issue at high frequencies.

C. FINFET devices

Researchers are striving hard to develop transistor with low cost and high performance, one such development is a FinFET. It uses a fin like structure instead of the conventional flat design, possibly enabling engineers to create faster and more compact circuits and computer chips. The term “FINFET” describes a non-planar, double gate transistor built on an SOI substrate, based on the single gate transistor design. The important characteristics of FINFET is that the conducting channel is wrapped by a thin Si “fin”, as shown in fig 3 which forms the body of the device. The fin thickness, which determines the effective channel length of the device [7].

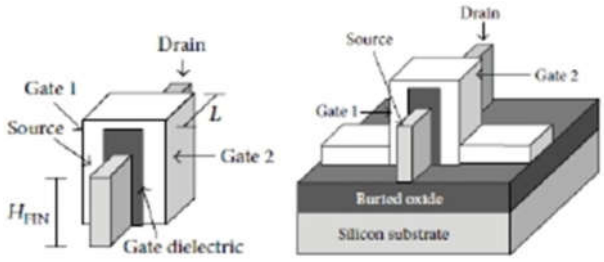

Fig 3:3D view of FinFET and SOI FinFET

The FinFET model structure consists of following regions

- With very low doping silicon fin region.
- Poly-silicon region, source and drain contact region, highly doped.
- Gate region- oxide (SiO2)

The advantages of FinFET are as follows

- Excellent control of short channel effects in submicron regime and making transistors still scalable. Due to this reason, the small- length transistor can have a larger intrinsic gain and much Lower off-state current compared to bulk counterpart.
- Promising matching behavior.
- Low cost
- Higher technological maturity than planar DG.
- Suppressed Short Channel Effect(SCE)

FinFET is one of the promising and better technologies for its applications and the circuit design for better performance and reliability. In [11] authors are evaluated the performance of FinFET based 6T SRAM cell in 22nm technology. The simulation result shows that FINFET based SRAM design is feasible design in contrast with CMOS based SRAM design.

Effective Channel Length (Leffg): Most of the scaling behavior of FINFET is not equal to poly length Lg which is very significant, but the effective channel length Leffg = Lg- ΔL. Generally effective length of the transistor can be extracted from measurement or simulation result. But it isn't a reliable technique. The reliable technique is, by looking the total oxide capacitance Cox as a function of Lg. The Cox is given by

$$Cox = (\varepsilon ox/tox)\ Weff\ (Lg-\Delta L) \quad (1)$$

Gate Capacitance (Cg):- It is given by the relation

$$Cg = Co\ W\ L \quad (2)$$

Where C0 is the gate capacitance per unit area given by

$$Co = Єr\ Єo\ /\ D \quad (3)$$

Where, D– Thickness of gate oxide, W – Width of the Channel L – Length of the Channel Єr – Relative permittivity

Channel Resistance (RC): - It is given by the relation

$$RC = \mu\ (L\ /W\ Qon) \quad (4)$$

Where, $Qon = Co\ x\ Vgs$ (4.a)

μ - Is carrier mobility Vgs – gate to source voltage

Gate Delay (Td): - Delay of the gate can be calculated as

$$Td = Ron\ X\ Cg \quad (5)$$

Where, Cg - Gate capacitance

The values of Gate capacitance, Charge per unit area, Gate capacitance per unit area, Gate delay and hannel resistance can be controlled by adjusting the Oxide thickness.

Effect on Leakage Current:

In current CMOS technologies, the sub-threshold leakage current, ISUB, is much larger than the other leakage current components.

A. Leakage current and Dynamic current

In [13], authors have explored the advantages offered by multi-gate fin FETs (FinFETs) over traditional bulk MOSFETs. The leakage-delay saving was obtained with back biasing were explored and evaluated the suitability for low wake-up time and energy-efficient BB schemes. Results were showed that 3T and 4T FinFETs are reduced the leakage at the cost of a moderately worse speed performance and are well suited for implementing fast and energy-efficient adaptive BB strategies. Interestingly, the better leakage reduction achieved by 4T FinFETs is due to the higher threshold sensitivity to back biasing was compared to bulk devices. In [20], authors are performed an extensive simulation on BOI FinFET and analyzed the effect of underlaps using the TCAD. The simulation of BOI FinFET device with underlap were performed. The incorporation of underlap with BOI FinFET device resulted in a significant improvement in SCEs, particularly DIBL reduced to 25%, leakage current reduced to 99% and ION/IOFF increased to 89%.There will be reduction in leakage current and power dissipation, when device is in off condition. The simulations were revealed that the BOI FinFET structures with underlaps are more efficient than conventional BOI FinFET as undoped underlap region reduces DIBL, leakage current(IOFF) and improved the ION/IOFF ratio. In [21] the leakage current and dynamic current are analyzed for the FinFET and CMOS based 7T SRAM at 45 nm node. They considered a mechanism for improving FinFETs efficiency, called variable-supply voltage schemes. The transistor stacking along with variable supply voltage operation of FinFETs obtained a larger leakage savings compared to that of bulk devices. The simulated results for variation of supply voltage from minimum 0.6V to maximum of 1V are verified that FinFETS save a larger leakage and dynamic current. In [12], the leakage current induced by DIBL was well suppressed. DIBL occurs when the depletion region of the drain interacts with the source near the channel surface to lower the source potential barrier. DIBL is increased at higher drain voltage and shorter effective channel length. Surface DIBL is happens before deep bulk punch-through and it decreased the threshold voltage and the leakage current. In [2] they designed 6T SRAM cell using the FinFET and compared it with conventional based 6T SRAM at 45 nm node. The internal transistor sub-threshold leakage current and gate leakage current are observed and compared with the conventional structure of 6T SRAM cell. FinFET SRAM cell is applied with self-controllable voltage level technique and then leakage current and leakage power also observed. The simulation results were carried out on Cadence Virtuoso Tool at 45nm Technology had a leakage current in conventional SRAM cell is 919.3 pA and that of SRAM is 858 pA. The Leakage in SRAM cell is reduced to 10% using FinFET. The resulted total leakage of FinFET SRAM cell is reduced to 34% after they applied for self-controllable voltage level technique. We conclude that better reduction in leakage current and dynamic current is possible in FinFET technology compared with traditional techniques.

B. Power dissipation

In [21], authors have analyzed for the dynamic power for FinFET and CMOS based 7T SRAM at 45 nm node. The simulated results were showed that FinFET saves the more power than that of CMOS. Table I shows the voltage variation scheme for dynamic power for FinFET at 45 nm node.

TABLE I: SIMULATION RESULTS OF FINFET 16 BIT SRAM ARRAY

Parameter	FinFET				
supply voltage	0.6	0.7	0.8	0.9	1
Dynamic power	34.02 nW	313.3 nW	630.5 nW	1.05 µW	1.29 µW

In [1] authors have evaluated and compared the performance of CMOS and FinFET based 6T SRAM cell in 22 technology and compared the 6T SRAM for SG/IG mode are carried out the dynamic power has 1.38e-04 and leakage power has 1.01e-06 at VDD of 0.8V. Among FinFET based SG and IG modes, SG mode design is giving better performance at all the load level. In [4], authors have analyzed the process induced variations on 14-nm technology node silicon on insulator (SOI) FinFET and impact of these variations on delay and static power dissipation of FinFET inverter was presented. The fin width and height variations were considered that the less effect on the static power dissipation of inverter whereas fluctuation in gate oxide

thickness has significant impact on it. The gate oxide thickness is incremented of 10% which reduced the effect of Lg variability on static power dissipation to 85.28%. The effect of variation in static power was minimized by choosing thicker gate oxide as it was reduced the gate leakage current. In [8] they scale down the device from 22nm to 14 nm and compared the parameters in both nodes. The power consumption was reduced in 14 nm than that of 22 nm node. The table II shows the compared power dissipation in 22 nm with 14 nm node. In [1], authors have compared the MOSFET and FinFET based logic circuits using 32nm technology and found that FinFET based circuits are more suitable for low power applications in nanometer regime. The power dissipation is found that 0.247μW for inverter and 0.131 μW and 0.096 μW for NAND2 gate, which is low in SG and IG mode. The FinFET based technology has less power consumption compared with Conventional MOSFET and CMOS technology.

C. Delay

In [3] authors have analyzed the FinFET logic circuits in terms of the delay-tradeoff and compared with bulk circuits. They obtained the delay saving with back biasing and evaluated for low wake-up time and energy efficient BB scheme. In [1] they evaluated the performance were analyzed for FinFET based 6T SRAM and CMOS at 22 nm node. The result of FinFET based 6T SRAM showed that the signal noise margin (SNM) is increased to 25.3% in memory cell and it became 5% faster than CMOS based SRAM. In
[2] they considered the operation speed of FinFET SRAM and CMOS array. The read and write delays are extracted from the function of number of rows. It was found that the FinFET realized the read and write operation roughly twice faster than that of bulk planar one. Table III and IV shows the compared delay operation for CMOS and FinFET SRAM array.

TABLE III: SIMULATION RESULTS FOR CMOS 16 BIT SRAM ARRAY

Parameter	CMOS 16 bit SRAM array				
Supply voltage	0.6	0.7	0.8	0.9	1
Delay (Write)	800.7ps	826.1ps	826.3 ps	818.5 ps	912.2 ps
Delay (Read)	575.4 ps	265.2 ps	771.1 ps	776.3 ps	820.3

In [4], authors have simulated the process induced variations on 14 nm technology node silicon on insulator (SOI) FinFET. The impact of process variation on the delay are minimized to 21.13 % and the height of the fin is decreased to 12%.In [8] they scale down the device from 22nm to 14 nm and compared the parameters in both nodes. The area covered by the device is reduced. Hence the power dissipation is also reduced but the delay in the operation in the device were increased at 14nm node compared with 22nm. The table V shows the compared results for 22 nm and 14 nm. FinFET technology have high speed performance than the

TABLE IV: SIMULATION RESULTS FOR FINFET 16 BIT SRAM ARRAY

Parameter	FinFET 16 bit SRAM array				
Supply voltage	0.6	0.7	0.8	0.9	1
Delay (Write ps)	200.2	188.3	174.5	182.1	193.7
Delay (Read ps)	425.8	254.2	229.6	224.6	229

the traditional one. FinFET based 22nm technology have good reduction in delay compared to 32 nm and 14nm technology.

TABLE V: SIMULATION RESULTS FOR FINFET BASED INVERTER, NAND AND NOR

Parameter	14nm	22nm
Supply Voltage	0.8V	0.9V
Inverter	74.0142ps	45.4125ps
NAND	74.2176ps	42.4052ps
NOR	86.2274ps	51.015ps

III. CONCLUSION

In this paper, Process technology of FinFET is reviewed and the comparative study of MOS, CMOS and FinFET technologies is carried out. FinFET technology is a good alternative to planar CMOS for scaling beyond 32nm and has superior performance for low power applications.

REFERENCES

[1] Aditya waingankar et all.,2016,"Logic Circuits using FinFET: Comparative Analysis" IJSRD, National Conference on Technological Advancement and Automatization in Engineering, January 2016 ISSN:2321-0613
[2] Anshul Jain et al.,2014, " Optimization of Leakage Current and Leakage Power of FinFET Based 6T SRAM Cell" Inte rnational Journal of Engineering Technology, Management and Applied Sciences, August 2014, Volume 2 Issue 3, ISSN 2349-4476
[3] Bazizi.E.M et al.,2015, "Advanced TCADSimulation of Local Mismatch in 14nm CMOS Technology FinFET's" SISPAD 2015, September 9-11, 2015, Washington, DC, USA
[4] Bhattacharya D et al., 2014, "FinFETs:from device to architecture- Review Article", Received 4 June 2014; Accepted 23 July 2014; Published 7 September 2014.
[5] Dominique schreurs et al.,2010"Capabilities and Limitations of Equivalent Circuit Models for Modeling Advanced Si FET Devices", MIXDES 2010, 17th International Conference "Mixed Design of Integrated Circuits and Systems", June 24-26, 2010, Wroc_aw, Poland
[6] Frank He et al.,2010, "FinFET: From Compact Modeling to Circuit Performance", 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)
[7] Girish h et all.,2016, " Design of finfet" international journal of engineering research ISSN: 2319-6890) (online), 2347-5013(print) volume no.5 issue: special 5, pp: 992-1128,20 may 2016
[8] Gracieli Posser et al.,2014, "Performance Improvement with Dedicated Transistor Sizing for MOSFET and FinFET Devices" Conference Paper • July 2014, DOI: 10.1109/ISVLSI.2014.13
[9] Jain A and Saxena M, 2014 "Optimization of Leakage Current and Leakage Power of FinFET Based 6T SRAM Cell" International Journal of Engineering Technology, Management and Applied Sciences, Vol:2, PP 156-163
[10] Khandelwal S et al.,2013 "Leakage current and Dynamic power analysis of FinFET based 7T SRAM at 45nm Technology", International Arab conference on Information Technology (ACIT 2013)