Design of Static RAM Cell Through 16 nm FinFET Technology

Dr. R. Prakash Rao
Associate Professor, ECE Department, Matrusri Engineering College, Saidabad, Hyderabad. India.
prakashiits@gmail.com

Abstract: *Stability is an important performance metric of Static Random Access Memories(SRAMs). A well-designed SRAM must have high stability. This paper proposes a novel 8 transistor SRAM cell to improve read stability and write ability. The proposed novel 8T SRAM memory cell achieves a Read Static Noise Margin (RSNM) of 517.73 mV and Write Static Noise Margin (WSNM) of 504.31 mV using 16 nm FinFET technology at 0.85 V. It provides 6.91x and 0.97x improvement in RSNM; 1.3x and 0.89x improvement in WSNM over conventional 6T and 8T SRAM cells respectively. Read and write delay per read and write operation* are *0.708 ns and 0.439 ns respectively. The measured power consumption of read and write operations is 7.9988 µW and 10.020 µW respectively. The proposed 8T SRAM cell achieves better read stability and write ability while maintaining less cell delay and low power.*

Key Words: SRAM, FinFET, Stability, RSNM, WSNM, Read Delay, Write Delay.

1. INTRODUCTION

Static Random Access Memories (SRAMs) have become an important part of modern electronics. SRAMs are faster compared to Dynamic Random Access Memories (DRAMs) and do not require clocking or frequent refreshing to store the data. The data stored in SRAMs remains stable until power is applied to it. Due to these features of SRAMs, they are mainly used in the cache memory of microprocessors.

Large area of modern-day chips are occupied by SRAMs. On – die cache memory is ever increasing to achieve higher performance benefits in modern microprocessors, portable, mobile and handheld applications in each new technology generation [1]. Thus, the CMOS IC technology has been continuously scaled down to enter the nanometer regime. As the technology scaling enters the nanometer regime, significant challenges such as reliability issues, process variations and Short Channel Effects (SCEs) are faced [2]. Scaling reduces the gate's control on the channel which degrades the performance of the device. SCEs result in undesirable sub-threshold leakage currents. In severe cases, SCEs may also affect the other devices in the chip. Using thinner gate oxide in MOS transistor reduces SCEs at the cost of more power and less reliability [3]. New devices are suggested to overcome SCEs instead [4]-[8]. FinFETs are one of the best devices among these towards deep nanometer technology nodes.

FinFET devices provide superior control on the channel subduing SCEs, lower leakage current and higher ON current compared to CMOS counterpart [9]. They show greater scalability, insensitivity to random variations and better choice of nanometre technology [10]. Hence, robust and energy-efficient SRAM cell designs can be achieved by using FinFET technology.

Stability is an important performance metric of SRAMs. A well-designed SRAM must have high stability. The read and write operations are performed in conventional 6 Transistor SRAM cell differentially. Minimum sized access transistors are required for read operation to reduce the data disturbance which can otherwise result in flipping the stored data in the SRAM cell called read failure. On the other hand, strong access transistors are required to reduce the write access times and improve WSNM. Therefore, problem of sizing of access transistors exists in conventional 6T SRAM cell forcing a compromise between read and write operations with good stability and ability of the cell respectively. For conventional 8T SRAM cell there is an additional requirement of a bitline to improve the stability performance of the cell adhering to area overhead. The proposed novel 8T SRAM cell improves both read stability and write ability relative to conventional 6T and 8T SRAM cells while maintaining less cell delay and low power at 0.85 V using 16 nm FinFET technology.

This paper is organized as follows. Section II briefs FinFET Technology and its working. Section III discusses conventional SRAM cells. Section IV proposes the Novel 8T SRAM cell. Section V discusses simulation results. Section VI deals with the conclusion of the manuscript.

2. FINFET TECHNOLOGY

FinFET is a non-planar structure unlike planar CMOS structure built on Silicon on Insulator (SOI). Around the fin, the gate is deposited to form channel as shown in Fig. 1. A CMOS device has gate only on one side while a FinFET device has gate on three sides, called as multi-gate FinFET.

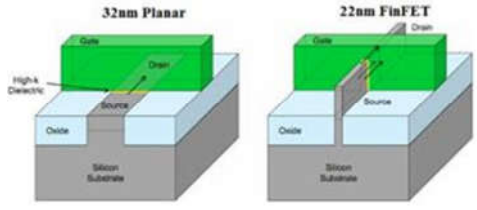

Fig. 1 Planar CMOS structure vs non - planar FinFET structure

FinFETs operate in two modes namely Short – Gate (SG) mode and Independent - Gate (IG) mode as depicted in Fig. 2 (a) and Fig. 2 (b) respectively.

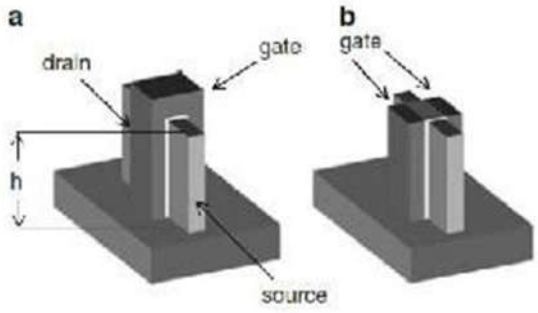

Fig. 2 (a) Short - Gate FinFET (b) Independent - Gate FinFET

3. CONVENTIONAL SRAM CELLS

Six transistors are typically required to store one memory bit. Fig. 3 shows the conventional 6T SRAM cell [3]. Each bit is stored in the latch which consists of series connection of two cross-coupled inverters. The first inverter is formed by PU1 and PD1 while the second inverter is formed by PU2 and PD2. The data bit is stored at node Q and its compliment is stored at node QB. AC1 and AC2 are the access transistors. The stored bit in the SRAM is written to or read from differentially. Weaker access transistors are required for successful read operation while stronger access transistors are required for successful write operation. Thus, design of conventional 6T SRAM cell has the problem of sizing access transistors.

Conventional 8 Transistor SRAM cell is shown in Fig 4 [11]. In this, conventional 6 Transistor SRAM cell acts as the core. Two additional n-type transistors with an additional bitline (RB) and control signal (RWL) are used to isolate the cell core from the output. Wtite operation is performed via access transistors (PG2-PG1) and bitlines WBL and WBLB. The read operation is performed via RG1 and RG2. The data stored in the cell appears on the read bitline RB. PG1 and PG2 are made stronger than PU1 and PU2 for successful write operation.

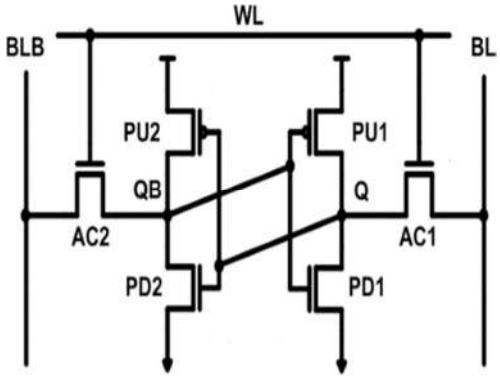

Fig. 3 Conventional 6T SRAM cell (CN6T)

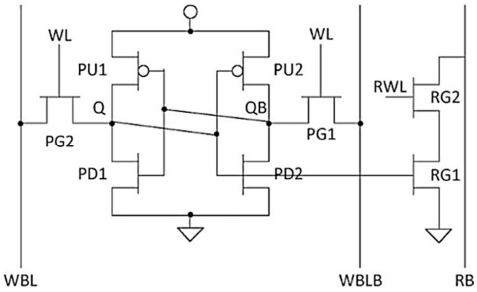

Fig. 4 Conventional 8T SRAM cell (CN8T)

4. PROPOSED NOVEL 8T SRAM CELL

Read and write operations are single ended to overcome the problem of sizing of access transistors. Fig. 5 depicts the structure of the proposed novel 8T SRAM cell. In this cell, write ability is improved by weakening the left inverter before the write operation because the write access transistor can then overpower the feedback loop with ease. This is achieved by floating the supply voltage and ground rails by turning OFF the additional p-type FinFET (P3) and providing a virtual ground for N-type FinFET (N1) respectively. A virtual ground for each column of the SRAM is provided by using a NAND gate and an N-type FinFET. Word-line (WL), write enable signal (wr_en) and the signal for selecting the column (col_sel_j; where j is the index of column) are made high during write operation. The corresponding virtual ground of SRAM becomes float. Virtual ground goes to ground in the other cases.

In conventional 6 Transitor SRAM cell, an increase in the storage node (q) voltage higher than the ground potential due to voltage dividing through the access transistor and pull-down transistor during read operation degrades the cell's resistance to noise. The voltage of storage nodes in the cell (q and qb) can be reversed when it is higher than VT of the other inverter, resulting in a read failure. An additional conducting p-type FinFET (P5) is used in novel 8T SRAM cell to avoid this. The increase in the node (q) voltage is limited below the $V_{DD} - |V_{TP4}| - |V_{TP5}|$, where V_{TP4} and V_{TP5} are the threshold voltages of FinFETs P4 and P5 respectively. In addition to this, the read access transistor (P4) should be designed weaker than its corresponding pull down transistor (N2) for successful read operation. This is achieved inherently as read access FinFET (P4) is p-type and pull-down FinFET (N2) is n-type (implying p-type FinFET has lower hole mobility).

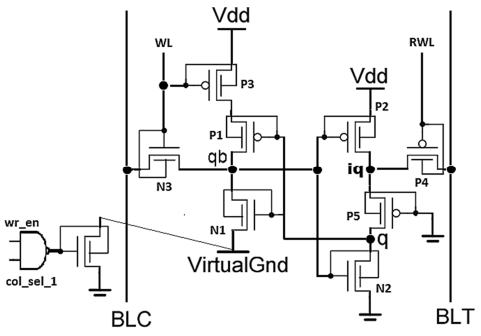

Fig. 5 Proposed Novel 8T SRAM Cell (No8T)

For brevity, in the coming sections, the conventional 6T SRAM cell is referred as CN6T, conventional 8T SRAM cell as CN8T and proposed novel 8T SRAM cell as No8T.

5. RESULTS AND DISCUSSIONS

Cell Delay

The time delay between 50% activation of read enable to when the sense amplifier output has reached 90% of its full swing is called as read delay[10]. Read operation is performed through p-type read access FinFET (P4) and read bitline (BLT). Read delay is 0.708 ns per read operation of the cell. "The time delay between 50% activation of write enable to when node q is 90% of its full swing is called as write delay" [10]. Write operation is performed through n-type write access FinFET (N3) and write bitline (BLC). It is to be noted that the compliment of the data to be written is carried by BLC. Write delay is 0.439 ns per write operation of the cell.

Power Consumption

Only read bitline (BLT) has to be pre-charged due to single ended read operation. HSPICE simulation results show that the power consumption for read logic 1 operation is less since it does not require discharging of read bitline (BLT). Power consumption for write logic 0 operation is more because of the high threshold voltage of conducting p-type FinFET (P5). The advantage of single-ended write operation over differential write cells is that less power is consumed by charging and discharging of only one write-bitline (BLC). HSPICE results for power consumption of Novel 8T SRAM cell are summarized in Table 1.

Table 1. Power consumption of novel 8T SRAM cell

Operation	Logic 1	Logic 0
Read	4.8885 µW	8.9988 µW
Write	6.2237 µW	11.020 µW

Read Stability and Write Ability

Static Noise Margin (SNM) is a major performance metric for analyzing SRAM cell stability [13]. It is the maximum noise which can be tolerated by the device. Stability of SRAM during read and write operations are called as Read Static Noise Margin (RSNM) and Write SNM (WSNM) respectively [13]. Read stability is determined by RSNM of the cell. Higher RSNM indicates good read stability while lower RSNM indicates poor read stability. Write ability of SRAM cell is determined by WSNM. The width of the smallest square that can be embedded between the lower-right half of the curves is called as WSNM [14]. Fig. 6 shows the VTC curve for WSNM characteristics plot of novel 8T SRAM cell. The WSNM is 504.31 mV.

Fig. 7 shows the rotated (45) butterfly plot for novel 8T SRAM memory cell for read operation. The voltage U spans from $-V_{dd}/\text{sqrt}(2)$ to $+V_{dd}/\text{sqrt}(2)$.
V(IQ) and V(QB) are obtained from Fig. 7.

Equations (1), (2), (3) and (4) are used to calculate RSNM of the SRAM cell. The RSNM is 517.73 mV.

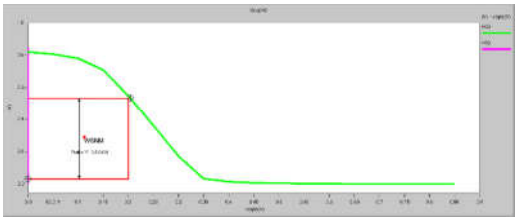

Fig. 6 VTC curve for WSNM characteristics

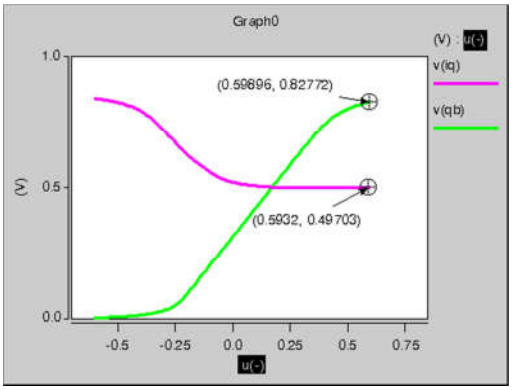

Fig. 7 Rotated (45) butterfly plot of Novel 8T SRAM cell for Read Operation

$$V1 = U + \text{sqrt}(2) * V(IQ) \quad (1)$$
$$V2 = -U + \text{sqrt}(2) * V(QB) \quad (2)$$
$$VD = V1 - V2 \quad (3)$$
$$RSNM = (1/\text{sqrt}(2)) * VD \quad (4)$$

Table 2. gives the RSNM and WSNM results of the prior published work with this work. CN6T provides very less RSNM and WSNM due to conflict of access transistor sizing. CN8T provides good RSNM and WSNM but it requires an additional bitline. No8T has the highest RSNM due to the addition of a conducting p-type FinFET which reduces the read failure and a p-type FinFET read access transistor. It also achieves highest WSNM as the feedback loop is weakened by floating the supply voltage and ground rails during write operation.

6. CONCLUSION

A novel 8T SRAM memory cell is proposed with improved read stability and write ability. To improve the read ability, an additional conducting p-type FinFET and a p-type FinFET read access transistor are used. To improve write ability, the inverter on the left side is weakened during the write operation by floating the VDD and ground rails. Read and write delay per read and write operations is 0.7 ns and 0.3 ns respectively.

Table 2. Comparison of RSNM and WSNM results

Parameter	Published Work			This Work		
	[9]	[16]	[17]	CN6T	CN8T	No8T
Technology	16 nm FinFET	90 nm CMOS	15 nm FinFET	16 nm FinFET		
Supply Voltage (V)	1	0.3	0.7	0.85		
RSNM (mV)	237	98	136.4	64.414	251.81	417.73
WSNM (mV)	312	78	378	229.29	263.58	404.31

REFERENCES

[1] Salahuddin S.M., Jiao H., Kursun V., (2013) A Novel 6T SRAM Cell with Asymmetrically Gate Underlap Engineered FinFETs for Enhanced Read Data Stability and Write Ability. *In Quality Electronic Design (ISQED), 2013 14th International Symposium,* IEEE.

[2] Delgado-Frias J.G., Zhang Z., Turi M.A., (2010) Low Power SRAM Cell Design for FinFET and CNTFET Technologies. *In Green Computing Conference, 2010 International,* IEEE.

[3] Moradi F., Peiravi A., Kargaard J.M., Farkhani H., (2014) Comparative Study of FinFETsversus22nm Bulk CMOS Technologies: SRAM Design Perspective. *In System-on-Chip Conference (SOCC), 2014 27th IEEE International*.

[4] Collaert N., De Keersgieter A., Dixit A., Ferain I., Lai L.S., Lenoble D., Mercha A., Nackaerts A., Pawlak B.J., Rooyackers R., Schulz T., (2008) Multi-Gate Devices for the 32nm Technology Node and Beyond. *Solid-State Electronics*, 52(9), pp.1291-1296.

[5] Noda K., Uchida T., Tatsumi T., Aoyama T., Nakajima K., Miyamoto H., Hashimoto T., Sasake I., (1994) 0.1 µm Delta-Doped CMOS Using Postenergy Implanting Selective Epitaxy. *In VLSI Symp. Tech. Dig*., pp. 19–20.

[6] Yan R., Ourmazd A. and Lee K., (1992) Scaling the Si CMOS: From Bulk to SOI to Bulk, *J. Electron Devices*, 39(7), pp.1704–1710.

[7] Sachid A.B., Hu D., (2012) Denser and More Stable SRAM using FinFETs With Multiple Fin Heights, *J. Electron Devices,* 59, pp. 2037-2041.

[8] Tawfik S.A., Kursun V., (2011) Multi-Threshold Voltage FinFET Sequential Circuits. *J. VLSI systems*, vol. 19, pp. 151-156.

[9] Pasandi G., Fakhraie S. M., (2014) An 8T Low-Voltage and Low-Leakage Half-Selection Disturb-Free SRAM Using Bulk-CMOS and FinFETs, *J. Electron Devices*, 61(7), pp.2357-2363.

[10] Shafaei A., Wang Y., Lin X., Pedram M., (2014) Fincacti: Architectural Analysis and Modeling of Caches with Deeply-Scaled Finfet Devices. *In VLSI (ISVLSI), 2014 IEEE Computer Society Annual Symposium,* IEEE.

[11] Jaksic Z., Canal R., (2013) Comparison of Sram Cells for 10-nm SoI Finfets Under Process and Environmental variations, *J. Electron Devices*, 60(1), pp.49-55.