A FUZZY CONTROLLER BASED STATCOM WITH DIODE-CLAMPED MODULAR MULTILEVEL CONVERTERS

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ABSTRACT-A fuzzy based static synchronous compensator (STATCOM) based on the diode-clamped modular multilevel converter (DCM2C) is proposed in this paper. Based on the structure of modular multilevel converter, the fuzzy DCM2C-STATCOM has the capability of Var compensation and negative-sequence current compensation. The quantity of voltage sensors is significantly reduced and is free from the number of voltage levels. In this converter topology, the capacitor voltage is clamped by using a low power rating diode in each sub module. Furthermore, the voltage balancing control method becomes very simple and the capacitor voltage balance speed is fast. The topology characteristics and compensation control method of DCM2C-STATCOM are investigated in this paper. Simulation results obtained from MATLAB software validate that the capacitor voltage of the proposed DCM2C-STATCOM can be well balanced and the Var and negative-sequence current compensations are effective.

INTRODUCTION

Nowadays, in medium-voltage distribution systems, many power quality issues, such as low power factor, harmonic distortion, and unbalanced voltage, are resulted from the unbalanced loads and nonlinear loads. To improve the power quality, the static synchronous compensators (STATCOM) are widely used on the grid side to achieve high power factor and low distortion. Recently, STATCOM based on multilevel converters are very popular in medium-voltage networks, including flying-capacitor multilevel converters (FCMC), diode-clamped multilevel converters (DCMC), and cascaded H-bridge multilevel converters (CHMC) [1]–[7]. Because there is a dc bus in the topology of the FCMC and DCMC, they have stronger capability of negative-sequence current compensation than the CHMC with star configuration and they can be used in the applications of ac/dc power conversion. However, the poor modularity and significantly increasing capacitors and power diodes restrict their applications in medium/high-voltage networks.

The CHMC with star configuration has good modularity and is very popular in medium-voltage Var compensation applications [8]. In [8], a hierarchical voltage balancing control method is carried out with the phase-shifted unipolar sine PWM method. Based on the same control structure, the low-voltage ride-through issue is solved in [9]. But the CHMC with star configuration has very weak negative-sequence compensation capability. The CHMC with delta configuration can overcome that defect [13], but the voltage across the arm of the converter is line voltage and the number of sub modules (SM) in an arm is increased a lot. Since it was applied in Trans Bay project in 2010, the modular multilevel converter (MMC) topology has gained growing attentions in many applications, such as high-voltage direct current transmission systems, flexible alternating current transmission systems, and STATCOM [14]–[21]. The MMC topology is very promising in mitigation of all the power quality problems. The structure and operating principles for MMC-STATCOM in distorted and unbalanced grid have been widely researched. Mohammadi and TavakoliBina proposed an MMC-STATCOM configuration used for medium-voltage large-current system and an extended configuration EMMC-STATCOM used for high power applications in [18].

Du and Liu presented an MMC based D-STATCOM system, which is able to compensate the seriously unbalanced nonlinear load while keeping all the floating capacitor voltages regulated . Though the MMC topology has many advantages in Var compensation, the capacitor voltage balancing control for all the floating SMs in each leg remains to be a challenging issue, which is a common problem in most multilevel converters. Usually, to realize the capacitor voltage balancing control, a large number of voltage sensors are needed and the amount of calculation in controllers is increased a lot, which maybe prolong the digital control cycle.

In, a kind of DCMC topology is proposed by using the clamping diodes to clamp the capacitor voltages of a multilevel converter with star configuration. The capacitor voltage balancing

control is simplified a lot and the number of capacitor voltage sensors is reduced a lot. However, the negative-sequence current compensation capability is weak and an energy feedback circuit is required. In this paper, the diode-clamped modular multilevel converter (DCM2C) is developed. A balancing branch, which consists of a low power rating diode and an inductor, is added to each SM. With the help of the balancing branches, the capacitor voltages are clamped and sorted naturally from the bottom SM to the top SM in each arm, and the clamping current pulse can be suppressed.

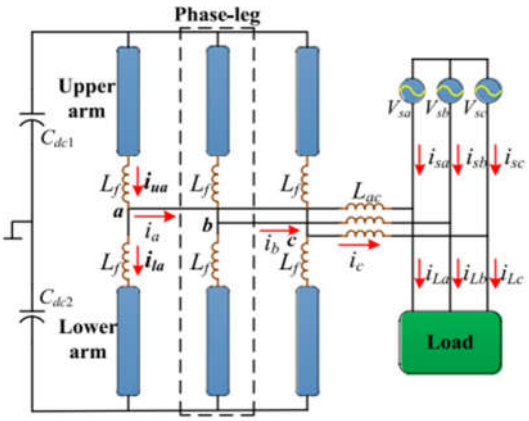


Fig. 1 MMC-STATCOM circuit configuration.

As a result, only the capacitor voltage of the top SM or the bottom SM needs to be measured in each arm. With a simple voltage control method, the capacitor voltage of the top or bottom SM can be controlled to the reference value and then all the SM capacitor voltages in this arm can be balanced. Although the clamping diodes and inductors are required in the DCM2C topology, the reducing cost of voltage sensors and the simplifying of capacitor voltage balancing control have great significance. In this paper, the power circuit and control algorithm of the DCM2C-STATCOM are discussed in detail.

The rest of this paper is organized as follows. Section II introduces the circuit configuration and operation principles of the proposed DCM2C-STATCOM. The sizing calculations and design equations for the inductor are also provided in this section. The voltage balancing control and power compensation control are presented in Section III. Then, Sections IV and V present the MATLAB simulations and experimental results, respectively, to validate the effectiveness of the DCM2C topology as well as the compensation performance of the DCM2C-STATCOM system. The conclusion is presented in Section VI.

STRUCTURE OF DCM2C-STATCOM

A. Capacitor Voltage Clamping Principle of DCM2C-STATCOM

Based on the traditional MMC, the structure of STATCOM configuration is shown in Fig. 1. On the grid side, V_{sj} (j = a, b, c) are the voltage sources. The unbalanced and nonlinear load, for example, the single-phase ac traction system, causes power quality issues, which are expected to be solved by STATCOM. On the converter side, each phase leg consists of an upper arm, a lower arm, and two arm inductors. Bulk capacitors are connected to the dc link. The STATCOM connects to the grid through the ac inductors Lac. As shown in Fig. 2, each arm contains n SMs, denoted as SM1−SMn. A typical SM consists of a dc energy storage capacitor and two power switches (e.g., IGBT).

The topology proposed in [29] uses clamping diodes to sort the SM capacitor voltages in one phase arm and the diodes have a good performance in the balancing process of the capacitor voltages, as shown in Fig. 3(a). The converter runs very well in the steady state; however, there is a potential problem when a high voltage deviation exists between two neighboring SM capacitors in the abnormal conditions.

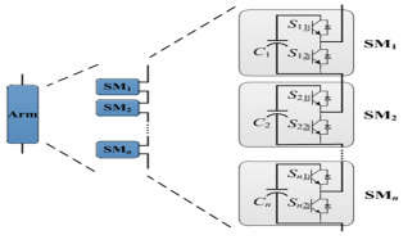


Fig. 2 Structure of SMs in MMC topology

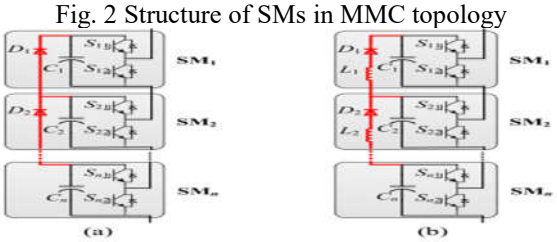


Fig. 3 Connection diagrams of SMs with balancing branches. (a) Using diodes to clamp capacitor voltages. (b) Using diodes and inductors to clamp capacitor voltages.

For example, in the starting process of the converter, the current flowing through the clamping diode will be of high pulses, which may damage the switches. In addition, the current rating of the clamping diodes should be high enough for the recovery from severe unbalance conditions. Fig. 3(b) shows an improved topology. A buffer inductor connected to the clamping diode in serial is used to suppress the current pulses. Considering that the basic structure of the proposed converter is the MMC; this converter is called the diode-clamped MMC.

For simplicity, all the devices in the DCM2C are assumed to be ideal devices. Fig. 4(a) shows the connection diagram of two neighboring SMs in each arm of DCM2C. In this paper, the phase-shifted carrier pulse width modulation (PSC-PWM) method is employed. According to the principles of PSC-PWM, there is a phase shift θ between the each two neighboring triangle carrier waves. Considering that the frequency of the carriers is much higher than that of the reference signal and the existence of the arm inductor Ls, the arm current can be seen as unchanged within a switching cycle. So, the two neighboring SMs absorb or release almost the same amount of energy via the arm current of the converter.

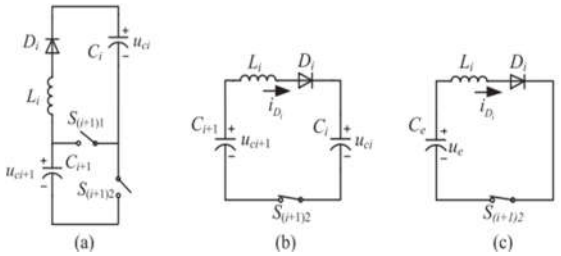


Fig. 4.Diagram of balancing loop between two SMs. (a) S(i+ 1)2 is OFF. (b) S(i+ 1)2 is ON. (c) Equivalent circuit for the balancing loop.

Thus, we can assume that the capacitor voltage difference between two neighboring SMs is not affected by the arm current. Now, neglecting the energy absorbed or released through the main power circuit in each switching period, the capacitor Ci, Ci+1, switch S(i+1)2, and the balancing branch constitute a closed loop when switch S(i+1)2 is ON (see Fig. 4). The simplified circuit of Fig. 4(a) can be derived, as shown in Fig. 4(b). If capacitor voltages u_{Ci}+1 > u_{Ci}, current iDi will appear and flow from Ci+1 to Ci. Conversely, if u_{Ci}+1 ≤u_{Ci}, no current will appear in the balancing branch and the clamping diode will keep off. When switch S (i+1)2 is OFF, the circuit loop is open and there is no energy exchange between the two capacitors.

According to the equivalent circuit of the balancing loop shown in Fig. 4(c), the following equation can be derived:

$$\begin{cases} C_e = \dfrac{C_i}{2} = \dfrac{C_{i+1}}{2} \\ u_e = u_{Ci+1} - u_{Ci} \end{cases} \quad (1)$$

Where C_e is the equivalent capacitor across which the voltage is u_e. Clearly, the circuit is a second-order circuit and the linear differential equation can be derived as follows:

$$LC\frac{d^2u_e}{dt} + u_e = 0 \quad (2)$$

Assume that p1 and p2 are the Eigen values of the above differential equation, then

$$\begin{cases} p_1 = j\omega_0 = j\dfrac{1}{\sqrt{L_iC_e}} \\ p_2 = -j\omega_0 = -j\dfrac{1}{\sqrt{L_iC_e}} \end{cases} \quad (3)$$

If the initial voltage of C_e is U0 when S (i+1)2 turns on, ue and the diode current iDi can be derived as follows:

$$\begin{cases} i_{Di} = -\dfrac{U_0}{L_i(p_2 - p_1)}(e^{p1t} - e^{p2t}) \\ u_e = \dfrac{U_0}{(p_2 - p_1)}(p_2e^{p1t} - p_1e^{p2t}) \end{cases} \quad (4)$$

Take ΔT, Tosc as the on-state time of S(i+1)2 and the period of the oscillation, respectively. According to (4), it can be seen that if the diode in Fig. 4(c) is bypassed and ΔT > Tosc, the voltage ue and current iDi will naturally oscillate continuously, as shown in Fig. 5(a). Capacitors Ci and Ci+1 are charged and

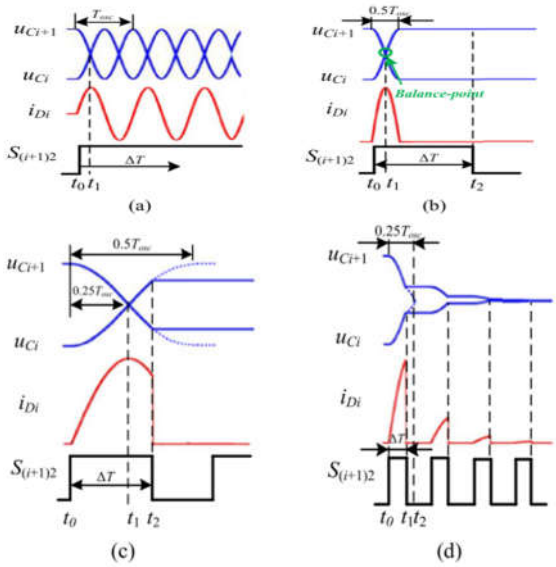


Fig. 5 Voltage and current diagrams in the equivalent circuit of the balancing loop. (a) With the clamping diode bypassed. (b) With the clamping diode enabled and ΔT > 0.5Tosc. (c) With the clamping diode enabled and 0.25Tosc < ΔT < 0.5Tosc. (d) With the clamping diode enabled and ΔT < 0.25Tosc discharged alternately and iDi is ac current. Tosc can be obtained as follows:

$$T_{osc} = 2\pi\sqrt{L_iC_e} \quad (5)$$

However, with the existence of the clamping diode Di, the oscillation of ue and iDi cannot be sustained in the aforementioned process. If ΔT > 0.5Tosc, as shown in Fig. 5(b), when S(i+1)2 turns on, the two capacitor voltages will exchanged and the current iDi flows from Ci+1 to Ci without reverse. Yet the balance of the capacitor voltages is the control purposes. Apparently, the final state of the

two capacitor voltages in Fig. 5(b) is "over balanced."

If 0.25Tosc < ΔT < 0.5Tosc, as shown in Fig. 5(c), when S(i+1)2 turns on, the current iDi also flows from Ci+1 to Ci. In this situation, S (i+1)2 turns off at t2 near t1, the final deviation between the capacitor voltages is smaller and the balancing performance is better. If 0.25Tosc = ΔT, the final deviation between the capacitor voltages is zero theoretically. However, if ΔT < 0.25Tosc, as shown in Fig. 5(d), the voltage deviation between the two capacitors will be reduced, but higher than zero in a switching cycle. It will be smaller and smaller, and after several switching cycles, the capacitor voltage can be balanced finally. The balancing process is longer than that in the other situations presented above. When the difference of ΔT and 0.25Tosc is higher, the quantity of switching cycles of the balancing process becomes larger.

However, the duty cycle of PWM is variable in the applications of the converter and it is impossible to keep ΔT ≤ 0.25Tosc in each period. Nevertheless, in the long run, the balancing performance between two capacitor voltages is still relevant to the relationship of switching frequency fs and oscillation frequency fosc.

According to the analysis above, the inductance in the balancing branch should be well designed to achieve good capacitor voltage balance with small deviation.

Thus, with the clamping diodes and inductors to sort the SM capacitor voltages, the voltage of upper capacitor is always higher than or equal to that of the lower capacitor as follows:

$$u_{Ci} \geq u_{Ci+1} \qquad (6$$

Then, all the capacitor voltages in each arm will show an ascending order from SMn to SM1 as follows:

$$u_{C1} \geq u_{C2} \geq \cdots \ldots \geq u_{Cn} \qquad (7)$$

It can be seen that without any control in each arm, all the capacitor voltages except u_{C1} are clamped by the diodes. If $u_{C1} = u_{Cn}$ is realized, all the capacitor voltages will be balanced. The control principle is presented in the following section.

CLAMPING INDUCTOR SIZING

Power deviations among the SMs, which are mainly caused by the difference of switch losses, modulation, and switching signal transfer delay, should be analyzed first for sizing the inductance in the balancing branch.

In one SM, the switch losses mainly consist of conduction losses and switching losses (without considering the leakage power in the capacitor and the losses resulted from the parasitic parameters in the dc link). Both IGBTs and freewheeling diodes (FWDs) have conduction losses as follows:

$$P_{c,T}(t) = \left[u_T + R_T i^{\beta}(t)\right] i(t) \qquad (8)$$

$$P_{c,D}(t) = [u_D + R_D i(t)] i(t) \qquad (9)$$

Here, Pc, T (t) and Pc, D (t) represent the conduction losses of IGBT and FWD, respectively. u_T and u_D are the forward on voltage. RT and RD are the equivalent resistance. β is a constant related to the specification of the IGBT, and i(t) is the arm current. The IGBTs also have switching losses as follows:

$$\begin{cases} E_{on} = \int_0^{t_{on}} u(t) i(t) dt \\ E_{off} = \int_0^{t_{off}} u(t) i(t) dt \end{cases} \qquad (10)$$

Here, E_{off} and Eon are the turn-on and turn-off losses, respectively. u(t) is the instantaneous voltage of IGBT when turning on and off. So, in one SM, the switch losses E_{sw} can be obtained as follows:

$$E_{sw} = \int_0^{2\pi} (P_{c,T}(t) + P_{c,D}(t)) dt + E_{on} + E_{off} \qquad (11)$$

The switch losses account for a small proportion of the power of an SM PSM making the proportion be λ (generally, λ is smaller than 5%). The difference of power devices in the electrical characteristics is also very small, making it be γ. The PSC modulation strategy and signal transfer delay can also cause small power difference among the SMs, making it be δ. Let us take SM1 and SM2 as an example and assume that u_{C2} is higher than u_{C1}. In normal conditions, the power difference P_{diff} between the two SMs can be described as

$$P_{diff} = (\lambda\Upsilon + \delta) P_{SM} \qquad (12)$$

Here, PSM is the average power of the two SMs. The instantaneous SM power is the product of SM output voltage and arm current. In one grid period, the average power can be

$$P_{SM} = \frac{1}{T} \int_0^T D u_{C,bal} i(t) dt \qquad (13)$$

Here, uC bal is the average capacitor voltage of the two SMs. T and D are the period of the grid voltage and PWM duty cycle, respectively. Expanding to the whole arm, uC bal = Udc / N. When a clamping diode is applied to balance the two SMs, SM2 will supply power for SM1 and their capacitor voltages will be balanced. The power flowing through the diode is half of Pdiff as

$$\frac{P_{diff}}{2} = u_{C,bal} i_{D\_av} \qquad (14)$$

Here, iD av is the average current flowing through the clamping diode. Substituting (13) and (14) into (12), the diode average current can be rewritten as

$$i_{D\_av} = \frac{1}{2T} (\lambda\Upsilon + \delta) \int_0^T i(t) dt \qquad (15)$$

When selecting clamping diodes and inductors, iD av can be considered as the reference value of average forward current IF , namely

$$I_F = \sigma i_{D\_av} \quad (16)$$

Here, σ is a proportionality coefficient, and σ is larger than 1 for enough current margin. Specifically, the peak current of the diode iD peak should be lower than the nonrepetitive forward surge current (IFSM). According to the datasheets of the diodes provided by the manufacturers, in a short time (normally several milliseconds), IFSM is allowed to be much higher than IF , making the ratio be τ. (τ can be higher than 10.) The relation can be obtained as follows:

$$i_{D\_peak} \le I_{FSM}, I_{FSM} = \tau I_F \quad (17)$$

The iD peak depends on the clamping inductor L. The relation of diode current and L is described in Fig. 6.

The dashed lines are the envelopes of the diode currents. It can be seen that when L gets smaller, the envelope slope and iD peak get larger. Consider (17), the inductor must be large enough to suppress the diode current and make the peak value lower than IFSM. Considering (3) and (4), the diode current can be obtained as follows:

$$i_D = \frac{U_o}{\sqrt{\frac{L}{Ce}}} \sin\left(\frac{t}{\sqrt{LC_e}}\right) \approx \frac{U_o}{\sqrt{\frac{L}{Ce}}} \times \frac{t}{\sqrt{LC_e}} = \frac{U_o t}{L} \quad (18)$$

Here, U0 is the initial voltage deviation between the two SM capacitors. Considering (12) and (13), U0 can be obtained as

$$U_o = (\lambda\Upsilon + \delta) u_{C,bal} \quad (19)$$

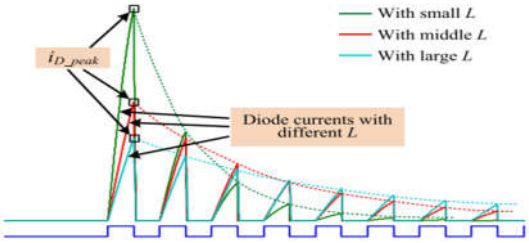


Fig. 6 Relation diagram of diode current and clamping inductance.

When PWM duty cycle D gets higher, the current peak value is larger. In order to make the final inductance be qualified, the duty is specified as 100%. Substituting (19) into (18), the peak value can be

$$i_{D\_peak} = i_D|_{t=T} = \frac{(\lambda\Upsilon+\delta) u_{C,bal} T_S}{L} \quad (20)$$

Here, Ts is the switching period, Ts = f1s . Substituting (20) into (17), the required inductor L can be derived as

$$L \ge \frac{(\lambda\Upsilon+\delta) u_{C,bal}}{\tau f_s I_F} \quad (21)$$

Based on the average current iD av shown in (16) and the minimum inductance shown in (21), sizing of the clamping inductor becomes easy. The inductors with Kool Mμ (Sendust) cores are widely used and low cost. According to the information provided by Magnetics, Inc., Kool Mμ material can be applied as the inductor toroid core for its low losses and relatively high saturation level, Bm = 10500 Gs. The calculation equation of inductance and core parameters is given as

$$L = \frac{\mu_0 \mu_r N_T^2 A_e}{l_e}$$

Where μ0 is the permeability of vacuum. μr is the core permeability, and NT is the number of turns. Ae and le are the effective cross section and core magnetic path length, respectively. The minimum size of inductor core is that when the current peak iD peak flows through the inductor, the flux just reaches saturation (enough magnetic flux density margin should be considered), as

$$\begin{cases} B_m = \mu_r H \\ H l_e = N_r i_{D\_peak} \end{cases} \quad (23)$$

Here, H is the magnetic field intensity. Substituting (23) into (22) to replace NT , the inductance can be rewritten as

$$L = \frac{\mu_0 B_m{}^2 l_e A_e}{\mu_r i_{D\_peak}{}^2} \quad (24)$$

Modify (24) and the sizing of the inductor can be obtained as

$$l_e A_e = \frac{\mu_r L i_{D\_av}{}^2}{\mu_0 B_m{}^2}$$

Considering (21) and (25), the product le Ae should meet the following demand:

$$l_e A_e \ge \frac{(\lambda\Upsilon+\delta)\mu_r u_{C,bal} i_{D\_av}}{\tau\sigma\mu_0 B_m{}^2 f_s} \quad (26)$$

According to (26), the core size can be located on the production table provided by the core companies. Practically, without cutting the production of leAe, low le can be selected to make the inductor dimension small. Considering the low average diode current, the diameter of the copper wire can be very small. Hence, no concerns for the fulfillment of the required turns are needed.

OPERATION PRINCIPLES

The control block diagram of DCM2C-STATCOM is proposed in Fig. 7, which is composed of four parts, A, B, C, and D. All the parts will be discussed in the following.

A. Capacitor Voltage Balancing Control

As shown in Fig. 8, the reference signal of lower arm is shifted by 180° compared to that of upper arm. So, assume that the dc component of the PWM duty cycle is Ddc, the relation of upper arm capacitor

voltages uCui, lower arm capacitor voltages uCli, and dc bus voltage udc is derived as follows:

$$\sum_{i=1}^{n} u_{Cui} \times D_{dc} + \sum_{i=1}^{n} u_{Cli} \times D_{dc} = u_{dc} \quad (27)$$

Since Ddc is 0.5, as shown in Fig. 8, then

$$\sum_{i=1}^{n} u_{Cui} + \sum_{i=1}^{n} u_{Cli} = 2u_{dc} \quad (28)$$

Only six voltage sensors are required in this converter, which are located in the six top SMs in the six arms of the converter. uC 1 can be controlled close to the reference value uC 1ref . Here, uC 1ref = udc/n, considering (7) and (28), then

$$u_{Cui} = u_{Cli} = \frac{u_{dc}}{n}, \quad i = 1,2, \ldots, n$$

As shown in Fig. 7 part A, the pulse width adjustment method is used to control capacitor voltage uC 1 in each arm. Because the capacitor voltage is determined by the active power flowing into an SM, the capacitor voltage can be regulated by adjusting the power of the SM. The PI regulators are used to realize the capacitor voltage control. The sign function is shown as follows:

$$\text{sign} = \begin{cases} 1, & \text{armcurrent} > 0 \\ -1 & \text{armcurrent} < 0 \end{cases} \quad (30)$$

Case 1 (arm current > 0):

The output of voltage PI controller Vua is added to the output of current controller output and the result is sent to the PSC-PWM unit. When capacitor voltage uC 1 < udcref, Vua is positive and the duty cycle of SM1 increases. As a result, the SM1 absorbed more active power from arm current and uC 1 rises. When capacitor voltage uC 1 > udcref, Vua is negative and the duty cycle of SM1 decreases. As a result, the SM1 absorbed less active power from arm current and uC 1 drops.

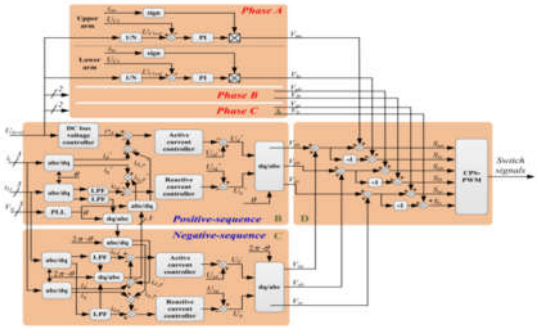


Fig. 7. Proposed control block diagram of DCM2C-STATCOM.

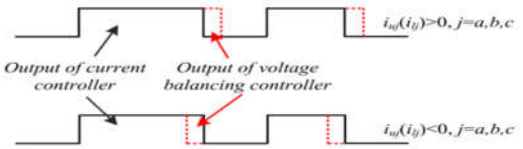


Fig. 8.Diagram of PWM duty cycle adjustment for capacitor voltage regulation

Case 2 (arm current <0):

The output of voltage PI controller Vua is subtracted from the output of current controller output. When capacitor voltage uC 1 < udcref, Vua is positive and the duty cycle of SM1 decreases. As a result, the SM1 emitted less active power to arm current and uC 1 rises. When capacitor voltage uC 1 > udcref, Vua is negative and the duty cycle of SM1 increases. As a result, the SM1 emitted more active power to arm current and uC 1 drops.

The aim of PWM duty cycle adjustment is to make SM1 to absorb more power or emit less power when uC 1 < uC 1ref, and absorb less power or emit more power when uC 1 > uC 1ref. The outputs of voltage balancing controllers are Vuj and Vlj (j =a, b, c), corresponding to the upper and lower arms in the three phases. The diagram of PWM duty cycle adjusting method is introduced in Fig. 8.

POWER CONTROL IN POSITIVE SEQUENCE

As shown in Fig. 7 part B, a phase lock loop (PLL) module is used to estimate the phase angle θ of the grid voltage, which is used in the coordinate transformation. The output current of the STATCOM is transformed into the dq coordinates. Then, a feedback control loop is used for the dc bus voltage control and another one is used for the reactive power compensation control. The dc bus voltage is regulated according to udcref and a PI controller is employed to estimate the active power required by the STATCOM, while the reactive current controller helps to accomplish the function of Var compensation. Here, the active and reactive components of output current in positive sequence are obtained as follows:

$$\begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} = C_{abc/dq} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (31)$$

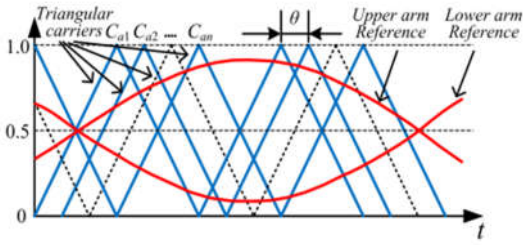


Fig. 9.PSC-PWM method diagram

TABLE I

PARAMETERS OF THE MODEL

Items	Symbol	Values
DC-link voltage	u_{dc}	10 kV
Total no. of SMs in each arm	n	10
SM capacitor	C	4700 μF
Arm inductor	L_a	3 mH
Switching frequency	f_s	2 kHz
Clamping inductor	L_i	100 μH
Filter inductor	L_{ac}	10 mH
Grid voltage (line voltage)	V_{sj}	6 kV rms

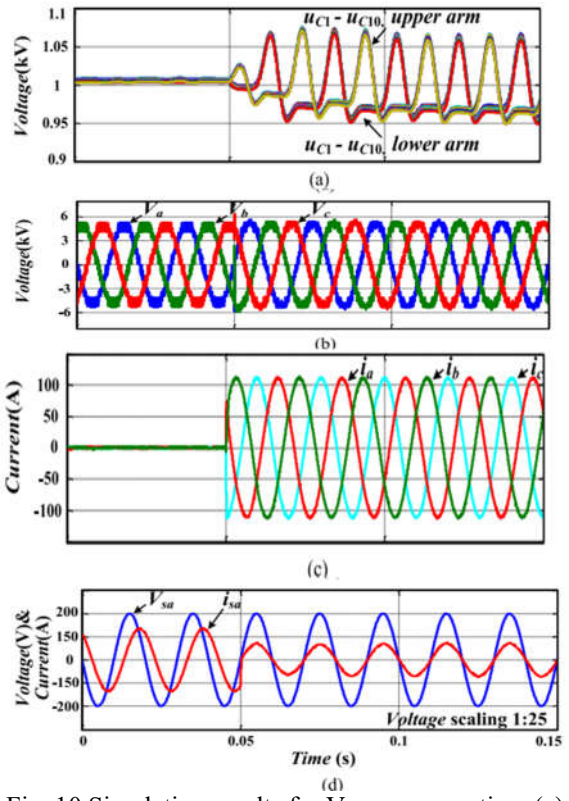
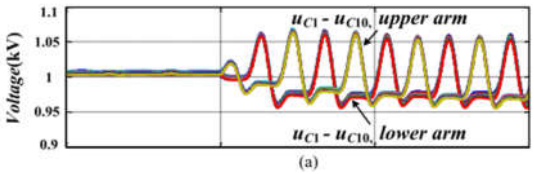


Fig. 10.Simulation results for Var compensation. (a) Capacitor voltages in upper and lower arms. (b) Output voltages of the STATCOM. (c) Output currents of the STATCOM. (d) Voltage and current on the grid side.

Where Cabc/dq is the coordinate transformation which is

$$C_{abc/dq} = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin\left(\theta-\frac{2}{3}\pi\right) & \sin\left(\theta+\frac{2}{3}\pi\right) \\ \cos\theta & \cos\left(\theta-\frac{2}{3}\pi\right) & \cos\left(\theta+\frac{2}{3}\pi\right) \end{bmatrix} \quad (32)$$



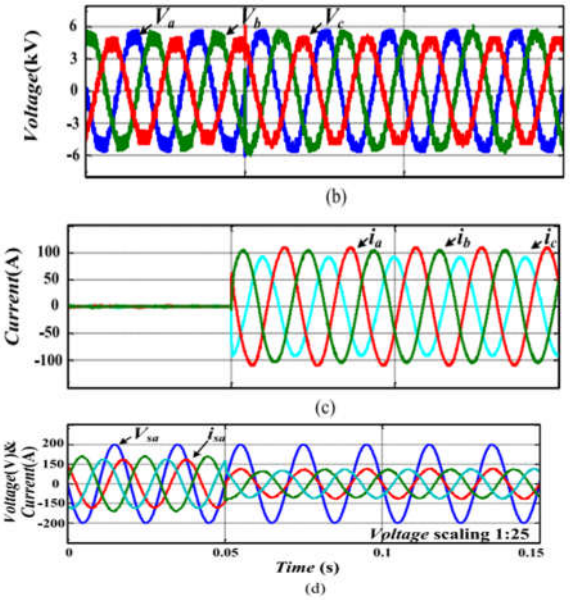


Fig. 11.Simulation results for Var and negative-sequence current compensation. (a) Capacitor voltages in upper and lower arms. (b) Output voltages of the STATCOM. (c) Output currents of the STATCOM. (d) Voltage and currents on the grid side.

Similarly, the reference reactive current is calculated from the load current as Similarly, the reference reactive current is calculated from the load current as

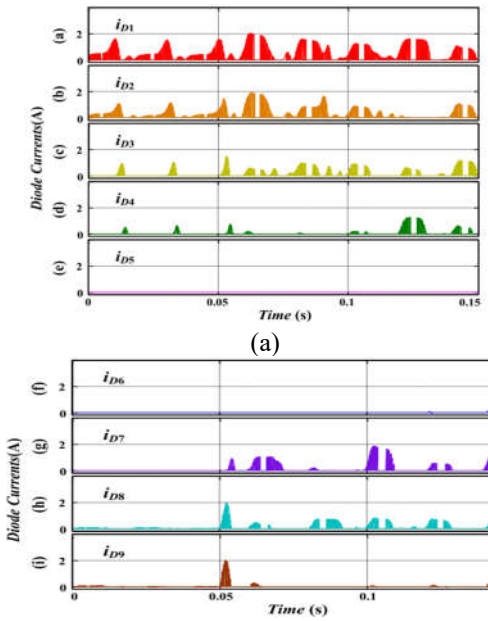
$$\begin{bmatrix} i_{Ld}^{+} \\ i_{Lq}^{+} \end{bmatrix} = C_{abc/dq}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (33)$$

$$\begin{bmatrix} u_{sd}^{+} \\ u_{sq}^{+} \end{bmatrix} = C_{abc/dq}\begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} \quad (34)$$

Where i+ Ld and i+ Lq are the active and reactive components of load current ilj (j = a, b, c) in positive sequence, respectively. u+ sd and u+ sq are the active and reactive components of grid voltage usj (j = a, b, c), respectively, which are introduced as feed forward components to enhance the dynamic response of the current control. The output of voltage regulation and Var compensation is achieved as follows:

$$\begin{bmatrix} V_{pa} \\ V_{pb} \\ V_{pc} \end{bmatrix} = C_{dq/abc}\begin{bmatrix} u_{sd}^{+} \\ u_{sq}^{+} \end{bmatrix} \quad (35)$$

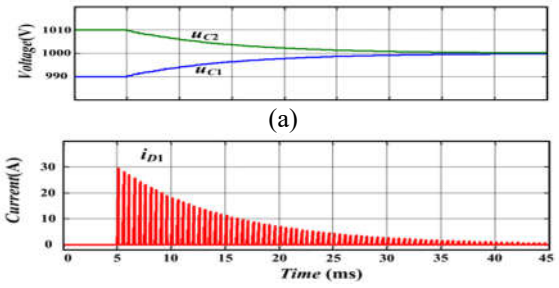
Where u+ d and u+ q are the sum of the output of the current controller and the feed forward component of the grid voltage, as shown in Fig. 7 part B. Cdq/abc is the coordinate transformation



(a)

(b)

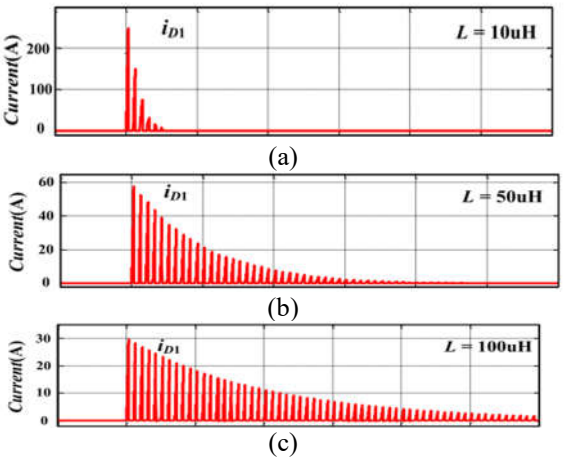
Fig. 12.Simulation results for diode currents. (a) Currents in D1−D5 . (b) Currents in D6−D9 .



(a)

(b)

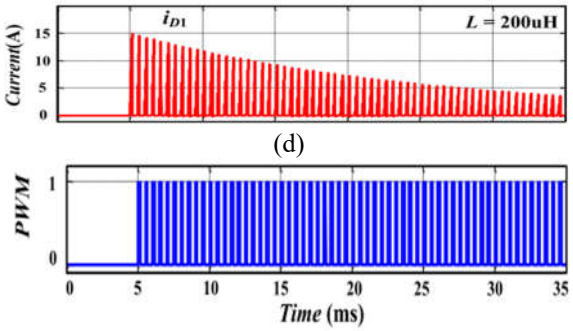
Fig.13. Simulation results for capacitor voltage balancing process between two SMs. (a) Capacitor voltages. (b) Diode current. (c) Switching signals.



(a)

(b)

(c)



(d)

(e)

Fig.14 Simulation results for diode current versus balancing inductance. (a)–(d) Diode currents with difference inductance. (e) Switching signals.*as follows*:

$$C_{dq/abc} = \begin{bmatrix} \sin\theta & \cos\theta \\ \sin\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta - \frac{2}{3}\pi\right) \\ \sin\left(\theta + \frac{2}{3}\pi\right) & \cos\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \quad (36)$$

POWER CONTROL IN NEGATIVE SEQUENCE

As shown in Fig. 7 part C, such as the positive-sequence components of the load current, the active and reactive components with negative-sequence can also be achieved by using the coordinate transformation of Cabc/dq. But there are dc component and ac component with double line-frequency in the conversion result. The dc components iLd and iLq are extracted through two low-pass filters, respectively. The phase angle used in the negative-sequence coordinate transformation is

$$\theta^- = 2\pi - \theta \quad (37)$$

The output of negative-sequence compensation can also be achieved as follows:

$$\begin{bmatrix} V_{na} \\ V_{nb} \\ V_{nc} \end{bmatrix} = C_{dq/abc} \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} \quad (38)$$

Where the Cabc/dq is based on phase angle θ– as

$$C_{dq/abc} = \begin{bmatrix} \sin\theta^- & \cos\theta^- \\ \sin\left(\theta^- - \frac{2}{3}\pi\right) & \cos\left(\theta^- - \frac{2}{3}\pi\right) \\ \sin\left(\theta^- + \frac{2}{3}\pi\right) & \cos\left(\theta^- + \frac{2}{3}\pi\right) \end{bmatrix} \quad (39)$$

Switching Modulation As shown in Fig. 7 part D, the PSC-PWM method is employed to generate the switching signals. As presented in Fig. 9, the phase difference of the reference for the upper arm and the one for the lower arm is π, without considering the output of voltage balancing controllers. The final modulation waves for six arms are obtained as follows, where j = a, b, c:

$$\begin{bmatrix} S_{uj} \\ S_{ij} \end{bmatrix} = \begin{bmatrix} V_{pj} \\ -V_{pj} \end{bmatrix} + \begin{bmatrix} V_{nj} \\ -V_{nj} \end{bmatrix} + \begin{bmatrix} V_{uj} \\ V_{uj} \end{bmatrix} \quad (40)$$

SIMULATION RESULTS

To verify the proposed DCM2C-STATCOM structure, a three phase model was built in MATLAB/Simulink environment. The simulation parameters are shown in Table I. Figs. 10 and 11 show the simulation results for positive sequence reactive current compensation and negative-sequence current compensation, respectively. The compensation begins at t = 0.05 s. As shown in Figs. 10(a) and 11(a), the DCM2C topology achieves a good voltage balancing performance. The output voltages and currents of the STATCOM are shown in

TABLE II
PARAMETERS OF THE PROTOTYPE

Items	Symbol	Values
Phase voltage peak value	V_{sj}	100 V
Phase voltage frequency	f	50 Hz
DC-link voltage	u_{dc}	300 V
Total no. of SMs in each arm	n	6
SM capacitor	C	1100 μF
Arm inductor	L_s	200 μH
Switching frequency	f_s	2 kHz
Clamping inductor	L_i	50 μH
Filter inductor	L_{ac}	2 mH
Three-phase load	R_L	12 mH + 10 Ω, star-connection

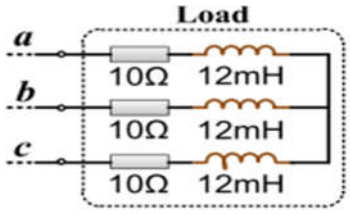


Fig. 15. Diagram of balanced load for Experiments I and II.

Fig. 10(b) and (c) and Fig. 11(b) and (c). Fig. 10(d) shows the compensation for positive-sequence reactive current, and Fig. 11 shows the compensation for both positive- and negative sequence currents. In order to enlarge the power difference between the SMs, a 4-kΩ resistor is attached to SM1. The currents flowing through the clamping diodes are shown in Fig. 12. It can be seen that the currents are intermittent, and all the amplitudes are lower than 2 A, much lower than that of output currents shown in Fig. 11(c).

Fig. 13 shows the voltage balancing process between SM1 and SM2. The initial voltage deviation is 20 V, and the two capacitor voltages get balanced in about 0.3 s. With the help of the 100 μH inductance in the balancing branch, the current maximum peak is suppressed to 30 A roughly, as shown in Fig. 13(b). Fig. 14 simulates the diode current with different balancing inductors in the balancing branch. The initial voltage deviation is still 20 volts. From 14(a) to (d), it can be seen that the diode current maximum peak inversely relates to the inductance value. This indicates that the inductor can effectively suppress the diode current.

DISCUSSION

For the first time, Gao et al. applied clamping diodes in the voltage balancing control of modular multilevel converter with star configuration. Without complex control methods or numerous voltage sensors, the clamping diodes and energy feedback circuits can regulate the SM capacitor voltages effectively. However, the clamping diode current maybe high current pulses when the capacitor voltage deviation is high in the abnormal conditions. Inductors are added to the clamping circuits in the proposed topology. According to the simulation results shown in Fig. 14, the inductors are necessary in suppressing the diode current: when the inductance is 0 or very small, the current peak is very high, which may destroy the devices; when the inductance is higher, the current peak can be suppressed to be acceptable. Appropriate inductance can be derived by referring Section II-B. The clamping current can be

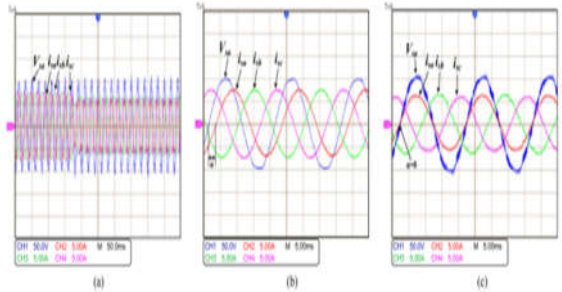


Fig. 16 Experiment results of Var compensation for balanced load. (a) Dynamic process of compensation. (b) Enlarged view before compensation. (c) Enlarged view after compensation.

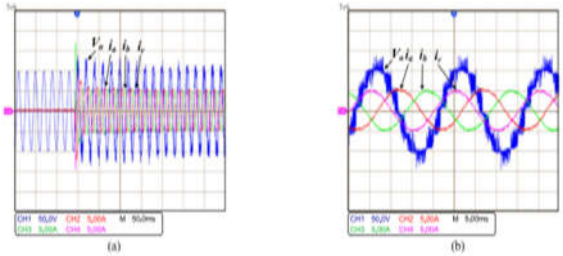


Fig. 17. Simulation results on the converter side. (a) Dynamic process of compensation. (b) Enlarged view after compensation.

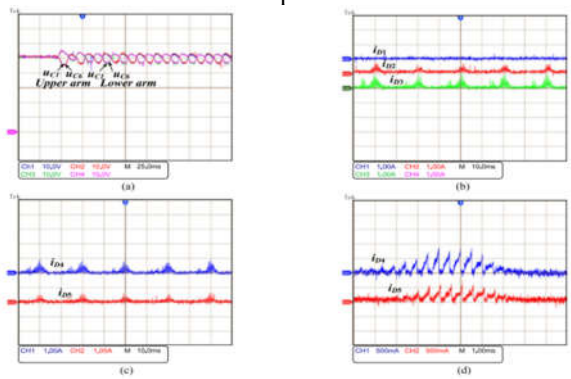


Fig. 18.Simulation results of the capacitor voltage balancing process. (a) Capacitor voltages of upper and lower arm in dynamic process of Var compensation. (b) Clamping diode currents iD1, iD2 , and iD3 after compensation. (c) Clamping diode currents iD4 , iD5 after compensation. (d) Enlarged view of currents iD4 and iD5.

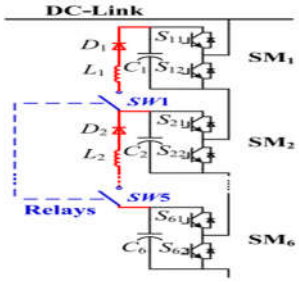
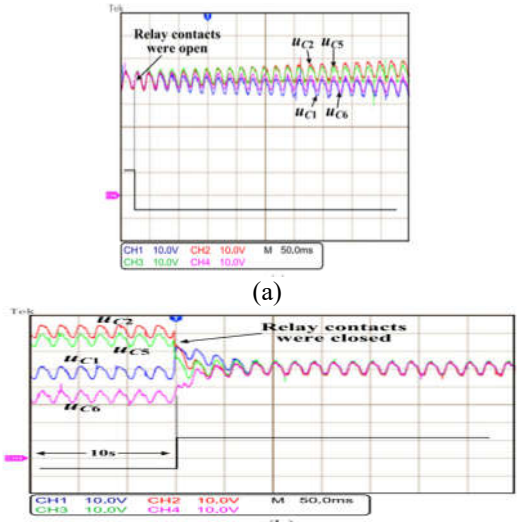


Fig. 19.Diagram of using relays to cut in and cut off the balancing branches



(a)

(b)

Fig. 20.Capacitor voltage waveforms of SM1 , SM2 , SM5 , and SM6 in uppe arm of phase A. (a) Cutting off the balancing branches. (b) Cutting in the balancing branches.

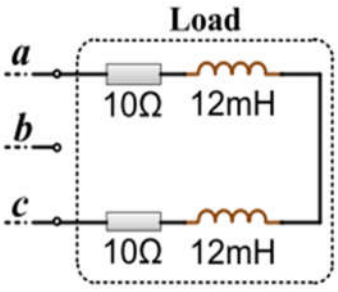


Fig. 21.Diagram of phase-lost load in Experiment III

Suppressed effectively and the energy feedback circuits are not needed for the proposed converter compared with that in [29]. However, the adding inductors will increase the complexity and the cost of circuits in theory.

CONCLUSION

This paper presents fuzzy based static synchronous compensator (STATCOM) based on the diode-clamped modular multilevel converter (DCM2C) the proposed DCM2C uses clamping diodes to keep the SM capacitor voltages balanced. The main advantage of this topology is that the quantity of capacitor voltage sensors is significantly reduced and the balancing control method is very simple. Furthermore, the capacitor voltage balance speed is fast. Although extra clamping diodes and inductors are required in the novel topology than that of the traditional MMC, the current rating of the diodes and inductors is much lower than the current rating of the main power branch of the converter. So, the cost of DCM2C is not much higher than that of the traditional MMC.

With the proposed power control strategy, the DCM2C STATCOM system can realize Var compensation and negative sequence current compensation. Simulation results have verified the effectiveness of the DCM2C topology along with the proposed power control strategy.

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