Three Phase Multilevel Inverter Using Switched Capacitor Units Fed Induction Motor Drive

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Abstract- Multilevel inverters have been attracting in favor of academia as well as industry in the recent decade for high-power and medium-voltage energy control. In addition, they can synthesize switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. The proposed inverter can output more numbers of voltage levels in the same number of switching devices by using this conversion. The number of gate driving circuits is reduced, which leads to the reduction of the size and power consumption in the driving circuits. The total harmonic of the output waveform is also reduced. The proposed inverter outputs larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors. In this paper two new topologies have been proposed for multilevel inverters. The proposed topologies consist of a combination of the conventional series and the switched capacitor inverter units. The proposed method introduces 17, 25 levels and three phase 25level Inverter fed Induction Motor drive. With the use of high level inverter, resolution is increase and also the harmonics is highly reduced. The simulation results are presented by using Matlab/simulink software.

Keywords: Multilevel inverter, series inverters, series– parallel connection, switched capacitor, induction motor.

I. Introduction

Power electronic converters, particularly dc/air conditioning PWM inverters have been broadening their scope of utilization in industry since they give decreased vitality utilization, better framework effectiveness, enhanced nature of item, great upkeep, etc. For a medium voltage matrix, it is troublesome to associate just a single power semiconductor switches straightforwardly [1]. Therefore, a staggered power converter structure has been presented as an option in high power and medium voltage circumstances, for example, laminators, factories, transports, siphons, fans, blowers, blowers, etc. As a practical arrangement, staggered converter accomplishes high power appraisals, as well as empowers the utilization of low power application in sustainable power sources, for example, photovoltaic, wind, and energy units which can be effectively interfaced to a staggered converter framework for a powerful application. The most widely recognized beginning use of staggered converters has been in footing, both in trains and track-side static converters [2].

Recently, some new topologies of staggered inverters have risen. This incorporates summed up staggered inverters, blended staggered Introduction 4 inverters [10], cross breed staggered inverters [11] and delicate exchanged staggered inverters. These staggered inverters can expand appraised inverter voltage and power by expanding the quantity of voltage levels. They can likewise build proportional exchanging recurrence without the expansion of real

exchanging recurrence, accordingly lessening swell segment of inverter yield voltage and electromagnetic obstruction impacts.

The proposed topologies have a secluded structure and can profit the upsides of the arrangement staggered inverters. The basic exchanging strategy is utilized in this examination. Likewise, to create all voltage levels at the yield (even and odd), another calculation for the assurance of the size of the separated dc voltage sources is proposed. At last, the misfortune computation is done, and the execution of the proposed topologies is confirmed by recreation aftereffects of single-stage 25-and 17-level inverters [10].

Majority of industrial drives use ac induction motor because these motors are rugged, reliable, and relatively inexpensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable frequency supply voltage. But numerous applications require variable speed activities. Verifiably, mechanical rigging frameworks were utilized to acquire variable speed. As of late, control hardware and control frameworks have developed to enable these segments to be utilized for engine control instead of mechanical apparatuses. Present day drive types are the Induction engine drives with voltage source inverters. Likewise the voltage waveforms of customary two dimension inverter bolstered Induction engine demonstrates that the voltage over the engine contains the required "crucial" sinusoidal segments, as well as beats of voltage i.e. "swell "voltage. The ongoing headway in power gadgets has started to enhance the dimension of inverter rather expanding the measure of channel. The aggregate symphonious mutilation of the established inverter is high. The execution of the staggered inverter is superior to established inverter. As it were the aggregate symphonious contortion for staggered inverter is low [11-13].

II. Proposed Switched Capacitor Topology

Figure.1. demonstrates the proposed Switched capacitor unit. This topology is yield from arrangement blend of a few essential units. In this figure, the switches Si (i=1, 2, n) interface the capacitors in arrangement, and the switches Pi associate the capacitors in parallel with the dc voltage sources. To create zero and negative voltage levels, a H-bridge has been utilized at the yield. The blocked voltage by each switch in Figure.1. is Vdc.
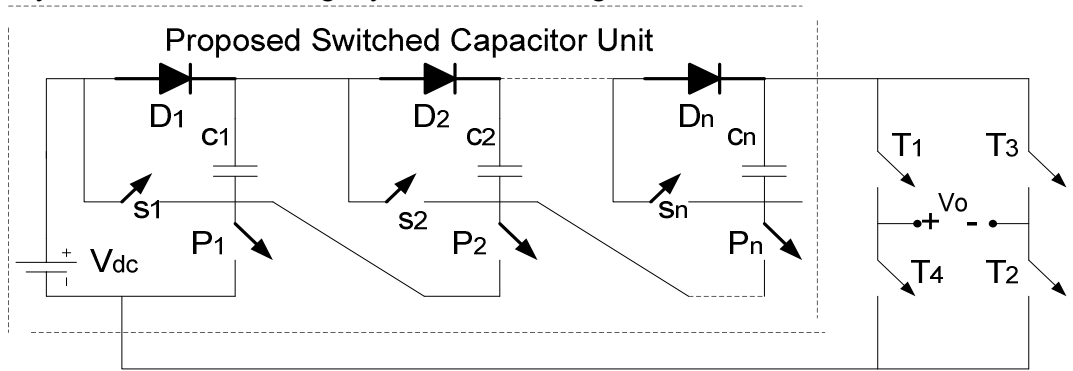

Figure 1. Proposed switched capacitor unit.

In this way, the proposed switched capacitor unit is additionally appropriate for a high recurrence application that isn't the point of this paper. The other favorable position of the proposed topology is the boosting capacity of the information dc voltage without utilizing any transformer. This component decreases the size and cost of the framework and builds its effectiveness. The most extreme quantities of yield voltage levels (Nstep), required protected door bipolar transistors (IGBTs) (NIGBT), and diodes (Ndiode) for the proposed topology appeared in figure 1. are determined by the accompanying conditions, separately,

$$N_{step} = 2n + 3$$

(1)

$$N_{iGBT} = 2n + 4$$

(2)

$$N_{diode} = n$$

(3)

Where n is the number of capacitors. The maximum output voltage that can be produced (Vomax) is equal to

$$V_{o,max} = (n + 1)V_{dc}$$

(4)

So as to decrease the capacitor voltage drop amid the arrangement association, the Pulse width-modulation switching patter example can be utilized between the it h and (i+1)th back to back voltage levels (i=0, 1, 2, n), which, thusly, will build the misfortunes. Then again, more capacitors are expected to deliver more dimensions at the yield. More prominent number of arrangement capacitors expands their voltage drop. In this manner, producing alluring voltage waveform without utilizing of separating components will be troublesome and requires increasingly complex exchanging plans. To deliver more noteworthy number of voltage levels at the yield and diminish the capacitor voltage drop, a few units appeared in Figure.1. can be utilized in arrangement. In this condition, the primary unit, the second unit, and the kth unit have n1, n2, and nk capacitors and dc voltage sources with extents ofV1, V2, and Vk, individually.
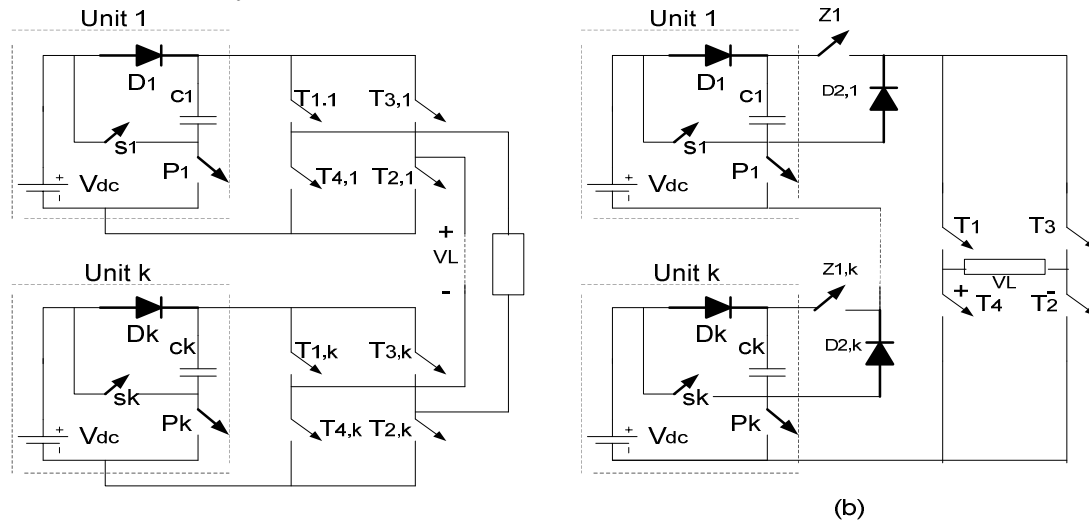

Figure 2. (a) First proposed topology. (b) Second proposed topology.

The general form of the equations that show the number of voltage levels and the number of IGBTs can be expressed as follows:

$$N_{step} = a \left[\prod_{j=1}^{k} (bn_j + c) \right] + d$$

(5)

$$N_{IGBT} = 2 \left[\sum_{j=1}^{k} n_j \right] + ek + f$$

(6)

Where a, b, c, d, e, and fare the integer numbers that depend on the unit connection order. In order to produce the maximum number of voltage levels at the output with using a specified number of IGBTs, (6) can be rewritten as follows:

$$N_{IGBT} = 2(n_1 + n_2 + \cdots + n_k) + ek + f = cte$$

(7)

$$n_1 + n_2 + \cdots + n_k = \frac{N_{IGBT} - ek - 1}{2n + e} = cte$$

(8)

Considering (5) and (8), the number of voltage levels in (5) will be maximum when the following condition is satisfied

$$n_1 = n_2 = \cdots = n_k = n$$

(9)

From (8)–(10), Nstep is obtained as follows

$$N_{step} = a(bn + c)\frac{N_{IGBT} - 1}{2n + e} + d$$

(10)

Equation (10) will be maximum when nets its minimum value. Thus, the proposed topologies produce the maximum number of voltage levels at the output form=1. This result is independent of the units' connection order. The proposed topologies have been presented in the next sections with considering n=1.

A. First Proposed Topology

Figure.2.(a) demonstrates the first proposed topology. In this topology, the switched capacitor units have been associated in arrangement by utilizing H-bridge. Every unit can just create positive voltage levels. The H-bridge produces zero and negative voltage levels. There are a ton of approaches to decide the size of the dc voltage sources. A portion of these calculations are not ready to create all voltage levels at the yield, and some of them deliver dreary voltage levels. So as to keep the referenced issues and deliver the greatest number of voltage levels, the greatness of the dc voltage sources in the jth unit can be as per the following:

$$V_j = (5^{j-1})V_1$$

(11)

Voltage and current evaluations of the switches in a staggered inverter assume essential jobs in the aggregate expense of the inverter. In all topologies, the flows of all changes are equivalent to the evaluated current of the heap. This is, notwithstanding, not the situation for the voltage. Consequently, there is a requirement for a foundation to assess the staggered inverter from the perspective of blocked voltage by power switches and the aggregate expense of framework. This rule is inscribed as "standing voltage". The standing voltage is equivalent to the whole of every blocked voltage by power switches in a converter. The standing voltage of the changes is equivalent to the entirety of the blocked voltages by switches S and P and the H-bridge switches for all units.

B. Second Proposed Topology

Figure.2.(b) demonstrates the second proposed topology. In this topology, every unit is skirted when the switch Pj and the diode D2,j are on and the turn Zj is off. At the point when the switch Zj is on, the diodeD2, j ends up turn around one-sided. In this way, the diode D2,j keeps the retrogressive current streaming amid the unit bypassing when an inductive load is utilized at the yield. As such, the second proposed topology can create the alluring voltage waveforms for resistive burdens. Then again, by supplanting the diode D2,j with a power

electronic switch, the second proposed topology can be utilized for resistive-inductive burdens. The greatness of the dc voltage sources and the quantity of voltage levels can be determined as follows:

$$V_j = (3^{j-1})V_1$$

(12)

The number of voltage levels (Nstep), the number of required IGBTs (NIGBT), the number of diodes (Ndiode), the maximum output voltage (Vo, max), the standing voltage of the switches (Vst and), the number of dc voltage sources (Ndc), and the variety of the dc voltage source magnitude (Nvariety) can b calculated for the first and second proposed topologies, as shown in Table I.

III. Comparison of the Proposed Topology Switch other Conventional Topologies

In this section, the first proposed topology has been compared with three main topologies of multilevel inverters, namely, the diode-clamped multilevel one, capacitor.

TABLE I
CALCULATION OF DIFFERENT PARAMETERS OF THE PROPOSED TOPOLOGIES

Parameter	Proposed Topology	
	First	Second
N_{step}	5^k	$(2 \times 3^k) - 1$
N_{IGBT}	$6k$	$3k + 4$
N_{diode}	k	$2k$
$V_{o,max}$	$2\sum_{j=1}^{k} V_j$	$2\sum_{j=1}^{k} V_j$
V_{stand}	$10(1+5+\cdots+5^{k-1})V_1 = 5\left(\dfrac{5^k-1}{2}\right)V_1$	$11(1+3+\cdots+3^{k-1})V_1 = 11\left(\dfrac{3^k-1}{2}\right)V_1$
N_{dc}	k	k
$N_{variety}$	k	k

TABLE II
Comparison of the First Proposed Topology with the Topologies Presented In [9]

Topology	N step	N switch	N diode	N capacitor	N dc
First Topology	15	12	2	2	2
DCM	13	24	132	12	1
CCM	13	24	0	66	1
CMM	13	24	0	6	1
CBCSM	13	10	12	6	1
SCBM	13	11	3	2	1
HSSCM	13	21	4	5	3

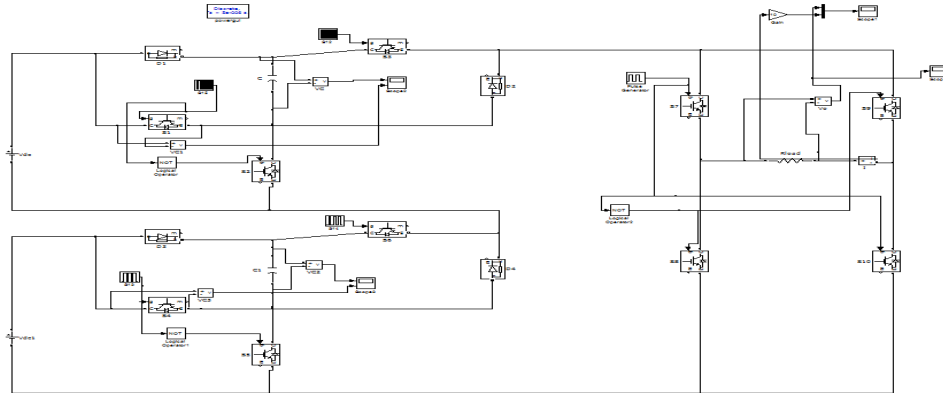## V. Matlab/Simulink Results

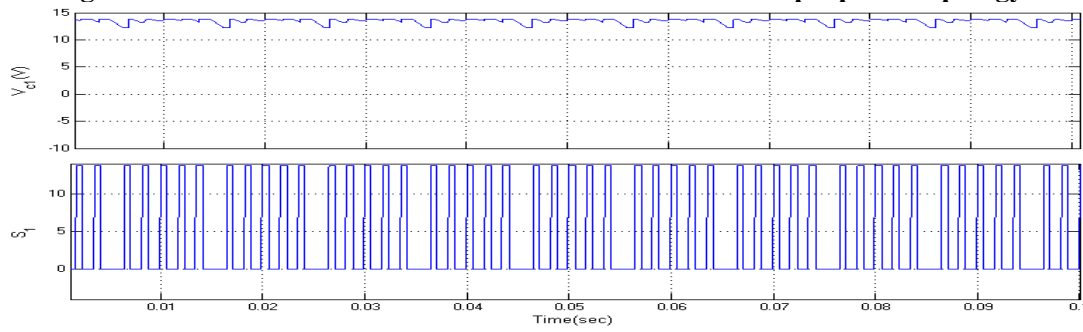**Figure.3.Matlab/Simulink model of 17-level inverter based proposed topology.**

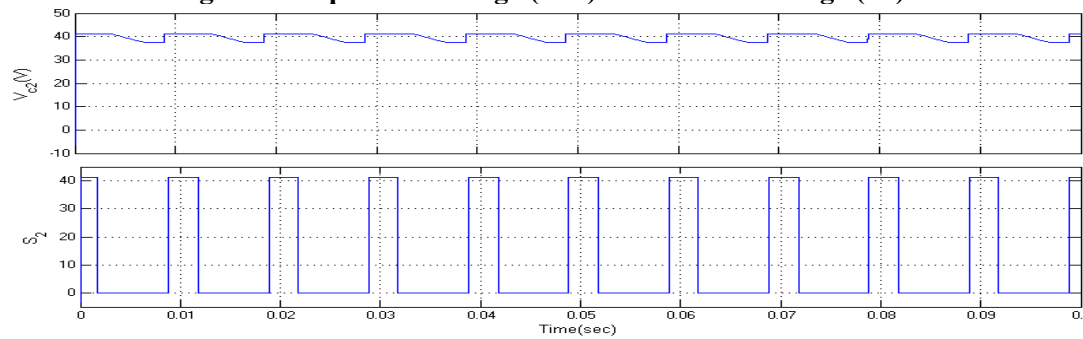**Figure 4. Capacitor Voltage (Vc1) and Switch Voltage (S1).**

Figure 5. capacitor Voltage (Vc2) and switch Voltage (S2).
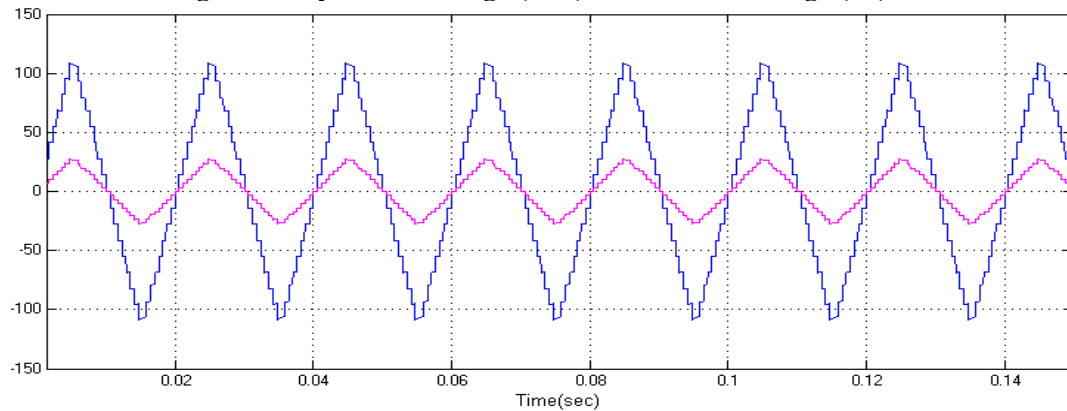
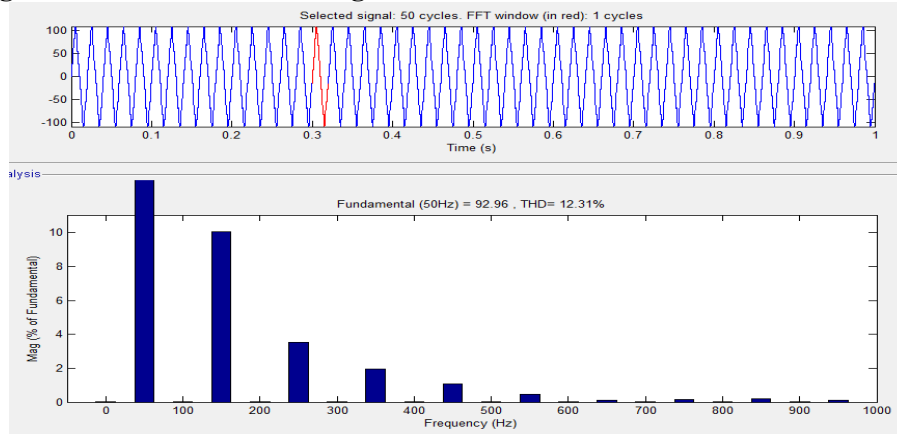**Figure 6. Simulated load voltage and current waveforms for 17-level inverter**.

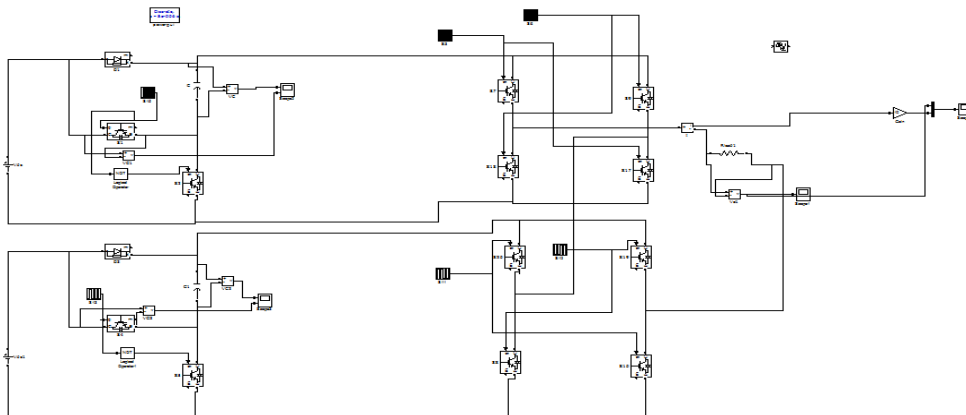**Figure 7.total harmonic distractions for 17 Level inverter.**

Figure 8.Matlab/Simulink model of 25-level inverter based proposed topology.
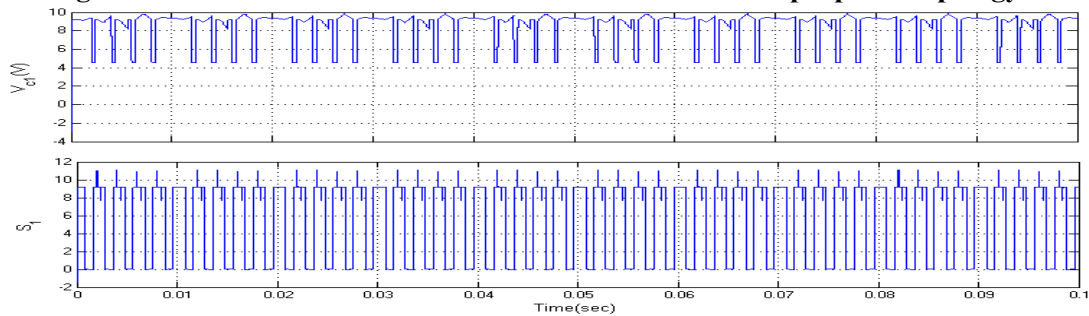

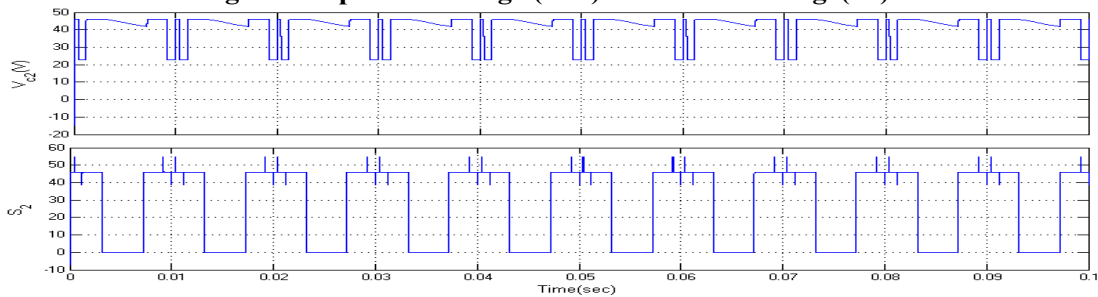**Figure 9.capacitor voltage (Vc1) and switch voltage(S1).**

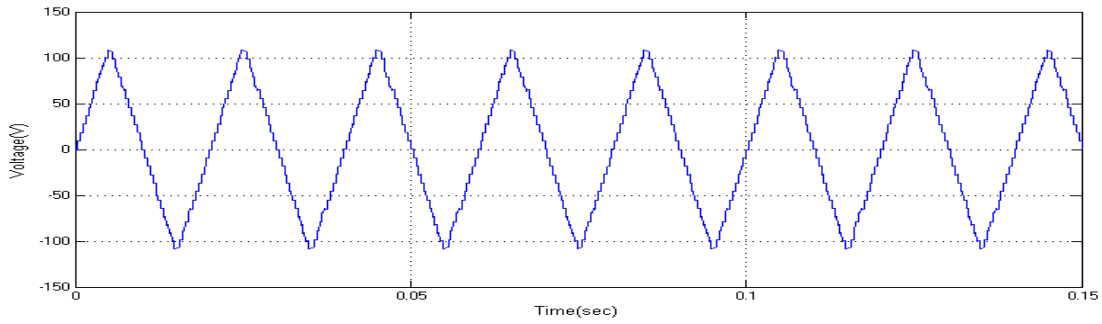**Figure 10.capacitor voltage (Vc2) and switch voltage (S2).**

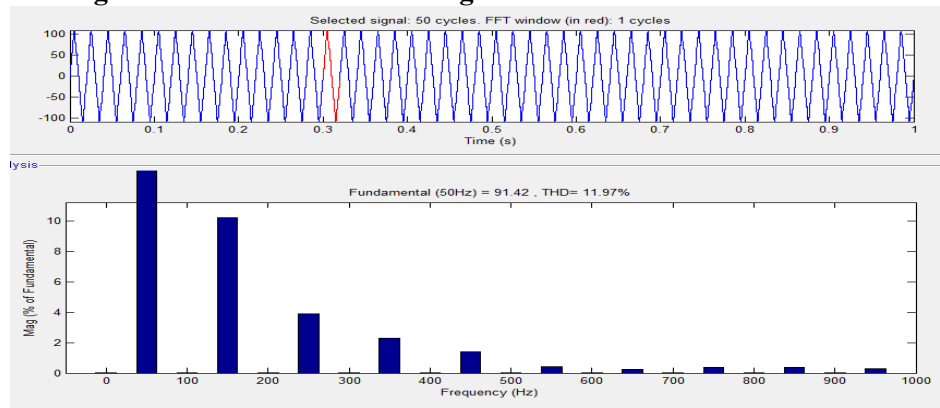**Figure 11. Simulated load voltage waveforms for 25-level inverter**.

Figure 12.total harmonic distractions for 25 Level inverter.
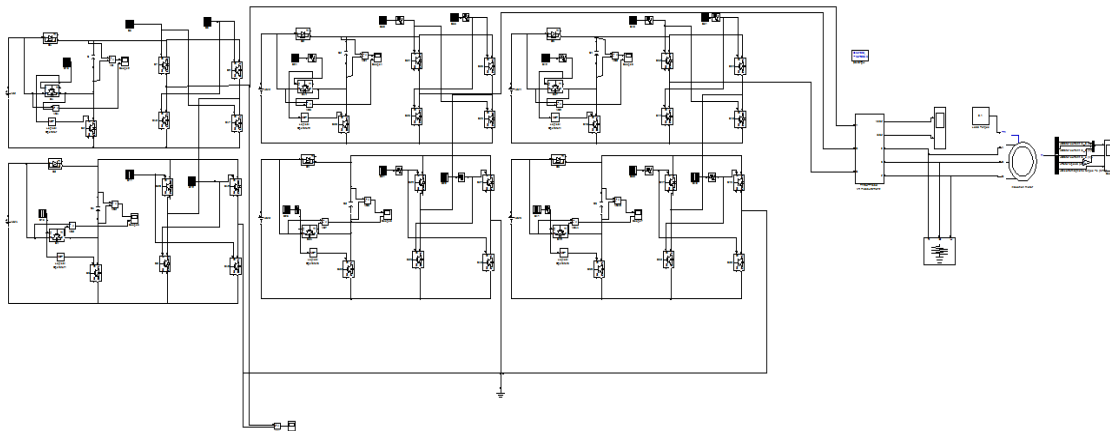

Figure 13.Matlab/Simulink model of three phase 25-level inverter based proposed topology with induction motor.
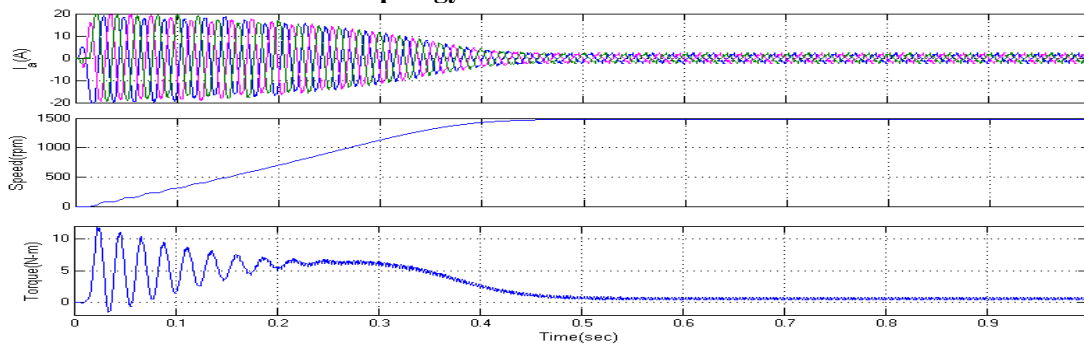

Figure 14. Stator Currents, Speed, Electromagnetic Torque.

VI. Conclusion

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. The proposed topologies reduce the number of switches and isolated dc voltage sources, the variety of the dc voltage source values, and size and cost of the system in comparison with conventional series topologies. The first proposed topology produces a 25-level voltage for all load power factors by using 12 IGBTs, 2 diodes, and 2 isolated dc voltage sources. It is also observed that the proposed topology decreased the number of required power electronic switches compared to a cascaded H-bridge inverter to obtain the same 17 and 25 level output voltage with lower THD. The multilevel inverter fed induction motor system has been successfully simulated and the results of voltage waveforms, current waveforms, motor speed, electromagnetic torque and frequency spectrum for the output were obtained. The inverter system can be used for industries where the adjustable speed drives are required.

References

[1]. K. Bandara, T. Sweet, and J. Ekanayake, "Photovoltaic applications for off-grid electrification using novel multi-level inverter technology with energy storage," Renew. Energy, vol. 37, no. 1, pp. 82–88, Jan. 2012.

[2]. J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energybalance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs,"IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 98–111, Jan. 2013.

[3]. N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system, "IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[4]. A. K. Pandam and Y. Suresh, "Performance of cascaded multilevel inverter by employing single and three-phase transformers, "IET Power Electron., vol. 5, no. 9, pp. 1694–1705, Nov. 2012.

[5]. Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/ parallel conversion with inductive load,"IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878–887, Feb. 2012.

[6]. P. Roshankumar, P. P. Rajeevan, K. K.Mathew, J. I. Gopakumar, and L. G. Leon, "A five-level inverter topology with single dc supply by cascading a flying capacitor inverter and an H-bridge,"IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3505–3512, Aug. 2012.

[7]. A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation,"IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1517–1526, Jun. 2010.

[8]. Y. Ounejjar, K. A. Haddad, and L. A. Gregoire, "Packed U-cells multilevel converter topology: Theoretical study and experimental validation,"IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1294–1306, Apr. 2011.

[9]. S. Ding, M. Cheng, Z. Wang, K. T. Chau1, Y. Wang, and W. Wang, "A hybrid-source switched-capacitor multilevel converter for electric vehicles," in Proc. ICEMS, Incheon, South Korea, 2010, pp. 288–292.

[10]. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters,"IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[11]. M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters,"IEEE Trans. Power Electron., vol. 28, no. 2, pp. 625–636, Feb. 2013.

[12]. K. N. V. Prasad, G. R. Kumar, T. V. Kiran, and G. S. Narayana, "Comparison of different topologies of cascaded H-bridge multilevel inverter," in Proc. ICCCI, Odisha, India, 2013, pp. 1 6.