DESIGN OF LOW POWER HIGH SPEED VEDIC MULTIPLIER USING REVERSIBLE LOGIC

Mrs.S.Aruna Kumari
Assistant professor, Department of ECE,
Baba Institute of Technology & Sciences, Visakhapatnam,
Email id: aruna0454@gmail.com.

Mrs.B V R Gowri
Assistant professor, Department of ECE,
Baba Institute of Technology & Sciences, Visakhapatnam,
Email id: gowri.bobbili@bitsvizag.com.

ABSTRACT- A Simple digital vedic multiplier architecture is based on the urdhva Tryakbhyam sutra is presented. This paper proposes the design of high speed multiplier. This sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In that multiply accumulate operation plays a vital role. In this paper we proposed two techniques to improve processor speed based on vedic mathematics. In Vedic mathematics among 16 sutras,2 sutras are applicable for multiplication. In this paper, comparison of conventional and Vedic multiplier can be performed. This project presents a technique to develop an Vedic multiplier for higher order bits to increase the processor speed.

I. INTRODUCTION

Vedic Mathematics is a standout amongst the most old strategies utilized by the Aryans so as to perform numerical counts [2]. This comprises of calculations that can come down expansive number juggling activities to straightforward personality estimations. The above said advantage originates from the way that Vedic science approach is entirely unexpected and considered near the manner in which a human personality works. The endeavors put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to acquaint Vedic Mathematics with the normal people and in addition streamline Vedic Algorithms into 16 classifications [1] or Sutras should be recognized and acknowledged. The Urdhva Tiryakbhayam is one such duplication calculation which is outstanding for its proficiency in lessening the computations included. With the progression in the VLSI innovation, there is a regularly expanding extinguish for compact and inserted Digital Signal Processing (DSP) frameworks. DSP is ubiquitous in pretty much every designing control. Quicker increases and augmentations are the request of the day. Duplication is the most essential and every now and again utilized tasks in a CPU. Duplication is a task of scaling one number by another. Augmentation tasks additionally frame the reason for other complex activities, for example, convolution, Discrete Fourier Transform, Fast Fourier Transforms, and so forth. With regularly expanding requirement for quicker clock recurrence it winds up basic to have quicker number juggling unit. Hence, DSP engineers are continually searching for new calculations and equipment to actualize them. Vedic science can be appropriately utilized here to perform augmentation.

Another essential region which any DSP build needs to think is the power dissemination, the first being velocity. There is dependably a tradeoff between the power disseminated and speed of activity. The reversible calculation is one such field that guarantees zero power dispersal. Along these lines amid the structure of any reversible circuit the postponement is the main criteria that must be dealt with. In [12] a reversible Urdhva Tiryakbhayam Multiplier had been proposed. This paper is an augmentation of the past work which endeavors to advance the circuit proposed in [12]. The paper is sorted out as pursues: The segment II gives the nuts and bolts of reversible rationale alongside the writing audit. Area III clarifies the Urdhva Tiryakbhayam calculation. The segment IV portrays the alterations of the past structure so as to develop the enhanced plan. Area V contrasts the proposed plan and the other non Vedic multipliers and additionally the past Vedic multiplier

structure and makes a determination guaranteeing the adaptability of Reversible Urdhva Tiryakbhayam multiplier.

II. LITERATURE SURVEY

A. Literature Survey and Significance of reversible logic

Customary combinational rationale circuits are known to dissipate warm for all of data that is lost. This is additionally apparent from the second law of thermodynamics which expresses that any irreversible procedure prompts loss of vitality. Landauer [3] demonstrated that any entryway that is irreversible, essentially disseminates vitality, and each irreversible piece produces k*T ln2 joules of warmth where k is Boltzmann's steady (1.38 x 10-23 joules/Kelvin) and T is temperature in Kelvin. Bringing down the edge voltage and the board of the power supply are broadly connected practices to diminish the vitality utilization in any legitimate task [23]. Anyway these advancements of bringing down the vitality utilization will hit an obstruction of kT [24]. So as to lighten this, procedures, for example, lessening the temperature of PC and developing a thermodynamically reversible PC can be utilized [25].

Blunt [25] broke down that the second alternative was a superior decision. At the point when the temperature of the framework decreases to supreme zero, the vitality diminishes two requests of greatness however utilizing reversible processing there can be further more decrease that matches with the hypothetical esteem. The cardinal element of reversible processing is that electric charge on the capacity cell comprising of transistors isn't allowed to stream away amid transistor exchanging [26]. This can be reused through reversible figuring and consequently diminish vitality scattering. Bennett in 1973 [2] demonstrated that an irreversible PC can generally be made reversible. Reversible rationale circuits normally deal with warming since in a reversible rationale each info vector can be extraordinarily recouped from its yield vectors and hence no data is lost.

B. Reversible Logic Gates

A Reversible Logic door is a n-input n-yield rationale work in which there is a balanced correspondence between the information sources and the yields. This not just decides the yields from the information sources yet in addition the data sources can be extraordinarily recouped from the yields. In light of this bijective mapping the yield vectors are simply changes of the info vectors.

A portion of the fundamental reversible rationale entryways in the writing those are valuable in structuring the Reversible Urdhva Tiryakbhayam Multiplier are the Feynman [5] Gate—the main 2x2 door, that is utilized for fan-out purposes and additionally to supplement. It has a quantum cost of one. Peres [6] Gate—a 3x3 entryway that is utilized to deliver AND activity and in addition EX-OR task. It has a quantum cost of four. New Fault Tolerant door (NFT) – is likewise a 3x3 entryway with a quantum cost five. HNG door which is a 4x4 entryway that can be successfully utilized as a full snake and gives least quantum cost execution. It has a quantum cost of six. BVPPG [11] is a 5x5 door with a quantum cost of ten. All the referenced doors are appeared in the figure 1.

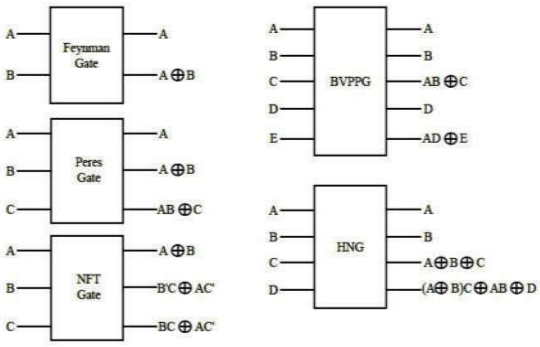

FIGURE 1: REVERSIBLE LOGIC GATES

C. Optimization parameters for reversible logic circuits

The essential parameters [14] which assume a noteworthy job in the plan of a streamlined reversible rationale circuit are as recorded:

•Constants (CI): This alludes to the quantity of sources of info that are to be kept up consistent at either 0 or 1 so as to incorporate the given sensible capacity.
•Garbage (GO): This alludes to the quantity of yields which are not utilized in the blend of a given capacity. These are extremely basic, without which reversibility can't be accomplished.
•Gate check (NG): The quantity of reversible doors used to understand the capacity.
•Flexibility: This alludes to the all inclusiveness of a reversible rationale entryway in acknowledging more capacities.
•Quantum cost (QC): This alludes to the expense of the circuit as far as the expense of a crude door. It is determined knowing the quantity of crude reversible rationale entryways (1x1 or 2x2) required to understand the circuit
•Gate levels: This alludes to the quantity of levels in the circuit which are required to understand the given rationale capacities.
•Total Reversible Logic Implementation Cost (TRLIC) [12]: Let, in a reversible rationale circuit

III. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tryakbhyam (UT) is a multiplier dependent on Vedic numerical calculations deviced by old Indian Vedic mathematicians. Urdhva Tryakbhyam sutra can be connected to all instances of augmentations viz. Paired, Hex and furthermore Decimals. It depends on the idea that age of every single halfway item should be possible and after that simultaneous expansion of these incomplete items is performed. The parallelism in age of fractional items and their summation is gotten utilizing Urdhva Tryakbhyam. In contrast to different multipliers with the expansion in the quantity of bits of multiplicand as well as multiplier the time delay in calculation of the item does not increment proportionately. Due to this reality the season of calculation is autonomous of clock recurrence of the processor. Consequently one can constrain the clock recurrence to a lower esteem. Likewise, since processors utilizing lower clock recurrence disperse bring down vitality; it is practical as far as power factor to utilize low recurrence processors utilizing quick calculations like the previously mentioned. The Multiplier dependent on this sutra has the favourable position that as the quantity of bits expands entryway postponement and territory increments at an ease back pace when contrasted with other customary multipliers. scaled up by improving every individual unit as far as quantum cost, refuse yields and so forth

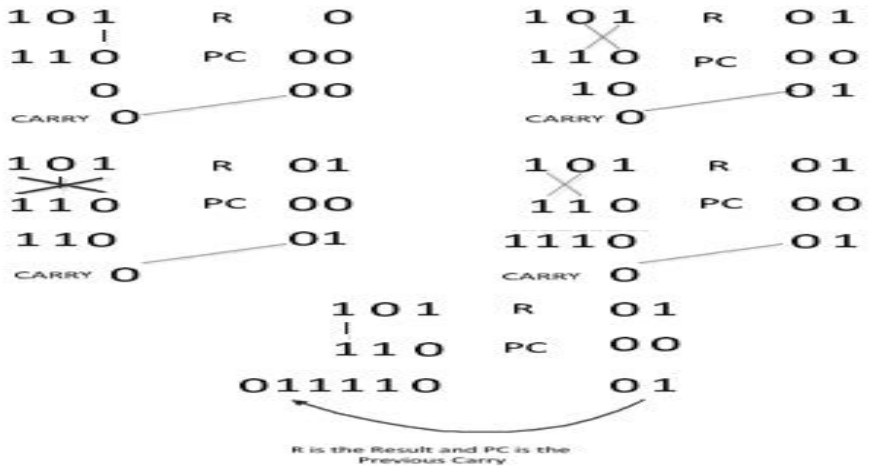

FIGURE 2: URDHVA TIRYAKBHAYAM PROCEDURE FOR MULTIPLICATION

1.We will take the right-hand digits and duplicate them together. This will give us LSB digit of the appropriate response.

2.Multiply LSB digit of the best number constantly bit of the base number and the LSB of the base number continuously bit of the best number. When we have those qualities, include them together.

3.Multiply the LSB digit of base number with the MSB digit of the best one, LSB digit of best number with the MSB digit of base and after that duplicate the second piece of both, and afterward include them all together.

4.This advance is like the second step, simply move one place to one side. We will duplicate the second digit of one number by the MSB of the other number.

5.Finally, just duplicate the LSB of the two numbers together to get the last item.

IV. OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The regular rationale structure execution of a 2x2 Urdhva Tiryakbhayam multiplier utilizing the irreversible rationale doors [8] is an appeared in the Figure 3. In [12] the four articulations for the yield bits are gotten from this figure and is utilized to acquire the reversible usage as appeared in Figure 4. The circuit utilizes five Peres doors and one Feynman entryway. This plan has an aggregate quantum cost of 21, number of refuse yields as 11 and number of steady information sources 4. The entryway check is 6. This structure does not mull over the fan outs. The general execution of the UT multiplier is scaled up by enhancing every individual unit regarding quantum cost, rubbish yields and so forth.

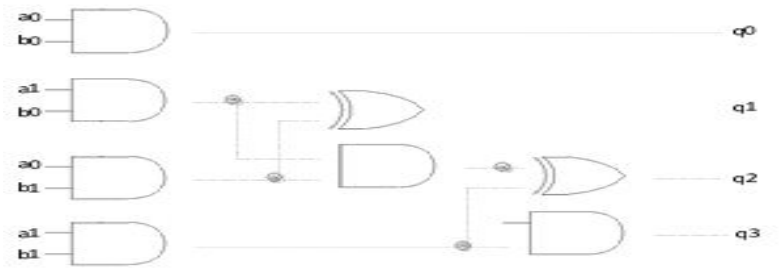

FIGURE 3: CONVENTIONAL 2X2 URDHVA TIRYAKBHAYAM MULTIPLIER

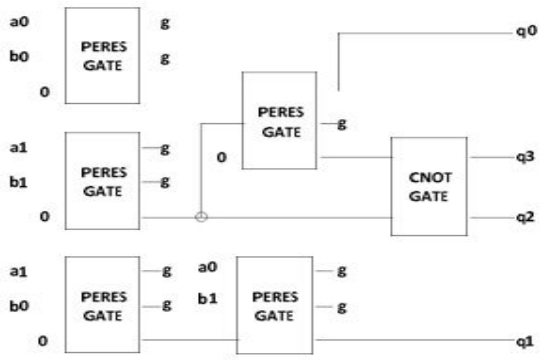

FIGURE 4: REVERSIBLE 2X2 UT MULTIPLIER IN [12]

A. Improved 2x2 Urdhva Tiryakbhayam multiplier

The structure articulations can be legitimately adjusted in order to enhance the plan. The new structure makes utilization of one BVPPG, three Peres entryways and a solitary Feynman door. The plan additionally considers the fan outs. One of the significant plan limitations of reversible rationale is the fan out, other being circles not allowed. This implies the reversible rationale circuit with various quantities of same data sources isn't prudent. One way out is to utilize a different fan out generator or to fabricate a circuit that inalienably deals with fan outs utilizing the reversible rationale entryways utilized in the structure. This structure has a quantum cost of 23, number of refuse yields as 5, number of doors 5 and the quantity of steady sources of info is 5.

The second structure likewise considers the fan out utilizing BVPPG, three Peres doors and one NFT entryway as appeared in the figure 5.

The quantum cost of the circuit is 24; number of waste yields as 4, number of entryways 5 and the quantity of steady sources of info is 5. I1, I2, I3 (Fig 5 and 6) and I4 (Fig 6) are the transitional yields that are utilized for fan-out purposes

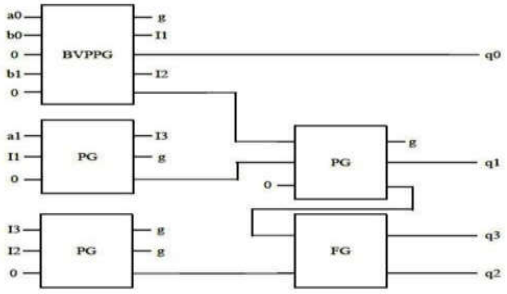

FIGURE 5: Modifed Design1

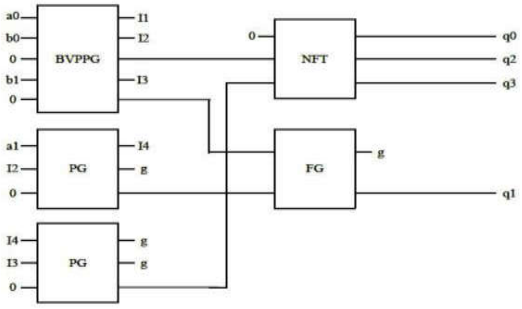

FIGURE 6: Modified Design 2

B. Design of 4x4 Urdhva Tiryakbhayam multiplier

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier configuration exudes from the 2X2 multiplier. The square graph of the 4X4 Vedic Multiplier is exhibited in the figure 6. It comprises of four 2X2 multipliers every one of which acquires four bits as sources of info; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the yield of the primary 2X2 multiplier are captured as the least two bits of the last consequence of duplication. Two zeros are connected with the upper two bits and given as contribution to the four piece swell convey snake. The other four info bits for the swell convey viper are acquired from the second 2X2 multiplier. In like manner the yields of the third and the terminal 2X2 multipliers are given as contributions to the second four piece swell convey snake. The yields of these four piece swell convey adders are thus 5 bits every which should be summed up. This is finished by a five piece swell convey snake which creates a six piece yield. These six bits shape the upper bits of the last outcome.

C. Modification in the design of ripple carry adder

The plan appeared in [12] comprises of just HNG entryways. The quantity of HNG entryways is 4 if the swell convey viper is utilized in the second stage or five if the swell convey snake is utilized in the last phase of the 4X4 Urdhva Tiryakbhayam Multiplier. the swell convey snake can be changed as under. Since for any swell convey viper the info convey for the primary full snake is zero, this certainly implies the principal snake is a half viper. Along these lines a Peres door can effectively supplant a HNG. This chop down the quantum cost by two for any swell convey snake and the waste yield by one. The Constant information sources and the entryway check stay unaltered.

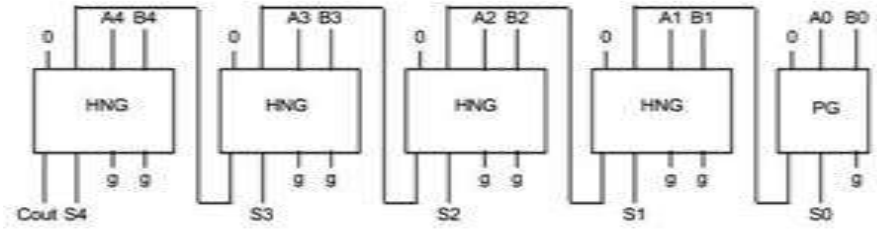

FIGURE 7: PROPOSED MODIFIED 5 BIT RIPPLE CARRY ADDER DESIGN

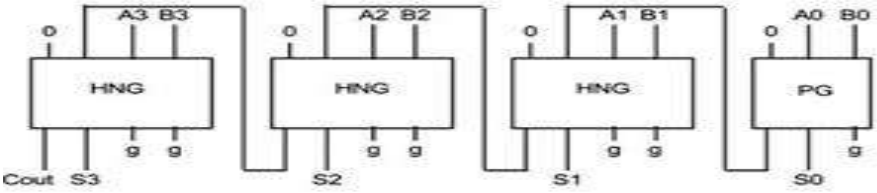

FIGURE 8: PROPOSED MODIFIED 4 BIT RIPPLE CARRY ADDER DESIGN

V. RESULTS AND COMPARISONS

The plan of the reversible 2x2 and 4x4 multipliers is coherently confirmed utilizing XILINX 14.2 and Vivado. The reenactment results are as appeared in figures 10 and 11 separately. Coming up next are the vital structure limitations for any reversible rationale circuits.

1. Reversible rationale circuits ought to have least quantum cost.
2. The plan can be advanced in order to deliver least number of refuse yields.
3. The reversible rationale circuits must utilize minimum number of reversible gates.
4. The reversible logic circuits must use a minimum number of reversible gates.

Since TRLIC is the entirety of all these desig n parameters, it is excellent to have a minimum estimation of TRL IC. The proposed plan of Reversible UT Multiplier is contrasted and upwards of 11 distinctive conspicuous multiplier structure s in the writing as far as Quantum cost, junk yields, number of entryways, number of steady sources of info and furthermore as far as TRLIC values. This likewise incorporates a correlation with our ow n past plan and the improvement is unmistakably clear from the table of Comparison as shown in table 1

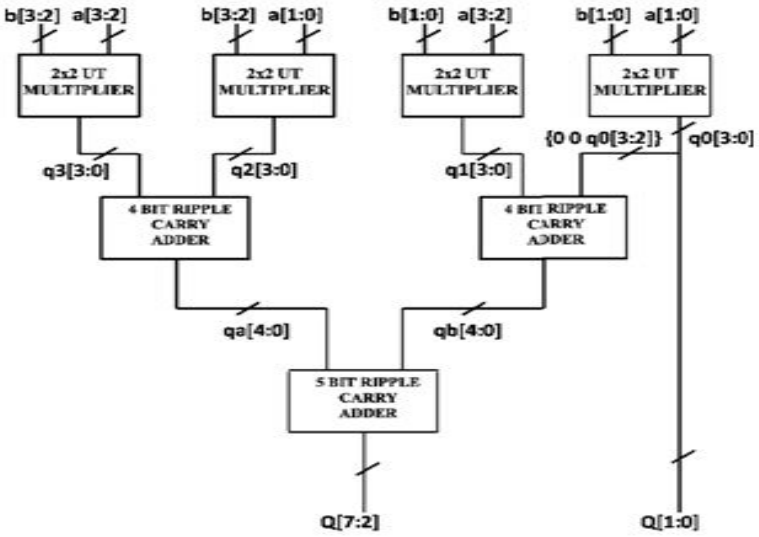

FIGURE 9: BLOCK DIAGRAM OF 4X4 UT MULTIPLIER

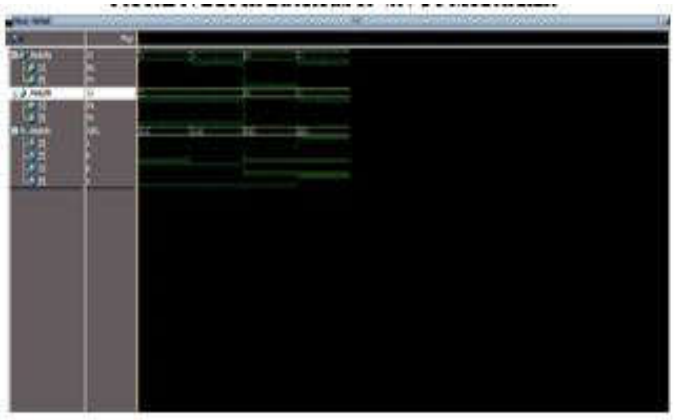

FIGURE 10: SIMULATION RESULTS FOR 2X2 UT MULTIPLIER

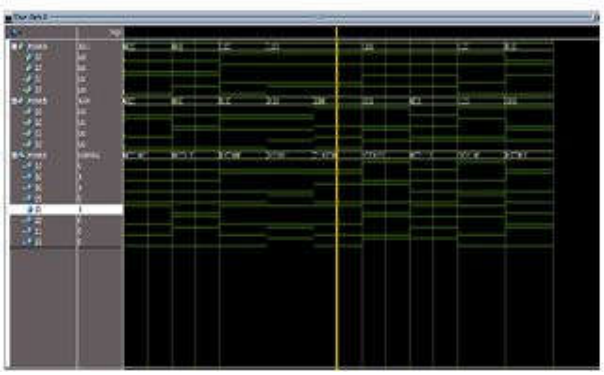

FIGURE 10: SIMULATION RESULTS FOR 4*4 UT MULTIPLIER

The proposed structure of 4x4 UT multiplier as of now referenced deals with the fan-outs moreover. Despite the fact that there is a slight increment in the quantum cost of the 2x2 UT multiplier (it is 23 in proposed plan 1 and 24 in proposed structure 2) when contrasted with past [12] plan (where it was 21), there is a considerable lessening in the num ber of trash yields (from 9 to 5 and 4 individually in structures 1 and 2) and the entryway tally esteems (from 6 to 5 in both the plans). Additionally there is a decrease in the quantum cost of all the swell convey adders by 2 due to the basic modifi cation including substitution of first HNG door by a Peres Gate and decrease in waste yield by one because of the sam e reason. Accordingly, regardless of whether the quantum cost has expanded somewhat, the diminishing in the refuse yields and door tally have completely invalidated its impact. The base enhancement in the TRLIC is at 5.86% which is as for [12] and th e most extreme enhancement stand high at 33.6% w.r.t [22]. Als o from the table unmistakably both proposed plans have a base door consider well as least refuse yields when contrasted with every single other multiplier examined here. The quantity of consistent data sources is superior to anything 10 of the 11 plans. Along these lines we c a say that the plan is especially improved when contrasted with others examined here.

CONCLUSION

The focal point of this paper is for the most part to plan a low power fast multiplier which is finished by building the multiplier utilizing reversible rationale entryways. T he method is done in order to yield an enhanced structure when contrasted with those in the writing. The effectiveness of a reversible rationale circuit is portrayed as far as parameters, for example, quantum cost, number of consistent information sources, trash yields and number of entryways used to understand the rationale execution. Lower the estimation of these parameters more proficient is the plan. In [12] parameter called TRLIC had been proposed which is characterized as total of all cost measurements of the given structure. The quantum cost is a parameter that critical ctly mirrors the deferral of the quantum circuit. Likewise lower TRLIC verifiably implies bring down the quantum cost, thus low er is the deferral and the other way around. Other than guzzling the structure measure that fan-out must be produced inside the circuit, th e proposed plans additionally diminish the TRLIC when contrasted with the recently proposed structure. The further streamlining of the circuit as far as the aggregate sensible expenses is under advancement and is taken as future work.