Study on Voltage Unbalance Improvement Using TCSC in Micro grids Using Unidirectional Fault Current Limiters

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Abstract: - This paper proposes a framework to simultaneously optimize the Power Quality (PQ) and Protection Coordination (PC) levels in a DER-enabled microgrid with multiple connection modes. Introduction of DERs in a grid increases the fault currents. Different connection modes for these DERs lead to varying fault levels. Both phenomena jeopardize the PC. A voltage unbalance in the source influences the power equipment by causing a reduction in the power generation capacity of the generator and a decrease in the output of the other facilities in the transmission line. In addition, many flexible ac transmission systems are applied to transmission lines to compensate for and control electric power. A voltage unbalance causes a control error in these systems. We propose the application of a superconducting fault current limiter (SFCL) with thyristor controlled series capacitor (TCSC) to improve the voltage unbalance in a transmission system linked to a Scott transformer. In addition, we analysed the effects of the proposed method using transient simulations. A Solid-State Unidirectional Fault Current Limiter (SSUFCL) is used as an interface between the microgrid as downstream and the utility as upstream networks, which limits the downstream contribution to the upstream fault currents for increasing the PC and PQ margins, while it is disabled in the case of downstream faults to improve the PQ. In this way the complete coordination between upstream and downstream networks will be achieved. To simultaneously optimize the PC and PQ, the time and current settings of the Over Current Relays (OCRs) and the characteristics of the SSUFCL are set. The optimization formulation of the protection coordination problem is extracted. Fuzzy optimization technique is used to make a compromise between PQ and PC after objectives fuzzification. Genetic Algorithm (GA) is used to find the proper characteristics of the SSUFCL as well as the best settings of OCRs.

KeyWords:- DERs, fault current limiter, microgrids, power quality, protection coordination.

I INTRODUCTION

Introduction of Distributed Energy Resources (DERs) in the grid has increased the fault current depending on the type of DERs [1]-[2], the distance of these units from the fault location, connection mode of DERs and the configuration of the grid. Introduction of more DERs, different connection modes that can be applied based on the operator requirements and intermitting nature of some DERs such as solar, lead to varying capacity microgrids where the Protection Coordination (PC) of the system may be lost, since the Coordination Time Interval Constraints (CTICs) cannot be fulfilled. Therefore, integration of DERs to the microgrids needs a close attention and technical modifications [3]-[5].Based on the standards [6], DERs should be disconnected in the case of the main distribution system (upstream network). Faults to reduce the microgrid (downstream network) share from the fault current. Though the PC is held, this will decrease the microgrid reliability due to unnecessary interruptions. In this situation limiting the fault current in the tie section may solve the problem. However, during a fault or starting a large motor load in the downstream network, limiting the upstream fault current leads to PC issues between upstream and downstream Over Current Relays (OCRs) and also PQ degradation due to the voltage reduction for the microgrid sensitive loads. Both problems can be alleviated using a Solid State Unidirectional Fault Current Limiter (SSUFCL) as proposed in this work. In the present paper a framework is proposed to simultaneously maximize the PC level and power quality (voltage sag

mitigation is considered) and therefore, to maximize the benefit gained by installing a SSUFCL in the tie section. In [7], SSUFCLs was used to preserve the PC and/or to improve the PQ of a microgrid. In contrast, co-optimization of PC and PQ levels is proposed in this paper. Here, different connection modes are considered for the microgrid DERs. The options available to optimize the PC and PQ levels are OCRs' time and current settings as well as the SSUFCL characteristics. The objectives are fuzzified and a fuzzy multi objective optimization technique is used to solve the problem. Genetic Algorithm (GA) is used to determine the characteristics of the SSUFCL and the OCRs' settings. In order to minimize the chance of PC failure, the basic solution is to find the best settings for protective devices. However, in this way, the full PC cannot be held. Simultaneous planning of DERs and tuning the protection devices was proposed in [8] and the reliability improvement was demonstrated on a test system. However, the PC might be lost due to the multiple connection modes of DERs. The DERs' penetration level may be also restricted. An adaptive scheme was suggested in [9]. Due to requirements such as a decision unit, adaptive settings of protection devices and a strong communication system, this scheme cannot be applied in all systems. Communication-based protection systems and digital relays were also proposed in [10]-[11].Installation of some devices such as Fault Current Limiters (FCLs) with proper characteristics may solve the problem[12]-[18]. The main idea is to avoid unnecessary power Interruptions to maximize the benefits of the DERs in both grid-connected and standalone modes [12]-[17]. Other than restricting the magnitude of the fault currents, FCLs can limit the variation of the current level in different fault situations.

As the number of DERs increases, one approach is optimal locating and parameter setting of additional FCLs in the connecting section of new DERs [19]-[22].A practical SSUFCL design which was proposed in [23]and was used in [7] is also used here. This SSUFCL is resonant type FCL with a fault direction detecting unit. The FCL acts as a series resonant circuit with very small impedance during the normal conditions. During the fault condition, this device switches to a parallel resonant circuit with relatively large impedance [23].Comparing to the reviewed papers, the contributions of this paper are fourfold:

1) To co-optimize the PC and PQ levels using SSUFCL to maximize the benefits gained by installing this device.
2) To consider different connection modes for DERs.
3) To solve the multi-objective problem using the fuzzy optimization technique.
4) To consider the practical limitations of SSUFCL.

The rest of this paper contains the following discussions. Section II presents the complete formulation for Co-Optimizing the PC and PQ and models the practical limitations of the SSUFCL as the problem constraints. Section III presents the operation and control of a TCSC system. Numerical results are provided in Section IV. The conclusion is drawn in Section V.

II CO-OPTIMIZATION OF PC AND PQ

The basic motivation for installing an FCL between the downstream and main networks is to prevent the fault current exceeding the current rating of the system equipment as the new DERs are presented. Since the main network equipment is not designed to undergo such over-currents, the main network is more vulnerable in such conditions. To address the PC issues of the downstream OCRs invariable capacity microgrids in the case of upstream faults, there are two key solutions. The first solution is to change the relays' setting continuously. Though replacing the OCRs with new relays with an adaptive protection scheme may solve the problem, this increases the complexity and cost of protection.

The second key solution is to reduce the microgrid impact on the relays' setting. Disconnecting all the DERs during faults and utilizing an FCL as the interface between the microgrid and the upstream network are proposed in the literature. While synchronization problems and loss of the DERs' power during the faults limit the application of the first solution, the second solution has been accepted as a common approach which limits the current contribution of all the downstream DERs for different disturbances in the main network. This increases the power quality of microgrid [14]-[15] and covers all the downstream DERs and sensitive loads. The benefits gained by limiting the current contribution of the downstream DERs in the case of upstream disturbances are summarized. These benefits include: Limiting the

fault current to avoid over-current in the main network equipment, protection coordination of the downstream OCR and improving the PQ for sensitive loads of the microgrids. However, during microgrid disturbances, operation of the FCL may cause the loss of PC between the upstream and downstream OCRs and PQ degradation. As an example, voltage sag will be further aggravated by limiting the contribution of the main grid. A SSUFCL has been proposed in the literature [7] to operate as a conventional FCL when a fault occurs in the main grid, and to be disabled it in the case of downstream faults. The fault current is limited only in the case of upstream disturbances, and under such situations, the downstream OCRs should not interrupt the fault current due to the PQ improvement strategy. Therefore, during the upstream disturbances there is possibility of losing selectivity of the protection system (due to low fault current), the downstream OCRs should not issue any trip command. A SSUFCL can solve most of PC and PQ issues in a microgrid with DERs. In the case that fault current level of the microgrid exceeds the permissible range, additional FCLs can be installed in the connected branches of some DERs to reduce the fault current contribution of these DERs and to help SSUFCL complete its duties. A framework is presented here to optimize the SSUFCL parameters as well as the OCRs' setting, to get the full benefits. Minimization of OCRs' operation time and average voltage sag minimization are considered as the objective functions. In V_{cb}, is the voltage of sensitive bus *b*, during fault *f* in connection mode *c*. The number of sensitive buses is given by N_{sb}. The voltage of bus *b*in connection mode *c* during the normal condition is given by V_{cb}. Obj_2 gives the average voltage sag for the sensitive buses

$$Min\ Obj_2 = \sum_{c=1}^{N^c} ND^c \frac{\sum_{b=1}^{N_{sb}} \sum_{f=1}^{N_F} (V_b^c - V_{b,f}^c)}{N_{sb} N_f} \quad (1)$$

In order to solve this multi-objective problem, fuzzy optimization is utilized. In fuzzy sets' domain, a membership function is assigned to each objective. For each value of the objective function, the degree of satisfaction of this objective is specified by this membership function. By contrast, an objective is satisfied or violated in the crisp domain, equivalent to the membership function values of 1 and 0, respectively. Fuzzy sets consider varying values for membership function all between 0 and 1. The rest of this subsection is dedicated to fuzzification of the objectives and a discussion on the SSUFCL characteristics.

A. Membership Function of the PC Objective

In fuzzy domain, the degree of satisfaction of each objective is specified by a value between 0 and 1 (signifying the worst and best possible objective function values). For each objective, it is necessary to find the best and worst values of objective. A single-objective optimization should be conducted to adjust the OCRs' setting and SSUFCL parameters to minimize obj_1 satisfying all the problem constraints. This optimization gives obj_1 min. For the worst value of the objective function, one approach (which is used here) is to estimate an upper bound for the value of objective function. The maximum value of the PC objective function (obj_1 max) is $2*N_f*t_{max}$- N_f*CTI_{min}. Fig. 1 shows the membership function of the PC objective. The degree of satisfaction of the first objective increases monotonically as the value of the PC objective function decreases from obj_1max to obj_1min.

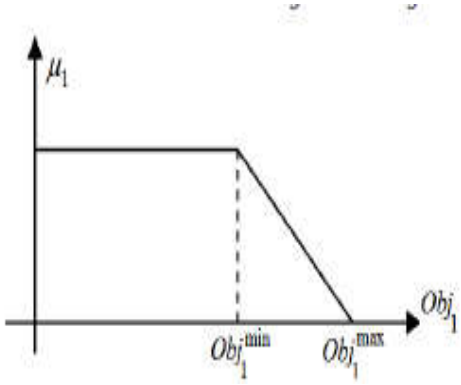

Fig.1: Membership functions of sum of OCRs' operation time.

B. Membership Function of the Voltage Sag Objective

The second objective is to minimize the average voltage sag. Here, obj_2 max would be the average voltage sag without SSUFCL and obj_2min is found using a single-objective optimization. The membership function of the PQ objective is the same as the one presented for PC objective. The relays' setting has no effect on the voltage sag. The SSUFCL parameters affect both obj_1 and obj_2 The

constraints on these parameters are introduced in sub-section *C*.

C. Discussion on the SSUFCL Limitations

The power quality improvement depends widely on the current limiting capability of the SSUFCL and the quality of its one way operation as well as its operation speed. According to [7], in `order to determine the fault direction in a short time,3rd and 5th orders of instantaneous harmonic power passing through the SSUFCL are calculated. The fault direction is then determined based upon their signs. The current limiting capability of a SSUFCL depends on the impedance inserted during the upstream faults. A resonant type solid state FCL is shown in Fig. 2.

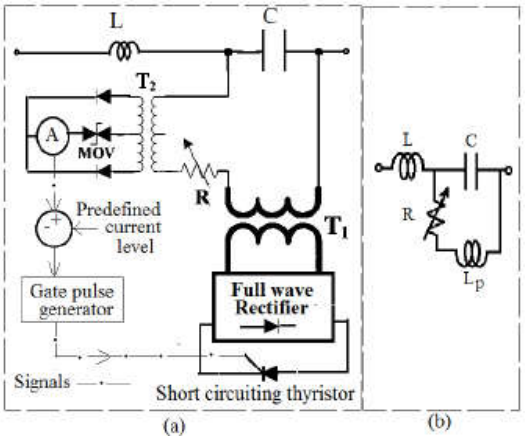

Fig.2: Resonant SSUFCL

As a fault occurs the voltage across the capacitor increases suddenly. As the result, the MOV operates and the gate cathode voltage of the short circuiting thyristor reaches sufficient level to fire the thyristor. In this condition, T2 which is a saturable transformer will be saturated and the inductance viewed from the primary of this transformer falls to a value of a few nanohenries, which does not affect the parallel resonant circuit. To achieve a fast turn on of the thyristor, T1 has a small magnetic core with a very low turn ratio. The variable resistance R models the resistance of the parallel resonant circuit in series with a variable resistance designed for the better adjustment. In such situation the impedance of the SSUFCL is found using (21). After segregation of the real and reactive components (22), the maximum impedance condition can be found.

$$Z_{SSUFCL} = jX + \frac{-jX_C(R+jX_P)}{R+j(X_P-X_C)} \qquad (2)$$

$$Z_P = \frac{RX_P^2}{R^2+(X_P-X_C)^2} - j\frac{(R^2X_C-X_P^2X_C+X_C^2X_P)}{R^2+(X_P-X_C)^2} \qquad (3)$$

$$\omega_0 = \frac{1}{\sqrt{(L+L_S).C}} \qquad (4)$$

$$\omega_0 = \frac{1}{\sqrt{L_P C}}\sqrt{1-\frac{R^2C}{L_P}} = \sqrt{\frac{1}{L_PC}-\frac{R^2}{L_P^2}} \qquad (5)$$

$$C = \frac{L_P}{L_P^2\omega_0^2+R^2} \qquad (6)$$

$$L = \frac{1}{C.\omega_0^2} - L_S \qquad (7)$$

$$t_1.I_P^{max.f}(T_1,R) < I_{th}^{holding} \qquad (8)$$

$$I_{th}^{Latching} < t_1.I_P^{min.f}(T_1,R) \qquad (9)$$

$$I_P^{max.f}(T_1,R) \le min\left\{I_{T_1}^n, I_R^n, \frac{I_{th_1}^n}{t_1}\right\} \qquad (10)$$

$$V_p^{max.f}(T_1,R) \le V_c^n \qquad (11)$$

Among the parameters *L*, *Lp*, *C* and *R*, two parameters (*Lp* and *R*) should be selected and two other parameters are found to satisfy the series and parallel resonant conditions. There are many constraints that should be also satisfied. A large value should be selected for the inductance of the parallel resonant circuit to attenuate the current oscillations and to improve the voltage distortion in the case of SSUFCL operation. To have a larger inductance value, the length of the winding should be increased. This increases the resistance of parallel circuit. Though the resistance of the parallel resonant circuit, smooth the oscillations, the higher value for this resistance reduces the current limiting capability of the SSUFCL. Therefore, the value of *R* should be kept as low as possible. However, this may over-rate the device components. On the other hand, lower values of the inductance require larger values of *C* which other than the higher costs, lead to overcompensation, especially in no-load conditions and higher circulating current. The maximum circulating current determines the current rating of the FCL components such as primary side ratings of T1 and T2. The maximum reverse bias voltage of the thyristor depends on the maximum voltage drop

across the capacitor and the turn ratio of transformer T1. In fault conditions, the capacitor voltage will increase. The voltage rating of the primary side of T1 is equal to the maximum voltage of the capacitor.

The turn ratio of T1 and the value of R should be selected in a way that the thyristor current becomes higher than the latching current as a fault occurs and becomes lower than its holding current after fault clearance. In order to meet the first condition, the circulating current in the minimum fault current should be higher than a predefined value for the safe thyristor turn-on. To meet the second condition, the circulating current in the maximum current after fault clearance should be lower than a predefined value for a safe turn-off. Designing an SSUFCL with lowest cost which can solve the grid PC and PQ problems is beyond the scopes of this paper. Here, it is assumed that there are different options available forT1, each of which with certain turn ratio ($t1$), Lp, internal resistance and current rating. The minimum value that should be considered for R, is the resistance viewed from the primary of T1. The values of L_p and R are selected as the optimization variables. The values of L and C can be found accordingly using the resonant condition.

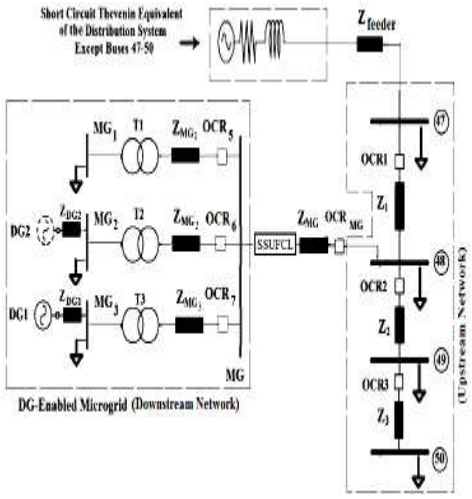

Fig.3: The downstream and upstream systems.

Fig. 3 shows a small microgrid connected to the upstream network which is used as the test system in the case studies. Assuming a system in which the DERs supply a portion of the load of the microgrid, the maximum current passing through the SSUFCL after the fault clearance is associated with the connection mode in which no DER is connected. However, since in this situation the microgrid does not contribute in the fault current, the maximum current is associated with the connection mode in which the DER with lowest production is the only DER connected. However, with a little over-design, the former connection mode is considered. $I_{pmin,f}$ is the minimum current passing through the primary side of T1 in the case of an upstream network fault. There are different fault conditions and the fault current passing through the SSUFCL depends on the place, impedance and type of fault. The minimum current passing through the SSUFCL which is considered as the fault current can be used to find the value of $I_{pmin,f}$. It should be noted that the value of$I_{pmax,cl}$ and $I_{pmin,f}$ depend on L_p $t1$ and R. depend on T1 and R and the network characteristics before installation of SSUFCL.

III OPERATION AND CONTROL OF A TCSC SYSTEM

In Fig. 2, the equivalent impedance X_{TCSC} of TCSC [6], [7] is as follows:

$$X_{TCSC} = \frac{X_C X_{TCR}}{X_C - X_{TCR}} = \frac{X_C X_L}{\frac{X_C}{\pi(2(\pi - \alpha) + \sin 2\alpha)} - X_L} \quad ...(12)$$

Where X_L is the reactance of the fixed reactor, α is firing angle of the thyristor measured from the zero crossing, and X_C is reactance of the fixed capacitor.

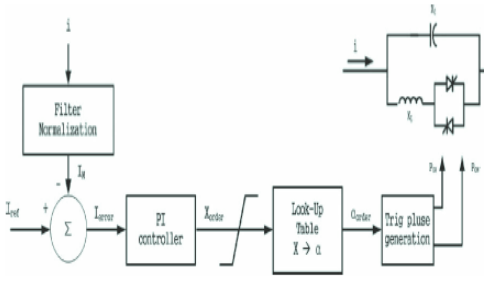

Fig.4: TCSC closed-loop constant current control methodology.

Control of α typically applies open-loop control or closed loop control. Fig. 4 details a schematic of a constant current closed-loop control [8]. In Fig. 3, I_{ref} is desired transmission line current, IM is

actual current, and I_{error} is difference between I_{ref} and IM. In particular, I_{error} is an important quantity in this control loop. A current unbalance can cause serious issues for TCSC control.

IV. SIMULATION RESULTS AND DISCUSSIONS

Different case studies are conducted on the micro grid shown in Fig. 3. The main distribution system is modeled by an equivalent short circuit Thevenin model. The system data is provided.

Table I: System Parameters.

Components	Characteristics
Short circuit model	V_L=12.66 kV, $S_{short\text{-}circuit}$=100 MVA, X/R=5
Z_{feeder}	Over-head Line: R=0.7 Ω, X=2 Ω
Z_1-Z_3	Over-head Line: R=0.5 Ω, X=1.5 Ω
Z_{MG}	Over-head Line: R=0.5 Ω, X=1.5 Ω
Z_{MG1}-Z_{MG3}	Over-head Line: R=0.5 Ω, X=1 Ω
DG1-DG2	300 kVA, R_{DG}=0.08 Ω, X_{DG}=0.07 Ω
T1-T3	Transformer: 12.66/0.4, 1 MVA, Z_T=5%, X_T/ R_T =4
L_{47}-L_{50}	Non-Rotating Loads: S=300 kVA, PF=0.95 lag
L_{MG1}	Non-Rotating Loads: S=150 kVA, PF=0.95 lag
L_{MG2}	Non-Rotating Load: S=150 kVA, PF=0.97 lag
L_{MG3}	Sensitive Non-Rotating Load: S=200 kVA, PF=0.96 lag

In Table I. Different connection modes including no DG, only DG1, and both DGs connected are considered as connection modes 1, 2 and 3, respectively. Tables II shows the primary-backup pairs for these connection modes. For some primary OCRs there is no backup protection. Duration of all the connection modes are the same. For all the OCRs, parameters *A*, *B* and *p*, are 0.3, 0.1 and 2 respectively. The TDS is between 0.05 and 11. The operation time is considered to be between 0.01 and 2 sec respectively. The coordination time interval should be between 0.2 sec and 0.5 sec.

Table. II: Primary Backup pairs.

	Connection Mode 1		Connection Mode 2		Connection Mode 3	
Fault	Pr	Bc	Pr	Bc	Pr	Bc
48	OCR_1	--	OCR_1	--	OCR_1	--
					OCR_{MG}	OCR_6
			OCR_{MG}	OCR_6	OCR_{MG}	OCR_7
49	OCR_2	OCR_1	OCR_2	OCR_1	OCR_2	OCR_1
			OCR_2	OCR_{MG}	OCR_2	OCR_{MG}
50	OCR_3	OCR_2	OCR_3	OCR_2	OCR_3	OCR_2
MG	OCR_{MG}	OCR_1	OCR_{MG}	OCR_1	OCR_{MG}	OCR_1
					OCR_6	--
			OCR_7	--	OCR_7	--
					OCR_5	OCR_{MG}
MG1	OCR_5	OCR_{MG}			OCR_5	OCR_6
			OCR_5	OCR_7	OCR_5	OCR_7
MG2	OCR_6	OCR_{MG}	OCR_6	OCR_{MG}	OCR_6	OCR_{MG}
					OCR_6	OCR_7
MG3	OCR_7	OCR_{MG}	OCR_6	OCR_7	OCR_7	OCR_{MG}
			OCR_7	OCR_{MG}	OCR_7	OCR_6

A protection CT should be used to supply an image of the fault current as reliably as possible to each OCR. For an easier interpretation of the results, the same CTs are applied for all the OCRs. The characteristics of these CTs are as follows: 100/5 A, 15VA, accuracy class 5P and accuracy limit factor (FLP) 30. The maximum fault current level of the system analyzed in the case studies of this paper is less than 2500 A. According to the CT FLP, the maximum permissible primary current (*I*pI), for which the total error in the CT secondary does not exceed the value implied by the CT accuracy class, is 30 times the nominal primary current (I_pI=30*100=3000 A). The value of I_pI is therefore, less than maximum fault current level and thus the maximum combined error would be less than 5% (accuracy class of 5P).

Before engaging in co-optimization of the PC and PQ, two different studies are conducted to find out how a UFCL improve the PQ considering an upstream fault (at bus 49) and another fault in the downstream network (bus MG1). The load connected to bus MG3 is considered as a sensitive load. The voltage at this bus is compared for the case with a bidirectional FCL and a UFCL to the voltage of this bus without FCL (Figs. 5 and 6). The parameters of the FCLs are considered to be the same as those obtained in the previous sub-section. The voltage sag is improved using an SSUFCL in the case of an upstream fault, while a bidirectional FCL degrades the PQ in the case of downstream disturbances. Table VII summarizes the results of this study. As can be seen the maximum PQ is attained using UFCL. The rest of this sub-section is dedicated to co-optimization of PC and PQ.

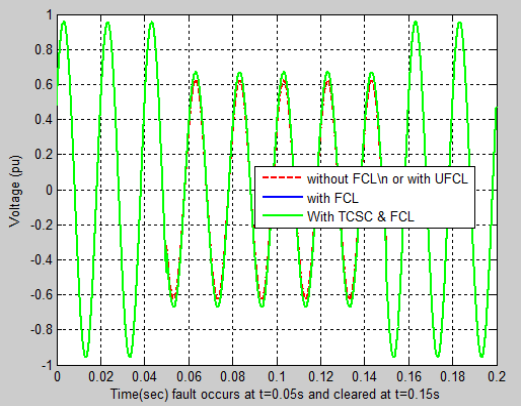

Fig.5: Voltage at bus MG3 during the fault at MG1.

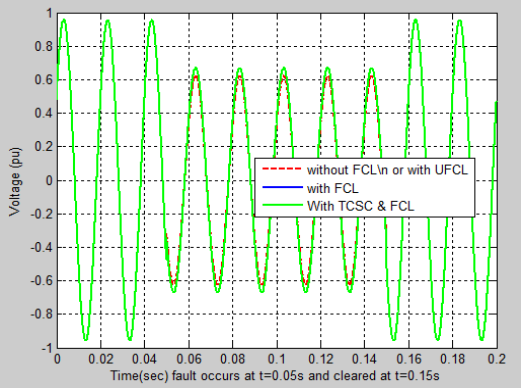

Fig.6: Voltage at bus MG3 during the fault at bus-49.

The results show that as the impedance of SSUFCL increases, the voltage sag in the sensitive buses of the microgrid decreases. The maximum PQ would be obtained for an open circuit SSUFCL. Though it is neither possible nor economical to attain this extreme situation, the average value of voltage sag in such situation can be considered as Obj_2 min.

In this case the values of Obj_2 min and Obj_2 max are 0.17 and 0.41, respectively. The value of PC objective function obtained in sub-section *B* is used as Obj_1min. based on Section III, sub-section *A*, the value of Obj_1max is 26.6 sec. The results of co-optimization of PC and PQ in the micro grid example show that with voltage sag minimization as one of the objectives, the constraints other than CTICs are activated maximum limit of TDS and maximum limit of operation time for some OCRs. As can be seen, applying the proposed framework, a SSUFCL can be used to maximize the PQ and PC levels.

V CONCLUSION

A framework was presented to solve the PC and PQ issues in a microgrid connected to the main distribution system. SSUFCL plus TCSC was used as the interface between the microgrid and the main system. In order to maximize the benefit gained by installing the SSUFCL and TCSC the framework optimizes the OCRs settings as well as the SSUFCL parameters to co-optimize the PC and PQ in the microgrid. The results show that the proposed framework can effectively co-optimize the PC and PQ levels. The physical restrictions of the SSUFCL and TCSC are taken into account. A complete formulation is proposed for PC optimization and is modified carefully to be solved using a heuristic optimization algorithm. The PC is restored in every connection mode in the microgrid after installing the DERs and the unnecessary interruptions are avoided to maximize the system reliability. The voltage sag issue in the sensitive buses of the microgrid in the case of the upstream disturbances is mitigated without engaging into the resynchronization issues.

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