High Voltage Gain Using Bridgeless PFC Modified SEPIC Rectifier

T. R. Premila[1]

[1]*Assistant Professor, Vels Institute of Science, Technology and Advanced Studies*
[1]*premila.se@velsuniv.ac.in*

Abstract

The concept of proposed method is to improve the efficiency at low input using the bridgeless PFC modified SPIEC rectifier. Instead of the input rectifier bridge two semiconductor switches are used in the current flowing path. Due to this switches the conduction losses will reduced and it improve the thermal management. Lower switch voltage stress allows utilizing a MOSFET with lower R_{DS} – on. The proposed method is designed to operate in discontinuous conduction mode (DCM) to achieve near a unity power factor. By using proposed method achieved low total harmonic distortion (THD) of the input current. The DCM operation gives additional advantages such as zero – current turn – on in the power switches and simple control circuitry.

Keywords: *Discontinuous Conduction Mode, Single Ended Primary Inductor Converter.*

1. Introduction

Bridgeless PFC modified SEPIC rectifier fed supply from AC source like electricity board power. Single Ended Primary Inductor Converter is combination of rectifier and converter. SEPIC rectifier is having several advantages such as: step up and step down capability in addition to magnetic coupling that will lead to reduction in input current ripple. Controller circuit of the driver and PIC microcontroller are fed power from power supply. The output of the modular SEPIC converter power supply is fed to the load [2].

2. Existing System

The DCM operation requires a high quality boost inductor since it must switch extremely high peak ripple current and voltage[4]. As a result, a more robust input filter must be employed to suppress the high frequency components of the pulsating input current, which increase the overall weight and cost of the rectifier[5]. In addition, several PFC topologies have an inverting output[3].

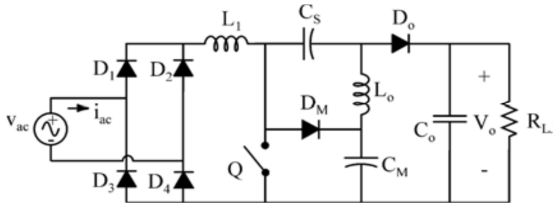

Figure 1.Modified SEPIC Rectifier

Modified SEPIC rectifier of the existing system is having more number of disadvantages like complex circuit, bridge rectifier circuit is used, conduction losses is high and switch voltage stress is high

3. Proposed System

In this paper, a new single phase PFC bridgeless rectifier is operated in discontinuous conduction mode. The DCM operation results in soft turn – on switching and relatively low inrush current. The voltage gain can be extended without extreme duty cycle. The proposed bridgeless rectifier is

coupled magnetic configurations, results in higher overall efficiency and higher power density.The bridgeless configuration will reduce the conduction losses and the multiplier cell (D_1, C_3) and (D_2 , C_3) will increase the gain and reduce the switch voltage stress.The proposed circuit consist of two MOSFET switches (Q_1, Q_2) and two slow diodes (Dp ,Dn).

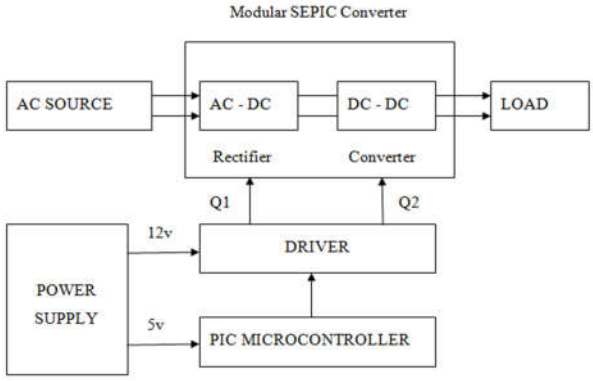

Figure 2. Block Diagram Of Bridgeless PFC Modified SEPIC Rectifier

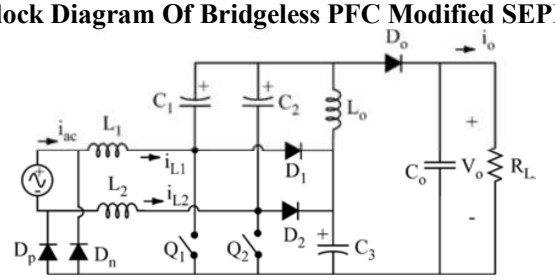

Figure 3. Bridgeless modified SEPIC Rectifier

The advantages of the proposed system having simple circuitry, lower voltage stress in whole operation, conduction losses is reduced and higher efficiency.

4. Mode of Operation

Bridgeless SEPIC PFC rectifier is having two switches Q_1, Q_2 and two diodes are serially connected with inductor in every half cycle of the operation. To shown in the positive and negative half line periods equivalent circuit diagram.

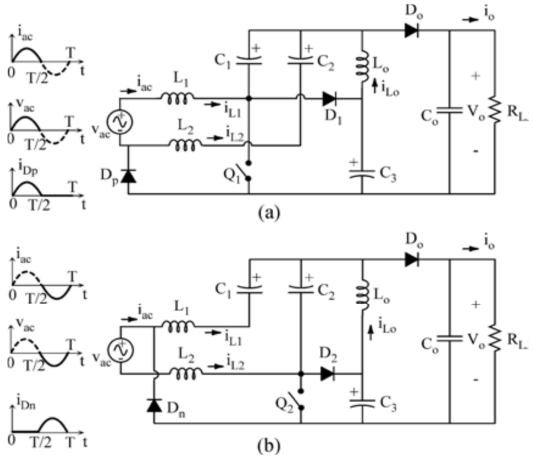

Figure 4. (a) During positive half- line period. (b) During negative half – line period.

4.1. Positive Half –line Mode of Operation

Since the proposed circuit consist of two symmetrical configurations as illustrated in fig.4, the circuit is analysed for the positive half line cycle configuration shown infig.4aAssuming that the three inductors are operating in DCM, then the circuit operation during one switching period T_s in a positive half – line period can be divided into three distinct operating modes as shown in fig 5 (a) – (c), and it can be described as follows

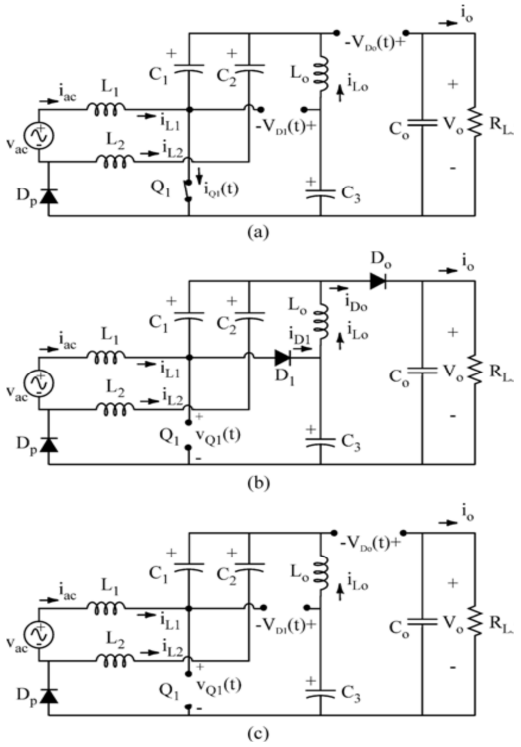

Figure 5. (a) Switch ON topology. (b) Switch OFF topology. (c) DCM topology.

Table 1.

No of stages	Switches	Diodes	Inductor current
First stage	Q_1, T_{on}	D_1 , D_0 is reverse biased	diLn/dt = Vac/Ln
Second stage	Q_2, T_{off}	D_1 , D_0 is forward biased	diLn/dt = - Lc/Ln
Third stage	Q_2, T_{off}	D_1, D_2 reverse biased	constant

4.1.1. First Stage

In this stage, switch *Q*1 is turned-on by the control signal and both diodes*D*1 and *Do* are reversed biased as shown in Fig. 4(a).
In this stage, the three-inductor currents increase linearly at a rate proportional to the input voltage

$vac\ diLn/dt = vac/Ln,\ n= 1, 2, o.$ (1)

4.1.2. Second Stage

During this subinterval, switch $Q1$ is turned-off and both diodes $D1$ and Do will conduct simultaneously providing a path for the three inductors' currents as shown in Fig. 4(b). In this stage, the three inductors' currents decrease linearly at a
rate proportional to the capacitor $C1$ voltage $VC1$. This stage ends when the sum of the currents flowing in the inductors addsup to zero, hence diodes $D1$ and Do are reverse biased

$diLn/dt= -vC1/Ln,\ n= 1, 2, o.$ (2)

4.1.3. Third Stage

In this stage, switch $Q1$ remains turned-off while both diodes$D1$ and Do are reverse biased as illustrated in Fig. 4(c). Diode Dp provides a path for iLo. The three inductors behave as current sources, which keeps the currents constant. Hence, the voltage across the three inductors is zero. This period ends when switch$Q1$ is turned-on initiating the next turn-on of the switching cycle. Fig. 5 illustrates the theoretical DCM waveforms during one switching period Ts for the proposed rectifier.

5. Simulation Results

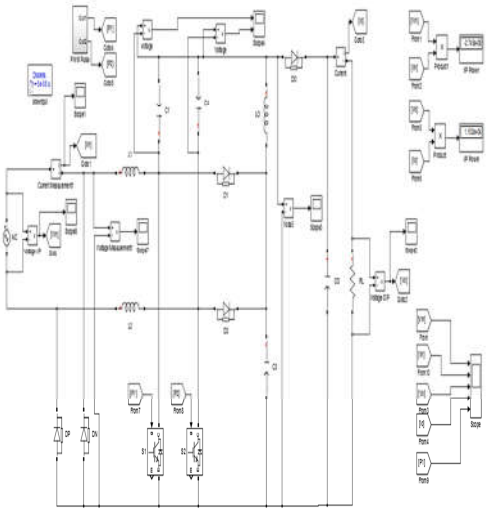

Figure 6.Bridgeless PFC Modified SEPIC Rectifier Simulation Diagram

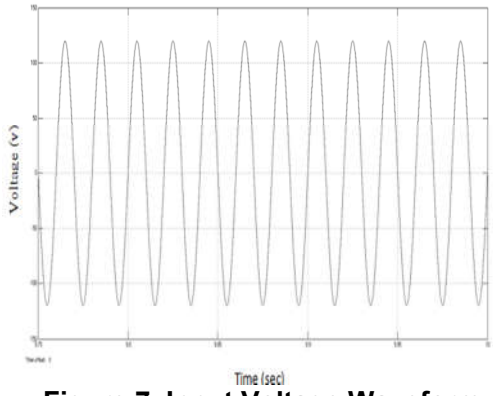

Figure 7. Input Voltage Waveform

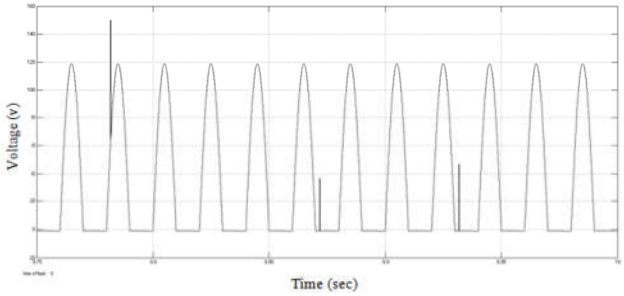

Figure 8. Rectifier Output Waveform

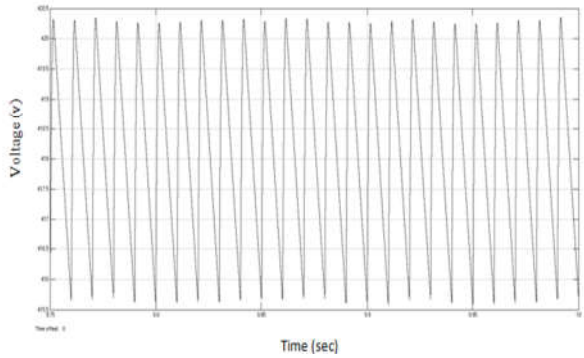

Figure 9.Output Voltage Waveform

6. Conclusion

In the proposed method achieved higher efficiency than the full bridge method. The proposed method having lower voltage stress over the whole input voltage range than existing method .The input voltage and current are in phase so the power factor correction is achieved perfectly. The desired boosted output voltage is achieved in the output. The simulation results are validate for proposed open loop and closed loop circuit condition

References

[1] Harmonic Current Emission Guidelines, European Power Supply Manufactures Association Standard EN 61000- 3-2 Nov. 2010.
[2] H. Wang, Y. Tang, and A. Khaligh, "A bridgeless boost rectifier for Low voltage energy harvesting application, " IEEE Trans. Power Electron., Vol.28. no. 11, pp. 5206 – 5214, Nov, 2013.
[3] W. Choi, J. Kwon, E. Kim, J.Lee, and B. Kwon," Bridgeless boost Rectifier with low conduction losses and reduced diode reverse- Recovery problems, " IEEE Trans. Ind. Electron., vol. 54, no. 2, pp.769 – 780, Apr. 2007.
[4] Y.Jang and M. Jovanovic, " A Bridgeless PFC boost rectifier withOptimized magnetic utilization, "IEEE Trans. Power Electron., vol.24.no.1, pp. 85 – 93, Jan. 2009.
[5] M.Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with Reduced components and conduction losses, " IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4153 – 4160, Sep. 2011.
[6] A Fardoun, E. Ismail, A. Sabzali, and M.AI –Saffar, "Bridgeless Resonant pseudo boost PFC rectifier, " IEEE Trans. Power Electron., Vol. 29, no. 11, pp. 5949 – 5960, Nov. 2014.
[7] C.Jingquan, D.Maksimovic, and R. W. Erickson, "Analysis and Design of a low – stress buck – boost converter in universal – input PFC application, "IEEE Trans. Power Electron., vol. 21, no. 2, pp. 320 – 329, Mar. 2006.
[8] A Sabzali, E.H. Ismail, M.AI-Saffar, and A.Fardoun, "A new bridgeless PFC SEPIC and Cuk rectifier with low conduction and switching Losses, " IEEE Trans. Ind. Appl., vol. 47, no. 2, pp. 873 – 881, Mar / Apr. 2011.
[9] E. H. Ismail, " Bridgeless SEPIC rectifier with unity power factor And reduced conduction losses, " IEEE Trans. Ind. Electron., vol.56,no. 4, pp. 1147- 1157, Apr. 2009.