A Single-Ended with Dynamic Feedback Control 10T Subthreshold SRAM Cell

[1]**Motla Sushma**   [2]**Mr.B.Kishore Kumar**

sushma.motla1@gmail.com[1]   bungakishore@gmail.com[2]

[1]M.Tech (VLSI-SD), J.B Institute of Engineering and Technology

[2]Assistant Professor J.B Institute of Engineering and Technology

ABSTRACT: **This paper implements the design of Single ended dynamic feedback control 10T sub threshold cell. The 10T can operate at very low power levels such as ultra low power ranges. The switching speed of 10T is very high as compared to the proposed method 8T cell. The proposed single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultralow power supply. The proposed 8T cell has less leakage current when compared to the 6T, 5T, RD-8T. The designs 6T, 5T, RD-8T, 8T and 10T are implemented at different voltage levels by using Tanner-Tool in 90nm technology and compared.**

1. INTRODUCTION

The convenient microchip controlled gadgets contain inserted memory, which speaks to a substantial part of the framework on chip (SoC). These convenient frameworks need ultralow power expending circuits to use battery for more term. The force utilization can be minimized utilizing nonconventional gadget structures, new circuit topologies, and advancing the engineering. In spite of the fact that, voltage scaling has prompted circuit operation in sub limit administration with least power utilization, however there is a drawback of exponential lessening in execution. The circuit operation in the sub threshold administration has cleared way toward ultralow power inserted recollections, fundamentally static RAMs (SRAMs). Be that as it may, in sub threshold administration, the information steadiness of SRAM cell is a serious issue and declines with the scaling of MOSFET to sub nanometer Technology. Because of these impediments it gets to be hard to work the traditional 6-transistor (6T) cell at ultralow voltage (ULV) power supply.

For a stable SRAM bit cell operating at lower supply voltages, the stability of the inverter pair should be improved. None of the aforementioned bit cells has a mechanism to improve the stability of the inverter pair under process variations. We propose a Schmitt trigger

based differential bit cell having built-in feedback mechanism for improved process variation tolerance. In particular:

1) We have proposed a novel Schmitt trigger based differential, 8-transistor SRAM bit cell with built-in feedback mechanism. It requires no architectural change compared to the 6T cell architecture. It can be used as a drop-in replacement for present 6T based designs.

2) We have demonstrated that with respect to 6T cell, the proposed Schmitt trigger based bit cell gives better read stability, better write-ability, and improved process variation tolerance, lower read failure probability, low-voltage/low power operation, and improved data retention capability at ultralow voltage.

3) We have fabricated a test chip in 0.13 m logic process technology and validated the proposed technique.

An SRAM array containing the proposed memory bit cell is functional at 160 mV of supply voltage. To maintain the clarity of the discussion, the "10T cell" is referred as the memory cell reported. The proposed Schmitt Trigger (ST) based 10T memory cell is referred as the "ST bit cell" hereafter. The rest of this paper is organized as follows. In Section II, the proposed ST bit cell operation is described. In Section III, comparison is made among 6T/8T/10T/ST bit cells for various SRAM metrics.

2. LITERATURE SURVEY

Design and Analysis of an 8T Read Decoupled Dual Port SRAM Cell for Low Power High Speed Applications

Speed, power consumption and area, are some of the most important factors of concern in modern day memory design. As we move towards Deep Sub-Micron Technologies, the problems of leakage current, noise and cell stability due to physical parameter

variation becomes more pronounced. In this paper we have designed an 8T Read Decoupled Dual Port SRAM Cell with Dual Threshold Voltage and characterized it in terms of read and write delay, read and write noise margins, Data Retention Voltage and Leakage Current. Read Decoupling improves the Read Noise Margin and static power dissipation is reduced by using Dual-Vt transistors. The results obtained are compared with existing 6T, 8T, 9T SRAM Cells, which shows the superiority of the proposed design. The Cell is designed and simulated in TSPICE using 90nm CMOS process.

8T SRAM Cell Design for Dynamic and Leakage Power Reduction

This paper addresses a, novel eight transistor (8T) CMOS SRAM cell design to enhance the stability and to reduce dynamic and leakage power. For the validation of proposed 8T SRAM cell, compared results with reported data. The parameters used in the proposed cell are comparable to the existing 8T SRAM cell at same technology and design rules. The stability of the proposed cell has been analyzed using N-curve metrics. Write operation is achieved in the proposed 8T SRAM cell by charging discharging single Bit Line (BL), which results in reduction of dynamic power consumption. The proposed 8T SRAM cell has achieved 38.33% dynamic power reduction and 25.31% reduction in leakage power comparing with the reported data of 8T SRAM cell, which validate the desired design approach.

3. EXISTING SYSTEM

The circuit operation in the sub threshold regime has paved path toward ultralow power embedded memories, mainly static RAMs (SRAMs). However, in sub threshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to sub nanometer technology. Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T)] cell which offers read static noise margin (RSNM) comparable with hold static noise margin

(HSNM). However, RD-8T suffers from leakage introduced in read path. This leakage current increases with the scaling thereby, increasing the probability of failed read/write operations. Similar cells that maintain the cell current without disturbing the storage node are also proposed.

6T SRAM CELL:

Like other memories, there are three operation modes for SRAM cell: standby (or hold), read, and write modes. In the standby mode, the word line is set to a low-voltage level and both the internal nodes are isolated from the bit lines.

Read Operation:

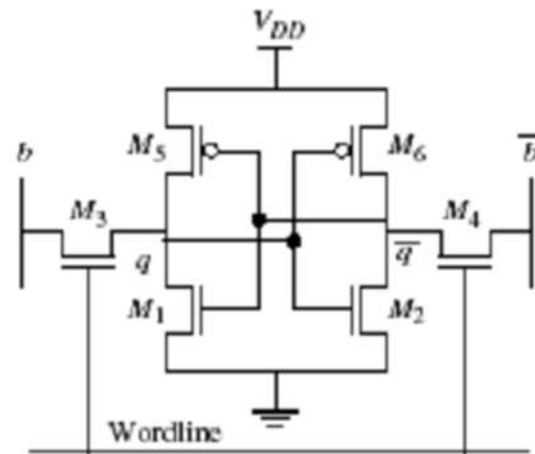In SRAM, for any operation to be performed, the word line should be high. To perform read

Fig 1: 6T SRAM cell

Operation, initially memory should have some value. Therefore let us consider memory has Q=1 and Q'=0. Raise the word line to high, to perform the read operation. Bit and bit_b acts as output lines, and these bit lines are initially pre-charged i.e. there will be a node voltage Vdd at bit and bit_b. As Q and bit are high, there will be no discharge in the circuit. As Q' is 0, there will be a voltage difference between the Q' and the node voltage at bit_b, hence bit_b voltage decreases. Therefore there will be discharge in the circuit and current flows. Bit and bit_b are connected to the sense amplifier, this sense amplifier acts as a comparator, so When bit' is low the output will be 1. Hence input Q=1 and we got the output as 1, read operation verified.

Write Operation:

Consider the memory bits consists of Q=0 and Q'=1. Initially word line is high and hence writes operation can be performed. In the write operation bit and bit' are input lines. As we have control on the bit lines, initially make the bit_b connected to ground so that we can have the voltage difference between Q' and bit_b. To write 1 into the SRAM cell, D2 must be stronger than P2; this can be achieved by changing the aspect ratio of the transistors. Hence Q will be 1. Initially Q=0 after the operation Q=1, hence we write successfully into the memory

5T SRAM CELL:

Operation of a standard 6T bit cell at low voltages is limited by both its read and writes margins, due to process and mismatch variations. The drive strength of MOSFET devices becomes an exponential function of the device's threshold voltage (VT), as the supply voltage nears the sub-threshold region, causing variation to increase dramatically. As
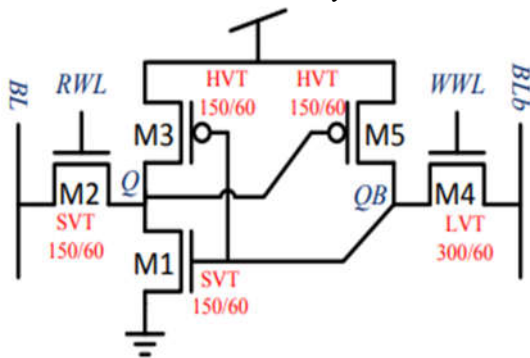

Fig 2: 5T SRAM cell

Read Operation:

The read access of the 5T cell is initiated by precharging the BL signal, while holding BLb discharged (its standby state). Subsequently, RWL is asserted, resulting in a single-ended readout of node Q. If Q is high (the hold '1' state), there is no voltage drop over M2 and all voltage levels remain unchanged. If Q is low (the hold '0' state), charge-sharing is initiated between BL and Q, discharging BL and resulting in a '0' readout. As with 6T readout, the voltage level at Q rises, lowering the overdrive voltage of M5, potentially cutting off the pull-up of QB. However, QB is left at a high state, as there is no active pull-down network to discharge it (the leakage pull-down to BLb takes much longer than the read access time). Therefore, once the read-access is completed and RWL is lowered, M1

(with VGS=QB≈VDD) will quickly discharge Q back to its original state. In fact, the feed through to Q on the falling edge of RWL actually improves this effect. As a result, the read-stability of the 5T cell is much higher than that of its6T counterpart, providing robust sub-threshold readability.

Write Operation:

The single-ended read operation of the proposed 5T cell essentially removes the read sizing constraint of the right access transistor (M4). In fact, the 5T cell enhances the efficiency of the pull-up operation through M4, as node QB has no pull-down network to contend it. Therefore, by charging BLb and asserting WWL, QB is easily pulled up past the threshold voltage of M1, enabling the pull-down network of node Q. This write '0' operation can be achieved single endedly; however, by discharging BL and asserting RWL, a faster and more robust write operation is achieved.

RD-8T SRAM Cell:

The read and write assist transistors are denoted as 'Rwa' and 'Twa' respectively. The cross-coupled inverters read and write assist transistors have a high threshold voltage and the access transistors have a low threshold voltage. The high threshold voltage transistors reduce leakage current of the cell in standby mode, hence limiting static power dissipation. The access transistors have a low threshold voltage to ensure minimum read and write delays and high speed operation.
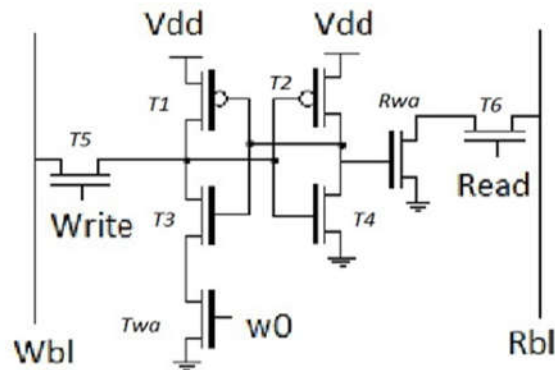

Fig 3: RD-8T SRAM cell

Read Operation:

The Rbl is pre-charged to Vdd before every read operation and W0 is kept '1' to sustain the latch operation. When Q is '0' and QB is '1' (cell storing a

'0') and Read is '1', Rwa is ON and forms a discharge path for the read bit-line to ground, which gives a successful read operation. Again, when Q is '1' and QB is '0' (cell storing '1') and Read is '1', Rwa is OFF and the read bit-line voltage is maintained at Vdd. The threshold voltage of Rwa is kept high to ensure that there is minimum leakage current during a read '1' operation and the voltage in RBL is maintained at Vdd.

Write Operation:

During every write operation W0 is made '0'. This turns Twa OFF, weakening the feedback loop to ensure a successful write operation. WRITE is '1' during write operation. Initially, when Q is '0' and QB is '1' (cell storing '0') and we want to write a '1', it is difficult to force the node Q to '1' through a pass transistor as the inverters are strongly cross-coupled. Hence the pull-down strength of the first inverter has to be weakened through the series transistor Twa. When a '0' has to be written to a cell initially storing a '1' the node Q discharges through T5 and Wbl, thus making a successful write operation. During HOLD state, W0 is kept high for normal operation of the latch and READ and WRITE signals are kept low.

4.   PROPOSED SYSTEM

8T SRAM CELL:

The single-ended design is used to reduce the differential switching power during read–write operation. The power consumed during switching/ toggling of data on single bit line is lesser than that on differential bit-line pair. The SE-DFC enables writing through single nMOS in 8T. It also separates the read and write path and exhibits read decoupling. The structural change of cell is considered to enhance the immunity against the process–voltage–temperature (PVT) variations.
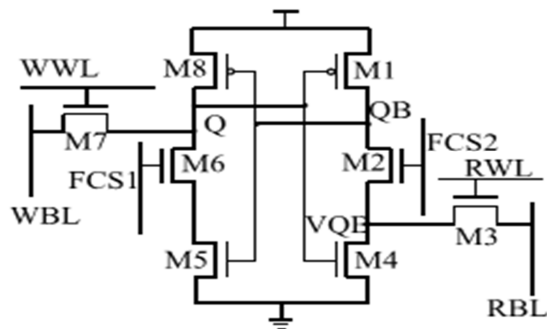

Fig 4: 8T SRAM cell

Write Operation:

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFFM6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1– M2–M4) changes the state of QB from 1 to 0. To write a 0 at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up pMOS M1 charges QB to 1.

Read Operation:

The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operations, Q is 0 and RBL holds pre charged high value and the inverter sense amplifier gives 0 at output.

EXTENSION:

10T SRAM CELL:

The power consumed in 10T SRAM is lesser than the SRAM that uses differential bit line pair. Moreover, it uses single nMOS to write data in SRAM. Transistors N1, N2 decouples the storage node from the bit line thereby increasing the SNM. Sleep transistors are introduced to reduce the power consumption further. These sleep transistors are ON when the circuit is ON and switch OFF when the circuit is idle. By cutting of the power supply it reduces the leakage power.SL and SLB signals are used to control the sleep transistors.
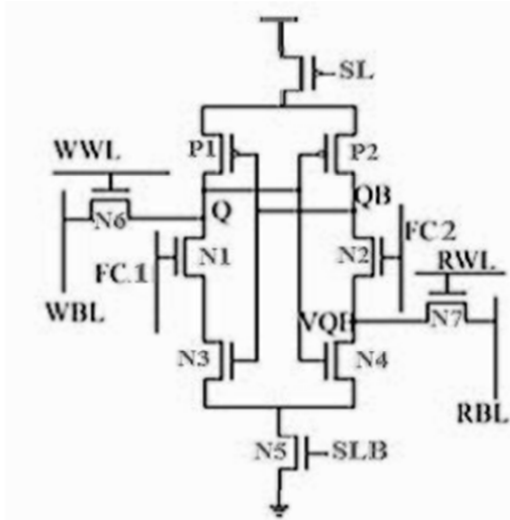
Fig 5: 10T SRAM Cell

The transistors P2, P3, N3 and N4 forms the cross coupled inverters to store the data. The write word line (WWL) controls the transistor N6 which transfers the data from word bit line (WBL). Where, read bit line (RBL) transfers the stored data to the output when the read word line (RWL) is activated. Transistors N1, N2 are used for the dynamic feedback control. FC1, FC2 are the lines used to control the N1 and N2 transistors.

Read Operation:

For both read and pre charge phase, SL is made low and SLB is made high: Before reading the data, RBL is pre charged to VDD. When the read operation starts the RWL is made high, both FC1 and FC2 is made low. If 1 is stored in node Q, the transistor N4 which is connected to the ground through N5 transistor is activated. Hence, the RWL which is made high gets discharged to ground through the N4, N5 transistors. If '0' is stored in node Q, the transistor N4 is not activated and hence does not have a connection to ground. Therefore, the RWL which is made high does not gets discharged to the ground and this can be sensed through the inverting sense amplifier.

Write Operation:

During write, read and precharge phase of the SRAM cell, SL is made low and SLB is made high otherwise SL is made high and SLB is made low to turn off the transistors P1 and N5. To write 1, SL is lowered to zero and SLB is charged to vdd, FC1 is made low, FC2 is made high which makes the transistor N1 ON and N2 OFF. Data is given to the WBL as 1 and WBL is made high. Then current flows

from WBL to Q node and the complement of it is store in QB node. Since, FC2 is high, N2 is ON and hence the nodal voltage gets transferred to the virtual QB node, whereas to write 0, FC1 and FC2 are made high and low, respectively. WBL is made low and WWL is made high. Hence, 0 is stored in Q and the complement data is stored in QB. Since FC1 is high N1 transistor is ON and the Q node is connected to the ground and even if there are any charges present in node Q gets discharged through it, whereas N2 is OFF since FC2 is lowered to zero. Therefore, 0 is stored in the node Q and '1' is stored in the node QB.
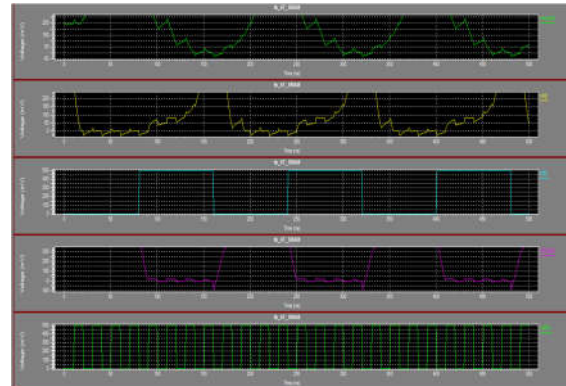
5. RESULTS

5.1 EXISTING RESULTS:

5.1.1 6T SRAM CELL:
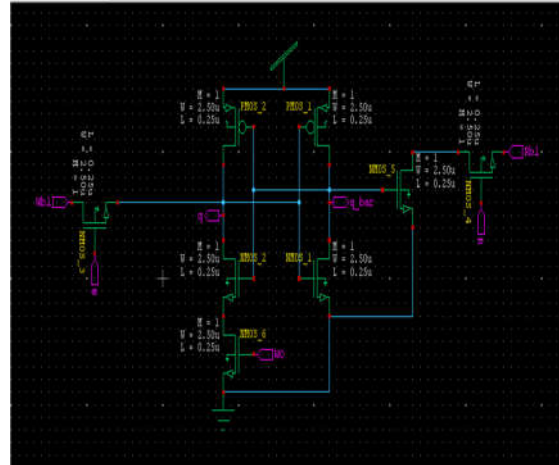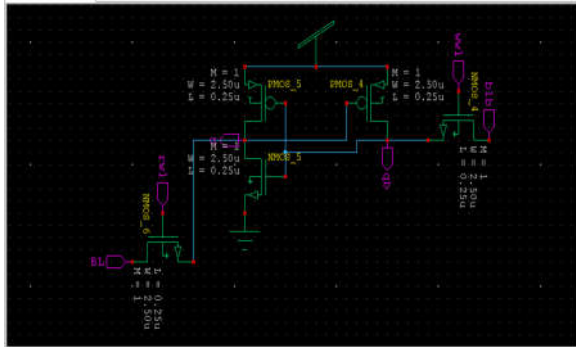
Schematic:
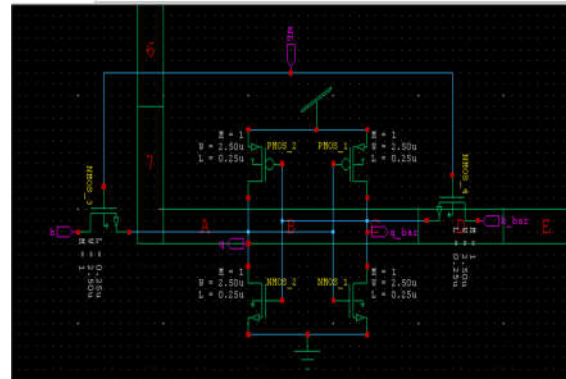
Output Waveform:
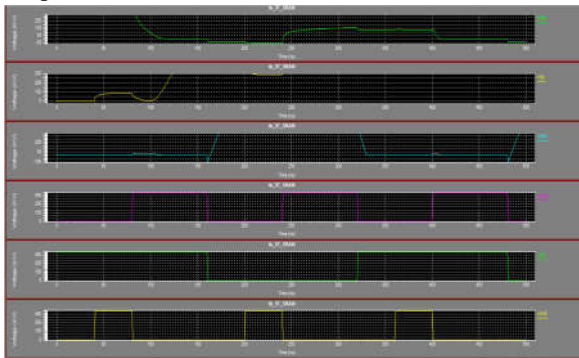

Power Calculation:

```
Power Results
VVDD from time 0 to 5e-007
Average power consumed -> 8.399260e-008 watts
Max power 1.724571e-006 at time 1.61e-007
Min power 2.163945e-010 at time 2.2e-007
```

5.1.2 5T SRAM CELL:
Schematic:
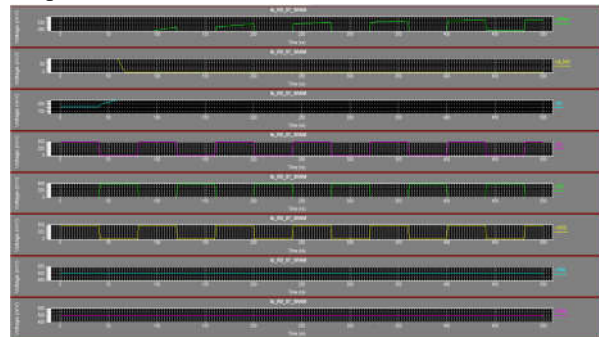

5.2.1 8T SRAM CELL (right schematic):

Output Waveform:

Output Waveform:

Power Calculation:

```
Power Results
vvdd from time 0 to 5e-007
Average power consumed -> 6.758239e-008 watts
Max power 1.588342e-006 at time 1.61e-007
Min power 1.599561e-012 at time 1.4725e-007
```

Power Calculations:

```
Power Results
vvdd from time 0 to 5e-007
Average power consumed -> 5.769548e-009 watts
Max power 2.948273e-007 at time 6.525e-008
Min power 1.046560e-011 at time 1.4125e-007
```
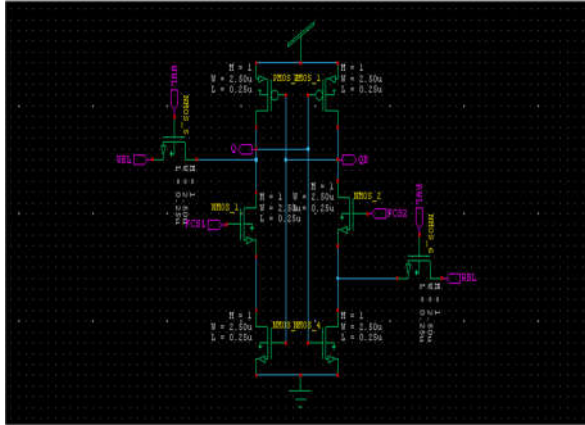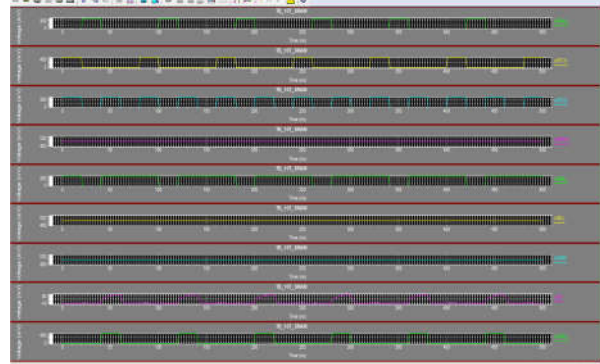
5.1.3 RD-8T SRAM CELL:
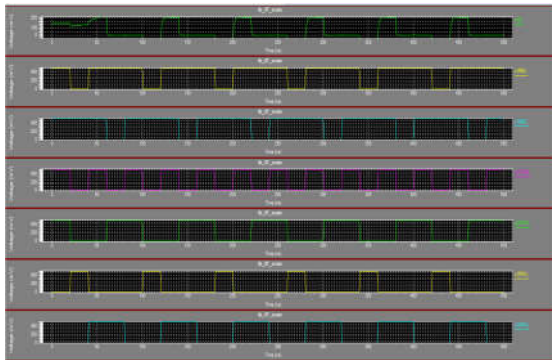Schematic:

5.2 PROPOSED RESULTS:
5.2.1 8T SRAM CELL:
Schematic:

Output Waveform:

Power Calculation:

Power Results

vvdd from time 0 to 5e-007

Average power consumed -> 4.421354e-008 watts

Max power 2.904644e-006 at time 6.1e-008

Min power 1.526950e-010 at time 1.2e-007

5.3 EXTENSION RESULTS:

5.3.1 10 T SRAM CELL:

Schematic:

Output Waveform:

Power Calculation:

Power Results

VVDD from time 0 to 5e-007

Average power consumed -> 1.285166e-010 watts

Max power 1.989407e-007 at time 6.1e-008

Min power 1.063266e-012 at time 6.25e-011

5.4 POWER COMPARISION OF 5T,6T,RD-8T,8T, and 10T at 400mv

DESIGN	POWER(WATTS)
6T	$8.399260e^{-008}$
5T	$6.758239e^{-005}$
RD-8T	$5.769548e^{-009}$
8T	4.421354^{-009}
10T	$1.285166e^{-010}$
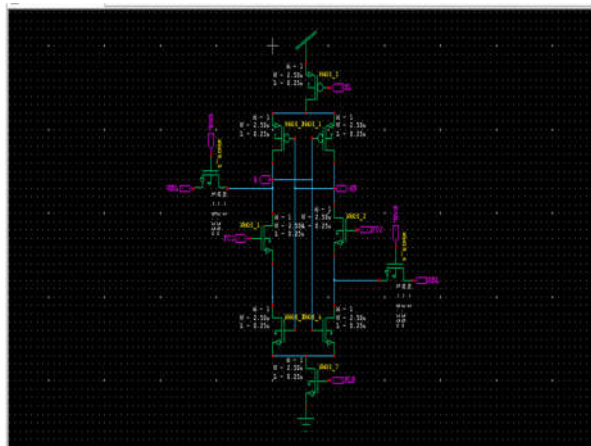
6. CONCLUSION

The implemented design of single ended 10T SRAM Cell and proposed 8T cell has high stability and are operated at different voltage levels and compared the proposed 8T SRAM with different transistor SRAM cell includes 5T, 6T, RD-8T and 10T. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design. Future and applications of the

proposed 8T cell can potentially be in low/ULV and medium frequency operation like neural signal processor, sub threshold processor, wide-operating-range IA-32 processor, fast Fourier transform core, and low voltage cache operation.

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BIOGRAPHIES:

GUIDE DETAILS:

Mr. B. Kishore Kumar is working as an Assistant professor in the Department of Electronics and communications in J.B Institute of Engineering and Technology.

STUDENT DETAILS:

Motla Sushma is pursuing her M.Tech VLSI-SD in J.B Institute of Engineering and Technology.

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