TORPEDO SUB SYSTEM PHYSICAL DESIGN IMPLEMENTATION

P V J Raj Kumar[1], S. Aruna Kumari[2] , K. Raja Sekhar[3]

[1]Assistant Professor, Department of Electronics and Communication Engineering,
BABA Institute of Technology and Sciences Visakhapatnam, Andhra Pradesh, India

[2] Assistant Professor, Department of Electronics and Communication Engineering,
BABA Institute of Technology and Sciences Visakhapatnam, Andhra Pradesh, India

[3] Assistant Professor, Department of Electronics and Communication Engineering,
BABA Institute of Technology and Sciences Visakhapatnam, Andhra Pradesh, India
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pvjrajkumar@gmail.com, aruna0454@gmail.com, rajkonari@gmail.com

ABSTRACT:

The Torpedo technology has invented for three centuries. In this paper, torpedo consists of no more than an explosive charge mounted on the end of a spar that was extended toward an enemy vessel. A combat ready torpedo consists of three major sections are guidance and control, propulsion and the warhead. The modern **torpedo** is a weapon moves with its main source of tractive power rather than requiring an external means with an explosive warhead, launched above or below the water surface, it determines the exact position underwater towards a target, and designed to detonate either on contact with its target or in proximity to it. Practically, it was called an autonomous torpedo; consequently called a *fish*. From about 1800, *torpedo* has been used trictly to designate an underwater self-propelled weapon.

Torpedoes require maintenance and repair, storage and warshot issue preparation, refurbishment after exercise shots, and engineering services to resolve problems after fleet introduction reviews for longer-range shellfire.

Today's torpedoes can be classified into two types depending upon its weights; and into straight-running, driverless guide, and wire-guided. They can be used in different types of platforms**.**

1 - PHYSICAL DESIGN FLOW

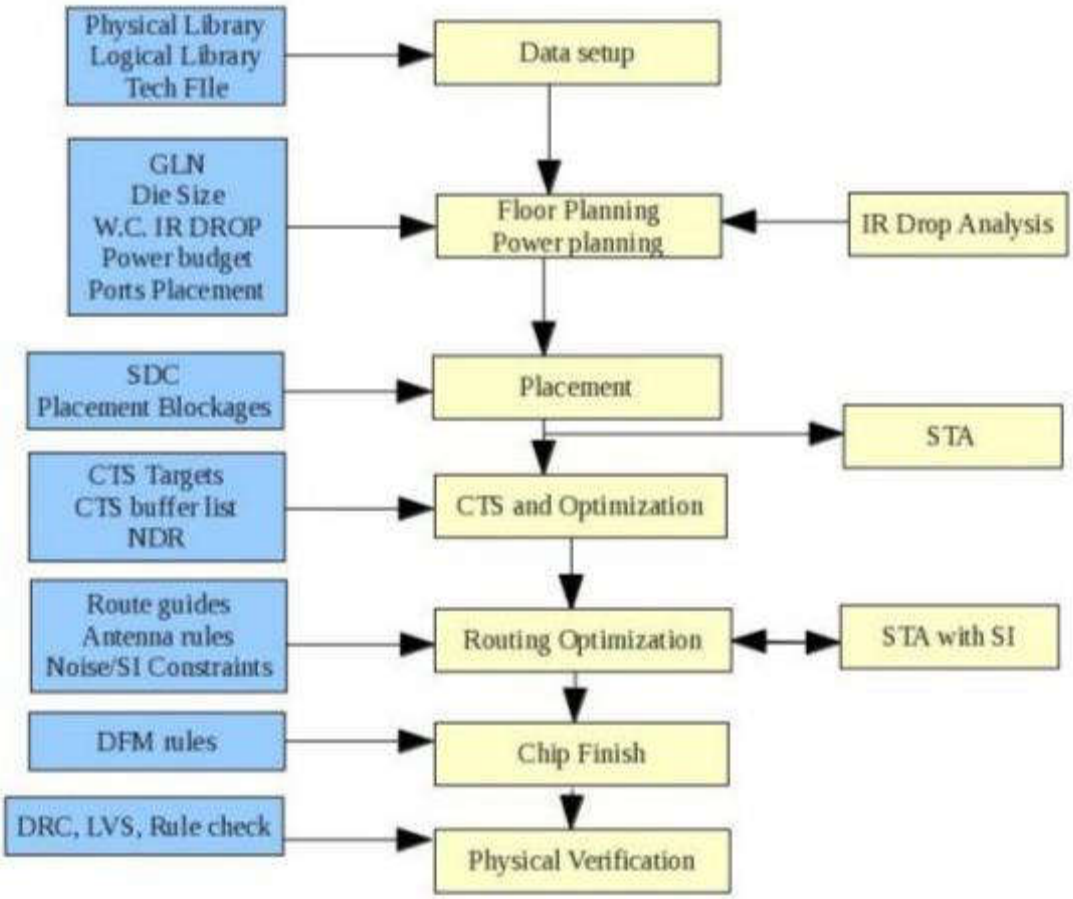

Fig 1. Physical Design Flow

2 -Data Set-up and Design Planning

This is the primary step of IC compiler flow. The objectives of design planning is to create milky-way design library and design cell and load necessary data required to run IC compiler. The data required for IC compiler are loaded in to a project specific container known as design library.

Logic/timing libraries (.db or lib for pad cells, macro cells and standard cells):

• Max min library for SRAM

• Milkyway reference libraries

• RC model files (TLU plus or .itf files) Mapping file for TLUplus, Max TLUplus file, Min TLUplus file.

• Physical libraries (for standard cell,macro,I/O cell)

• Technology file(.tf format)

Gate level net list (DEF/DDC/VERILOG):

For our design we used verilog file using read verilog and converting into hierarchical in flat by using uniquify.

- Torpedo.v info:
- Total number of cell instances: 43275
- Total number of nets: 43351
- Total number of ports: 129 (include 0 PG ports)
- Total number of hierarchical cell instances: 1089

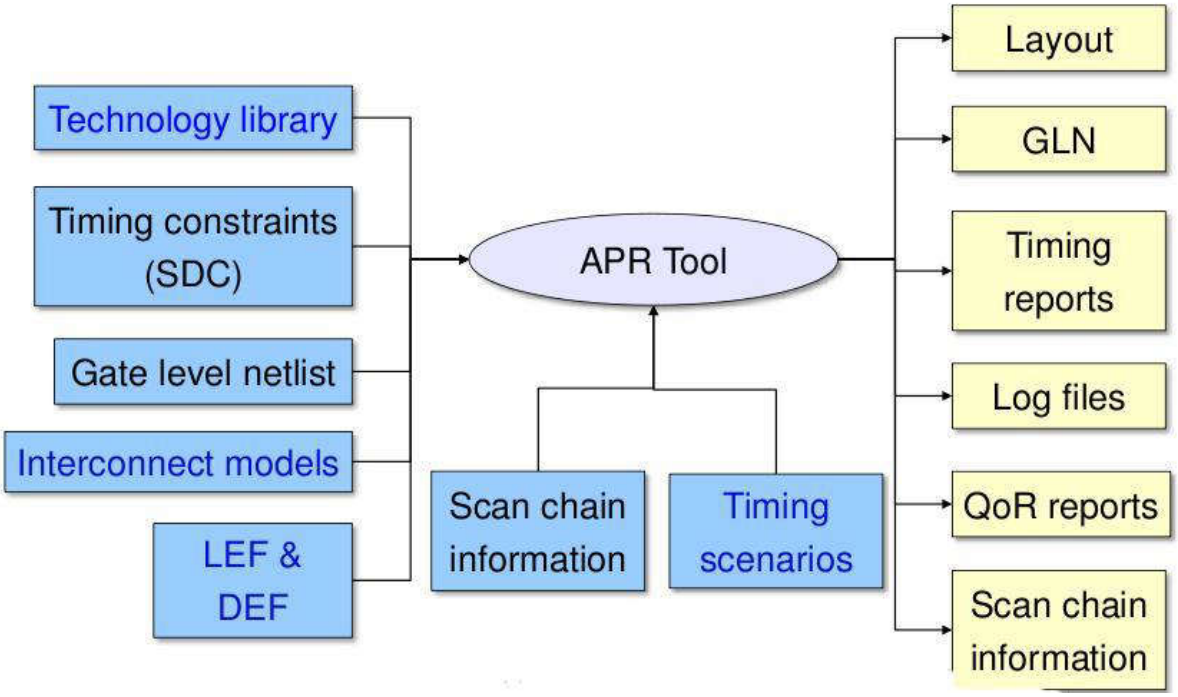

Figure2: Input and Output of APR

3 -Floor planning

Floor-planning is the process of sizing and placing hierarchical cells and functional blocks in a manner later physical design steps more effective. Floor planning in hierarchical flows provides a basis for estimating the timing of the top level. A timing budget allocation the clock cycle time to each block according to the top level timing estimation.

An effective floor-plan helps ensure timing requirement in many ways to make small of critical paths short by blocks placing and avoid blocking which leads to long path and avoids noise levels in the block placing. The challenge is to create a floor-plan with good area efficiency while leaving sufficient area for routing.

The step involves in floor-planning:

• Defining the core area (2450 X 2450) um and IO core spacing.

• Defining ports specified by top level engineer.

• Design a Floor Plan and Power Network with horizontal metal layer such that the total IR

• Drop must be less than 5% (VDD+VSS) of VDD to operate within the power budget of 300mW.

• Defining Placement and Routing blockages.

• Source the verilog file i.e., torpedo's. After reading all macros and standard cells, they are placed outside the core area as shown in the below figure.

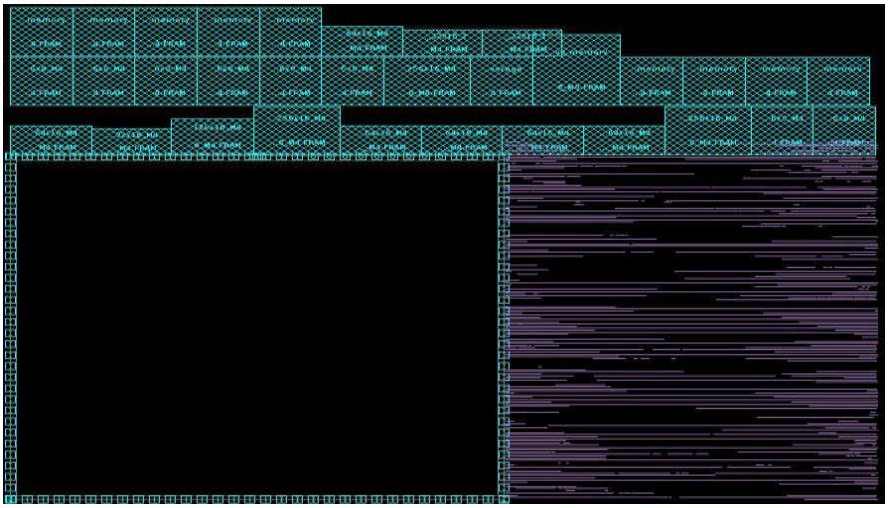

Figure 3: Basic Floorplan

Blockage creation:

During the Power planning in some vertical channel region between two Macros, we put partial blockage allowing only buffers & inverters to be placed there. In some of such regions, metal1 rail was discontinued .So we put some m4 rails connecting power/ground thus enabled m1 rails in those regions so that the buffers & inverters sitting there can get the power and ground connection. In some other vertical channel region, we put hard blockage to prevent placement of any cell in that region. Both partial & hard blockages are shown in the following figure.

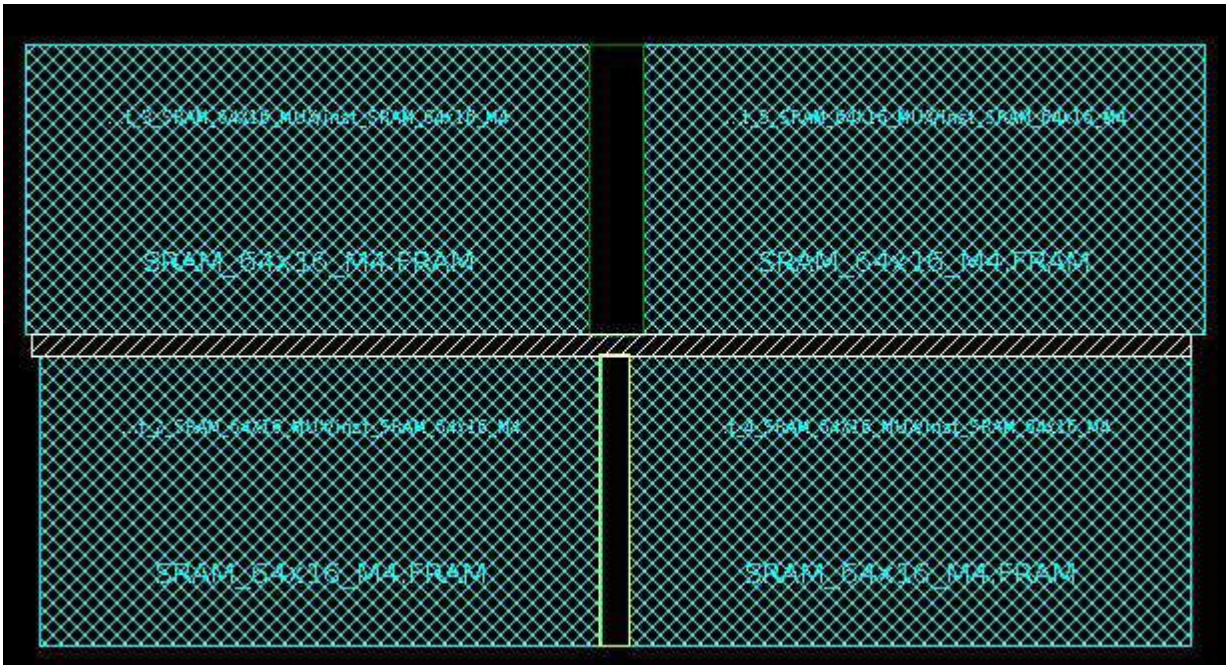

Figure 8: Soft, partial and hard placement blockage

Power Planning

Main objective is to provide power to each macro and standard cell while meeting IR drop and power budget.

Power Planning is very important stage in Physical design during which we synthesize the power network in order to provide power to all macros and standard cells within the given IR-Drop limit, in our case 5% of (VDD+VSS).

Steady state IR Drop is caused by the resistance of the metal wires comprising the power distribution network. By reducing the voltage differences steady-state IR Drop reduces both the speed and noise immunity of the local cells and macros.

As vertical power straps are fixed (m6_ power.tcl) only we have to modify the horizontal metals i.e.,metal_5 (m5) to achieve target IR-Drop of 90mV and power budget of 300mV.

Used set_fp_rail_constraints to generate vertical and horizontal power strap (width, spacing and pitch). Its an iterative process till you get desired IR drop. After that fixing metal5 width, pitch, spacing, off-set and no. Of strap information in a tcl file. This will save time for next run.

4 -Placement

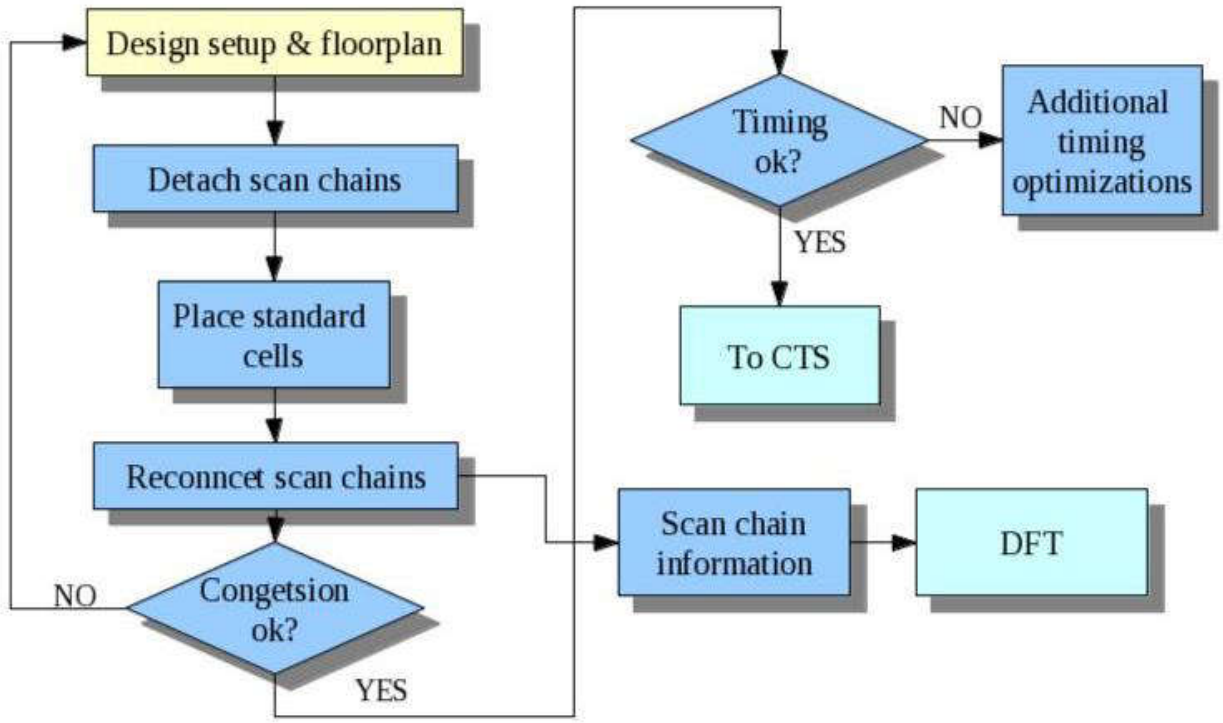

Figure 18: Placement Flow

Timing Analysis:

• During the first we got 24K violations with most violations in REGIN paths due to the over constraining of input to reg paths.

• We have analysed some paths which are false paths and reported them to synthesis engineer.

• We have observed some paths in which Macro delay is more than clock period and reported them to project manager.

• During initial design set-up , we have segregated all timing paths to REGIN, REGOUT and CLOCK groups for better optimization of sub-critical paths.

• We gave critical range just greater than WNS to optimize all sub-critical paths and gave another run, and observed that TNS got reduced.

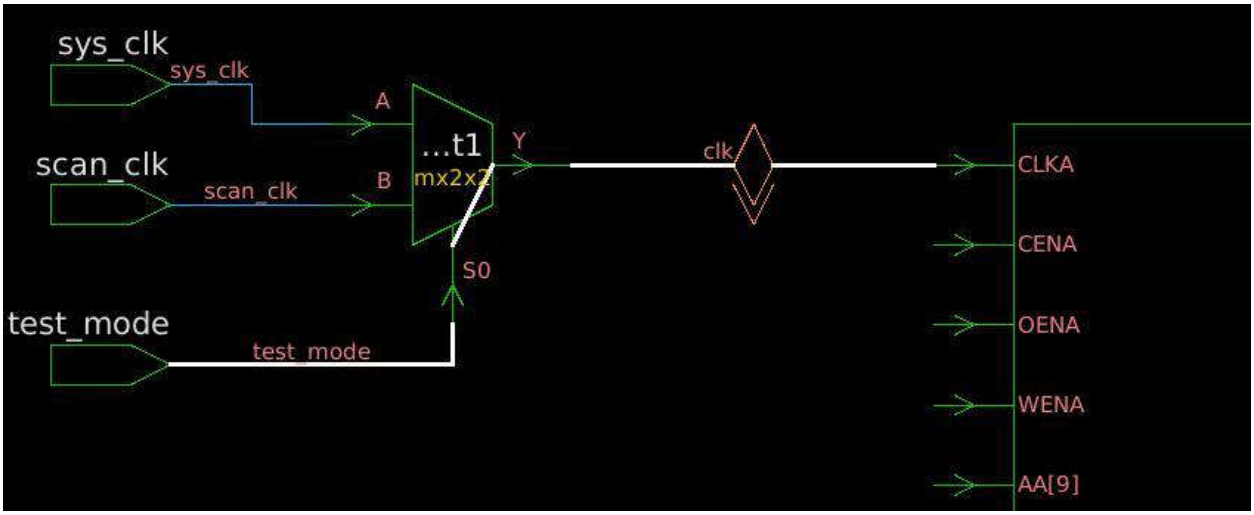

Figure 28: Timing Arc from So->Y of MUX.

Disabling timing arc from select pin to output pin for MUX in clock paths(false paths).

5 -Clock Tree Synthesis

Clock Tree Synthesis is the process of distributing clock signals to clock pins based on physical/layout information. By default, clock networks are considered ideal during logic synthesis and physical placement. An ideal clock network consists of a single driver connected to

all the sequential devices in the design clocked by the clock, without any buffers. An ideal network can have zero latency, uncertainty, or transition times, that are uniform throughout the clock network.

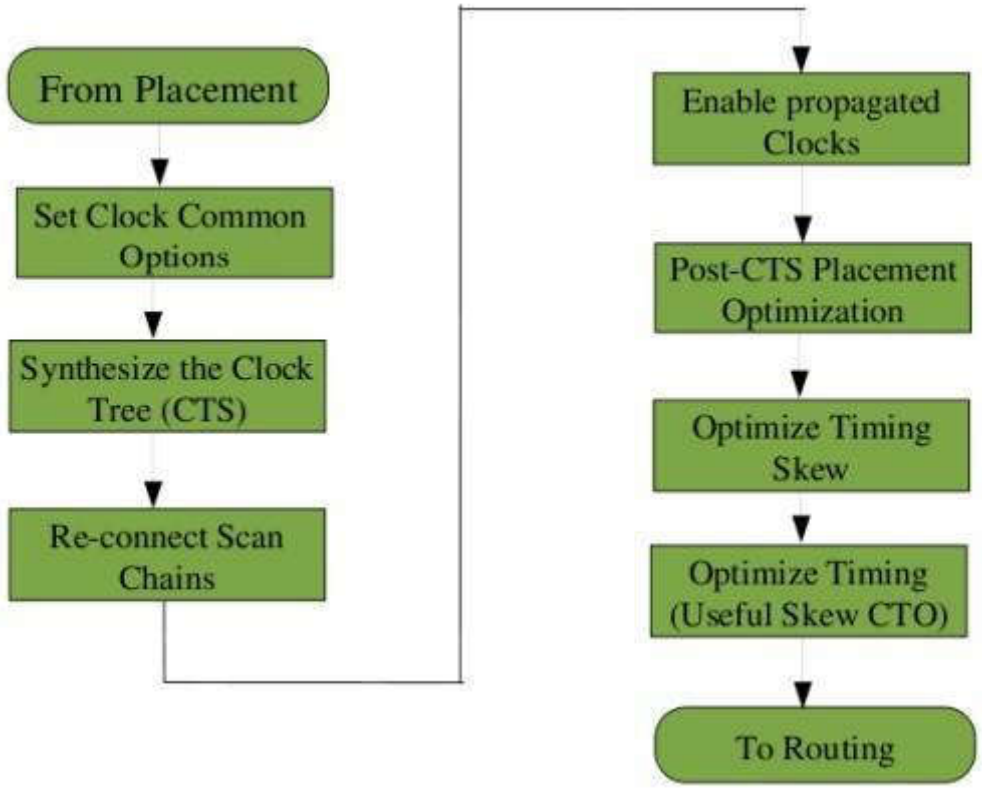

Figure 34: CTS Flow

Clock tree synthesis is the replacement of an ideal clock network with a hierarchy of buffer with the goal of minimizing latency, skew and transition times. This is typically done after placement and high-fanout net synthesis and before routing. Even though during placement High fanout nets are synthesized and clock is one of the high fanout net is kept ideal because HFN synthesis is used to balance load but it is not good at balancing skew.Figure 23: CTS Flow.

Results and Analysis:

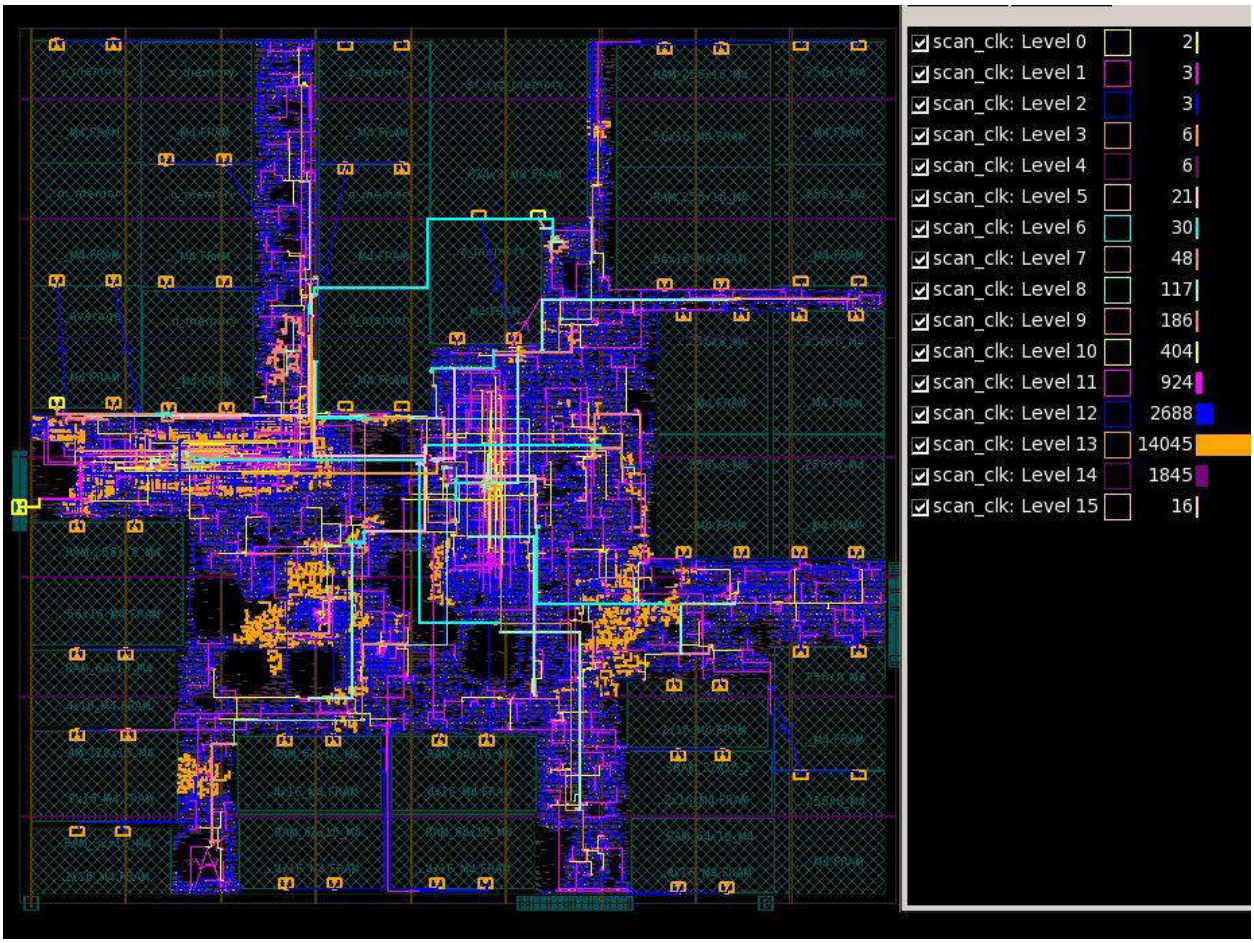

Figure 35: Clock Tree (scan_clk)

Inserting Port Protection Antenna Diodes:

Antenna effect:

During manufacturing of metal layers, each metal layers collect some charges and these gets discharged through the thin gate oxide layer. If the charge is huge enough it will break the gate oxide and destroy the transistor. This is called Antenna Effect.

During CTS we also used port protection diodes to prevent antenna effect on the gates connected to port terminals using insert_port_protection_diodes. So putting antenna diode the gates which are connected directly to ports will be protected from antenna effect at top level.

Port Protection Diodes :

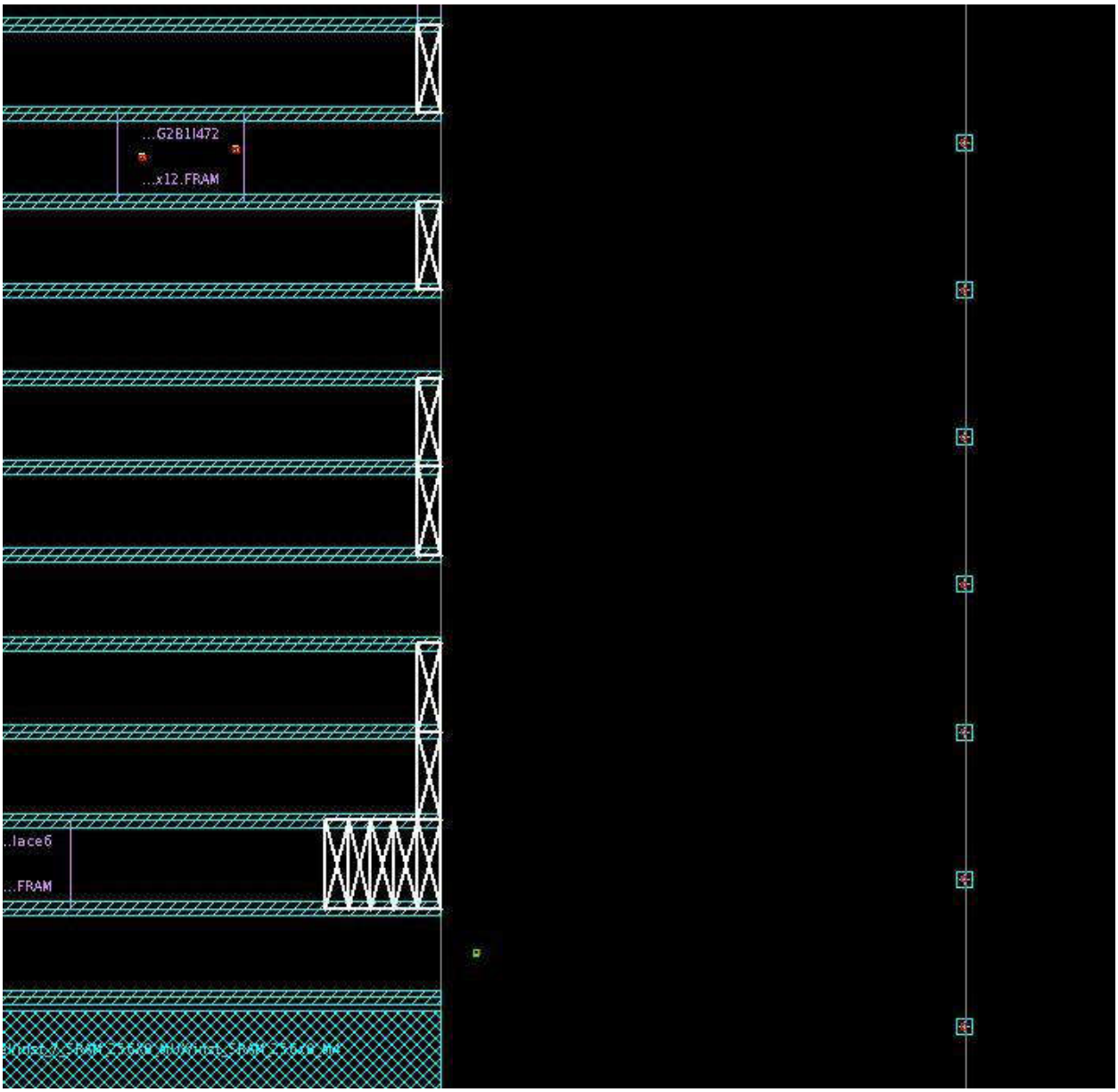

Figure 37: Port Protection Diodes

7 -Design For Manufacturability

Finding and Fixing Antenna Violations

In chip manufacturing, gate oxide can be easily damaged by electrostatic discharge. The static charge that is collected on wires during multilevel metallization process can damage the device or lead to a total chip failure. The phenomenon of an electrostatic charge being discharged into the gate oxide is referred to as either antenna or charge collecting antenna problems.

Charges collected on metal connecting to the gate can create a significant electrical fields across the gate oxide. This is called antenna effect. Antenna design rule: specify the maximum ratio of metal area to gate area such that charge on the metal will not damage the gate. So, to do it one technique is to do Metal Jumpering.

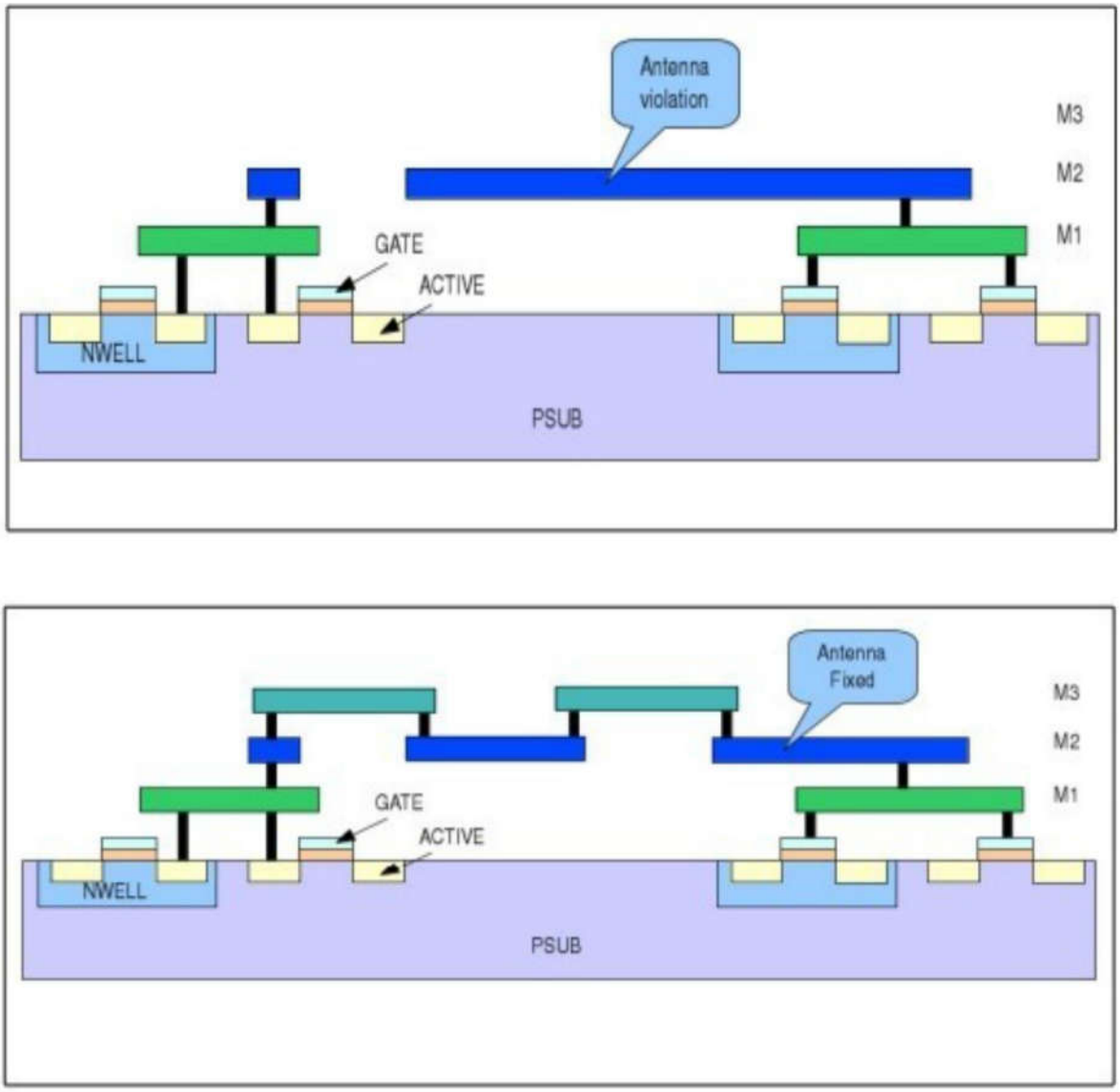

Figure 48 : Antenna Violations fixing by metal Jumpers

8 -Physical Verification

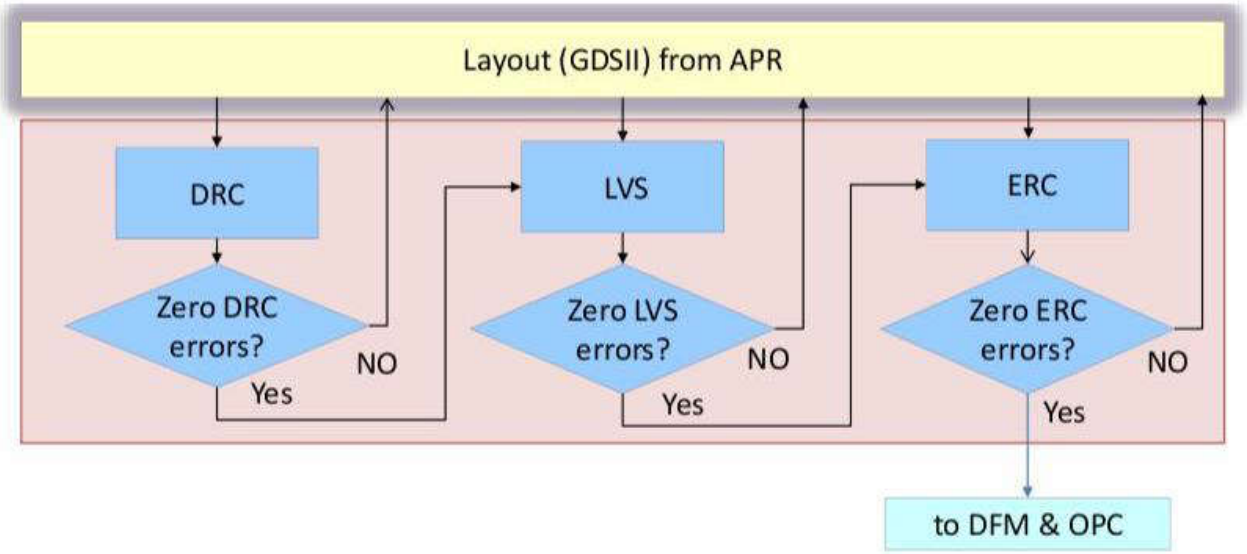

Figure 55: Physical Verification Flow

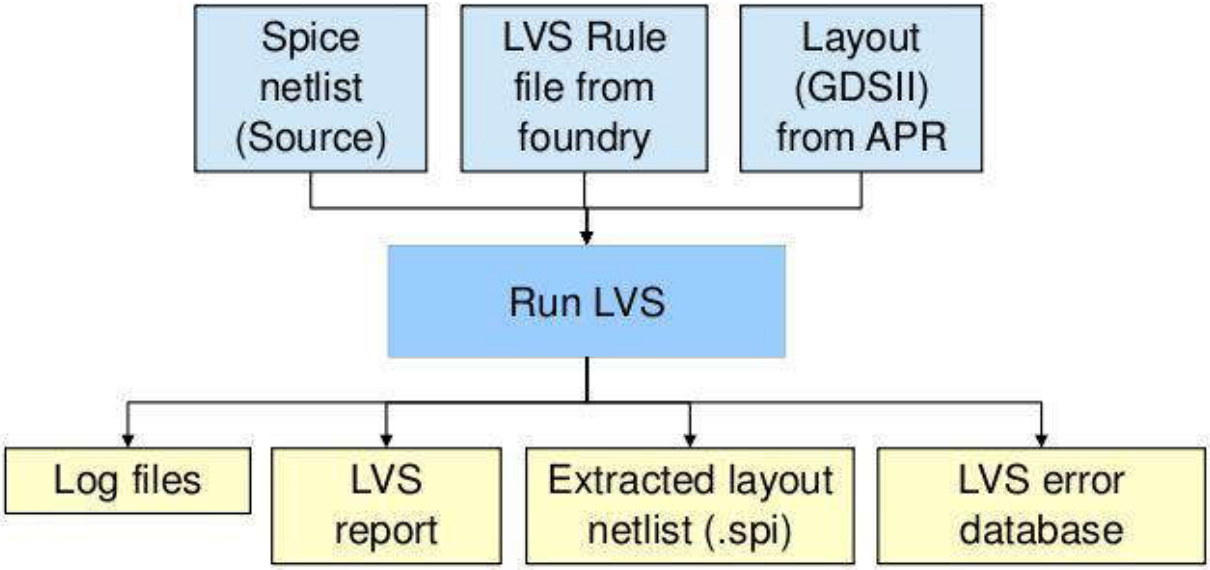

Figure 46: I/P and O/P of LVS

Design Rule Check

Design rules are series of parameters provided by semiconductor manufactures that enable the designer to verify the correctness of a mask set. Design rules are specific to a manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account variability during manufacturing process so that most of the design parts work correctly. In PD, we can check only subset of rules there in DRC rule deck, these subset of rules are related tp metal layers and vias. The rules are present in technology file. The rules include minimum spacing, minimum area, minimum width etc. A sample DRC error related to minimum area on an unconnected port, we encountered in our block is shown below.

Layout vs Schematic

A successful design rule check ensures the layout confirms to the rules required for faultless fabrication. However it does not guarantee that it is the correct circuit you desire to fabricate.This is where an LVS check is used.

Floating Port: Due to missing port in netlist.

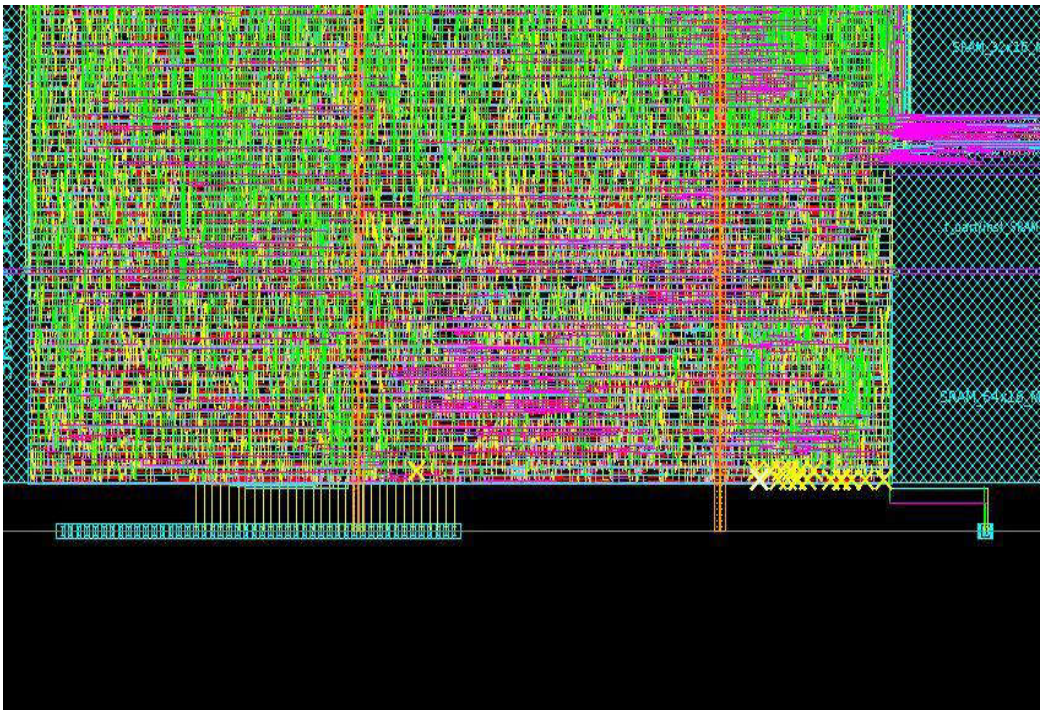

Figure (a): Floating Pins

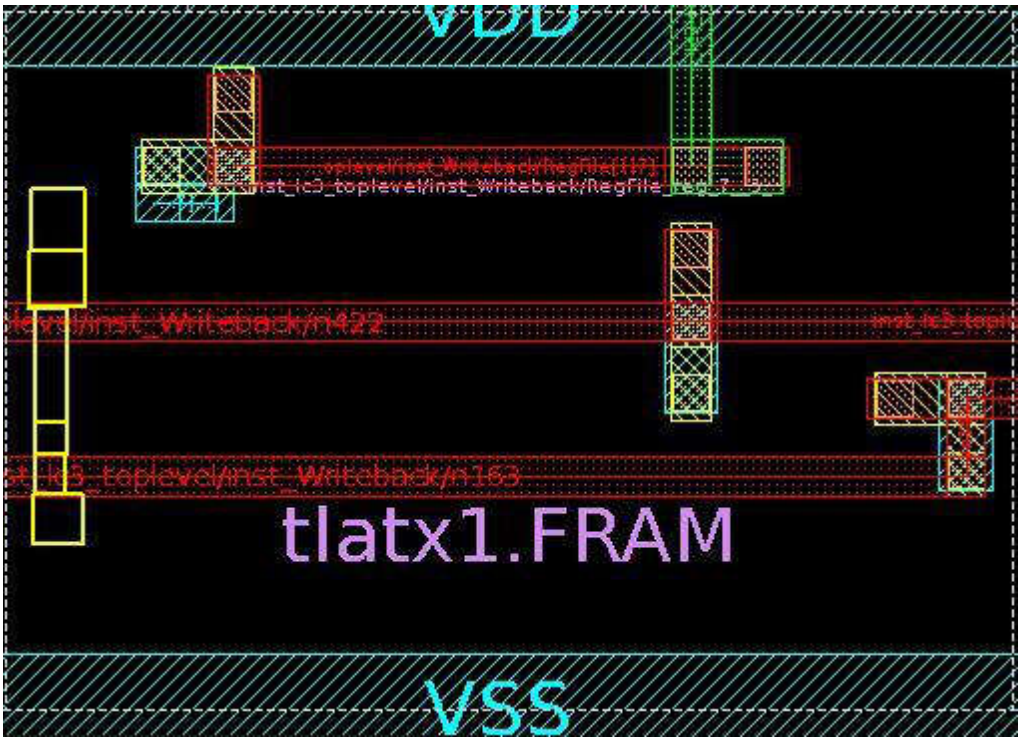

Figure (b): Floating Pins

2) **Min Area:** Due to missing port in netlist.

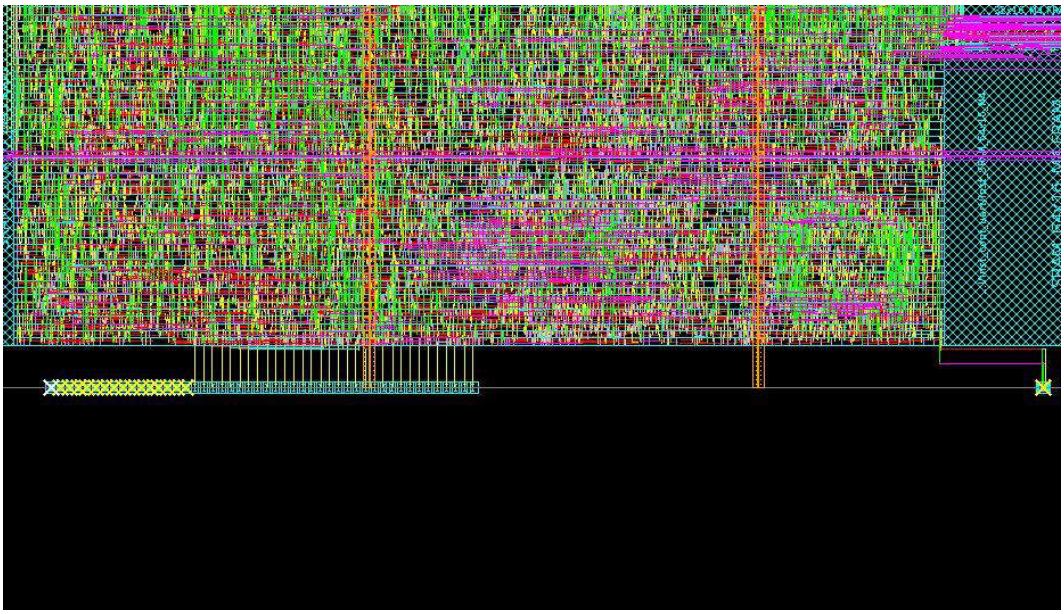

Figure : Min Area

3) open:

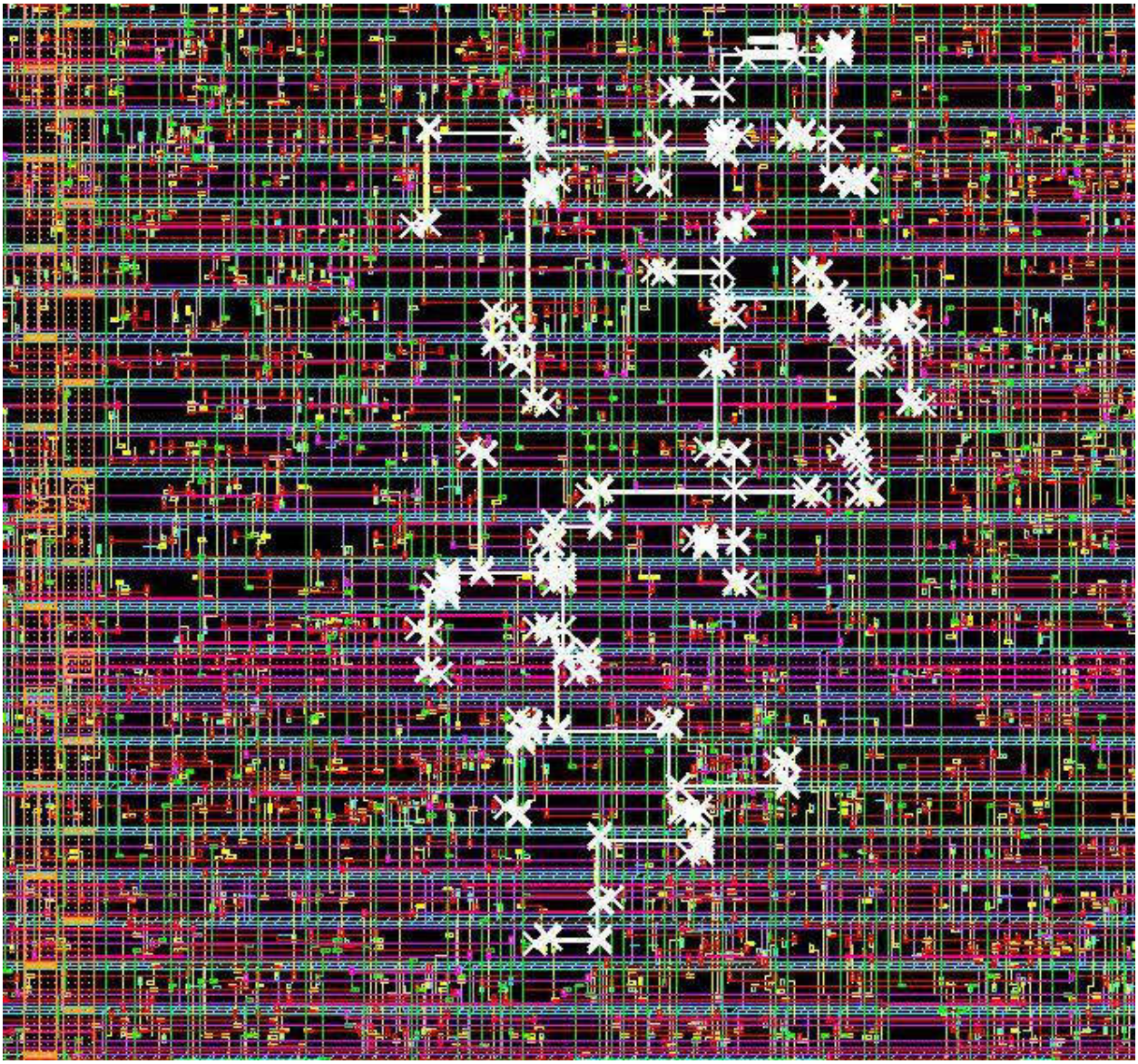

Figure : Open

3) Short:

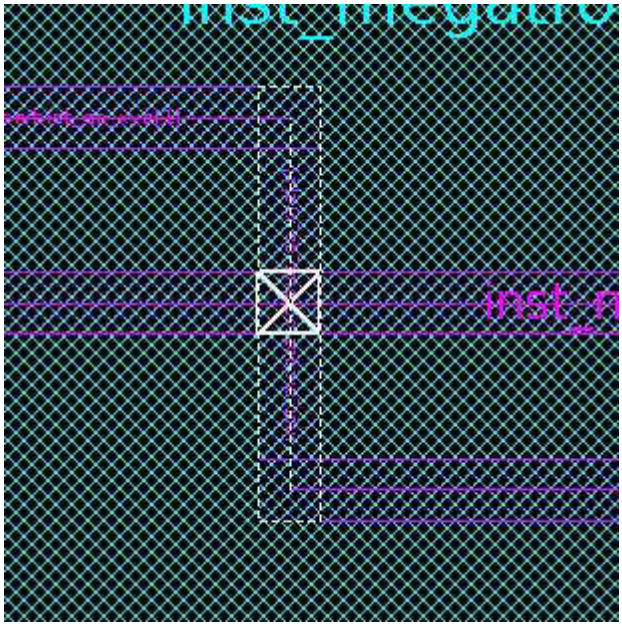

Figure: Short

9 -Sign-off STA

IC Compiler is an implementation engine, Star RC and Prime Time are sign off engines. In general, the implementation engine and the sign-off engine are well correlated with each other. However, small variations can occur because of the following:

• Prime Time and Star RC - as sign-off tools, are more accurate.

• Prime Time has reduced Signal Integrity pessimism.

• IC Compiler might have implementation margin

• IC Compiler might have fewer corners

These differences can cause timing violations during final sign-off. Prime Time supports the use of timing models to represent chip sub -modules. A timing model contains information about the timing characteristics, but not the logical functionality of a sub-module.

Prime Time can generate a timing model from a sub-module netlist , and then use that model in place of the original netlist for timing analysis at higher levels of hierarchy. This technique makes whole chip analysis run much faster.

To perform stage delay calculation accurately and efficiently, PrimeTime uses models to represent the driver, RC Network and capacitive load on the net. An ideal model would produce exactly the same delays and slews as a SPICE simulation at the output of the driver and at the input of each receiver.

To perform Static Timing Analysis, Prime Time must accurately calculate the delay and slew (transition time) at each stage of each timing path. A stage consists of a driving cell, the annotated RC network at the output of the cell and the capacitive load of the network load pins. The goal is to compute the response at the driver output and at the network load pins, given the input slew or waveform at the driver input using the least amount of runtime necessary to get accurate results.

The driver model is intended to reproduce the response of the driving cell's underlying transistor circuitry when connected to an arbitrary RC network given for a specific input slew. The reduced order network model is a simplified representation of the full annotated network that has really the same response characteristics as the original network.

Prime Time uses the Arnoldi reduction method to create this model.

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