Design of Complementary Dual Modular Redundancy Dynamic Memory for Space Applications

Bandi Siva Sankara Reddy[1], H Devanna[2]

[1]PG Scholar, Dept. of ECE, St.Johns College of Engineering & Technology, Yemmiganur, A.P.

[2]Associate Professor, Dept. of ECE, St.Johns College of Engineering & Technology, Yemmiganur, A.P.

ABSTRACT: The effect of charged particles in space environment will deteriorates the performance of space domain applications such as space crafts and satellites by altering the output which directly affects the system's reliability. So, there is a need of the reliable system that can withstand to such particle strikes. In this paper we proposed the smallest solution for soft errors in space application memory modules by using complementary dual modular redundancy (CDMR) with dynamic memory. The proposed CDMR consists of four transistors (4-T) for signal memory unit and addition of low-overhead parity, an error correction capability of architecture for robust soft error protection. The proposed work of this paper implemented in 45nm CMOS technology and implemented 4-T Complementary Dual modular redundancy dynamic memory, and offers smaller silicon footprint and lower power consumption when compared to other radiation hardened system.

Index Terms: complementary dual modular redundancy (CDMR), soft errors, dynamic memory, radiation hardening, space applications.

I. INRODUCTION

The space environment comprises cosmic ray particles, heavy ions and high energy electrons and protons. The charged particles can hit the ICs resulting in non-destructive or destructive effects according to the charge intensity and to the hit location. Microelectronic circuits used in space applications such as satellites and space stations are prone to upsets induced by these particles. With transistor dimensions shrinking due to continued scaling, terrestrial integrated circuits are also increasingly susceptible to radiation upsets. Hence radiation hardening is a requirement for microelectronic circuits used in both space and terrestrial applications. The Radiation effect problems in space applications can be tackled by using radiation hardened devices. In most of the spacecraft and satellites, the need for integration of an increased number of application- specific integrated circuit(ASIC) and field-programmable gate array(FPGA) components is raised that can be operated reliably within high-radiation environments. One of the primary components of ASICs and FPGAs is static random-access memories(SRAMs). In accordance with Moore's Law, the size, density, and power consumption of SRAMs has grown exponentially over the past five decades, often being responsible for over 50% of the total area and static power consumption of modern ASICs. The large area of SRAMs makes them highly susceptible to particle strikes, which are common in high-radiation environments, such as space. Furthermore, modern ASICs are often operated at scaled supply voltages in order to reduce their power consumption. This further reduces the noise margins of SRAMs and significantly increases their susceptibility to radiation effects, such as soft errors caused by single event upsets (SEUs).

A soft error leads to transient error(s), which can last for one or several clock cycles. A single event transient (SET) occurs when a charged particle hits the combinational logic resulting in a transient current pulse. If this transient has enough width and magnitude, it can

result in an erroneous value at the gate output. If the erroneous value is latched at a memory element, an SET becomes a single event upset (SEU). An SEU is a change of state in a flip-flop or memory cell caused by charged particles striking a sensitive node in an integrated circuit device, potentially causing system failure. SEUs occur when an energetic particle passes through a silicon substrate and its energy is transferred to the creation of electron–hole pairs along its path. When such a particle hits a reversed-biased junction inside the storage node of a memory circuit, the resulting transient current pulse can inject enough charge into the junction to cause a data flip. In this paper, a dynamic memory core based on Gain Cell-embedded DRAM (GC-eDRAM) is proposed that by nature is more susceptible to soft errors than a static memory cell. However, the reduced transistor count and the physical properties of the dynamic circuit allow us to internally apply complementary DMR (CDMR) to achieve inherent per-bit error detection. In addition, the simple addition of parity provides error correction capabilities at a much lower overhead than the traditional Error Correction Codes(ECC)-based approaches. The proposed 4-T CDMR memory was implemented in a low- power 45-nm CMOS process, consuming less area than any other previously proposed soft-error tolerant memory cell. The resulting cell is 53% smaller than a conventional non radiation hardened 6-T SRAM bit cell, and consumes up to 8x less static power than any other reported rad-hard solution. The proposed system can be used in space applications, such as satellites, probes, shuttles and others widely use microelectronic devices.

II. RELATED WORK

[1] "Technology scaling and soft error reliability", Lloyd W. Massengill, Bharat L. Bhuva, W. Timothy Holman, Michael L. Ales, Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashvile, TN, USA- depicts the influence of ionizing radiation on the proper operation of integrated electronics has been a phenomenon of concern, observation, and consequence. In those early days, the study of 'ionizing radiation effects' enjoyed widespread conversation in the aerospace community, where the extremely energetic particles found in orbital and flight-altitude environments wreaked havoc with sensitive integrated electronics. At that time, terrestrial electronics were not significantly troubled by ionizing radiation, with the exception in the 1980's of a brief bout with alpha particle emissions from IC packaging contaminants – a problem directly solved by eliminating the troublemaking impurities.

[2] "Soft error in advanced computer systems", R. Baumann, Silicon technol. Dev. Component Reliability Group, Texas Instrum.Inc., Dallas, TX, USA - As the dimensions and operating voltages of computer electronics shrink to satisfy consumers' insatiable demand for higher density, greater functionality, and lower power consumption, sensitivity to radiation increases dramatically. In terrestrial applications, the predominant radiation issue is the soft error, whereby a single radiation event causes a data bit stored in a device to be corrupted until new data is written to that device. This article comprehensively analyzes soft-error sensitivity in modern systems and shows it to be application dependent. The discussion covers ground-level radiation mechanisms that have the most serious impact on circuit operation along with the effect of technology scaling on soft-error rates in memory and logic.

[3] "A 65nm 32 b Sub-Threshold Processor with 9T Multi-Vt SRAM and Adaptive Supply Voltage Control", Sven lutkemeier, Thorsten jungeblut, Center of Excellence Cognitive Interaction Technology, Cognitronics& Sensor

Systems, Bielefeld University, Bielefeld, Germany. An energy-efficient SOC with 32 b sub threshold RISC processor cores, 32kB conventional cache memory, and 9T ultra-low voltage (ULV) SRAM based on a flexible and extensible architecture was fabricated on a 2.7 mm 2 test chip in 65 nm low power CMOS. The processor cores are based on a custom standard cell library that was designed using a multi objective approach to optimize noise margins, switching energy, and propagation delay simultaneously. The cores operate over a supply voltage range from 200 mV (best samples) to 1.2 V with clock frequencies from 10 kHz to 94 MHz at room temperature.

III. EXISTING SYSTEM

The conventional 6-T SRAM memory cell, shown in the inset of Fig. 1, utilizes an active feedback loop between cross- coupled inverters (M1/M3 and M4/M6) in order to retain its stored data value. This circuit is very sensitive to SEUs, as any upset that causes one of the data nodes to cross the switching threshold of the adjacent inverter will result in a bit flip. An example of such an occurrence is illustrated in Fig. 1, showing a particle striking the drain of one of the nMOS pull- down devices of a 6-T SRAM bitcell (M4, in the inset). If the particle injects sufficient charge to drive the voltage at the QB node past the switching threshold of the opposite inverter (M1/M3), the feedback loop will drive the storage state of the SRAM cell to the opposite level, as shown in the illustrative waveforms.

The failure risk, described above, increases with process scaling, since the critical charge of the memory cell decreases, resulting in higher soft error rates (SERs). Furthermore, static noise margins decrease significantly, and therefore the memory cell is more susceptible to read and write errors.

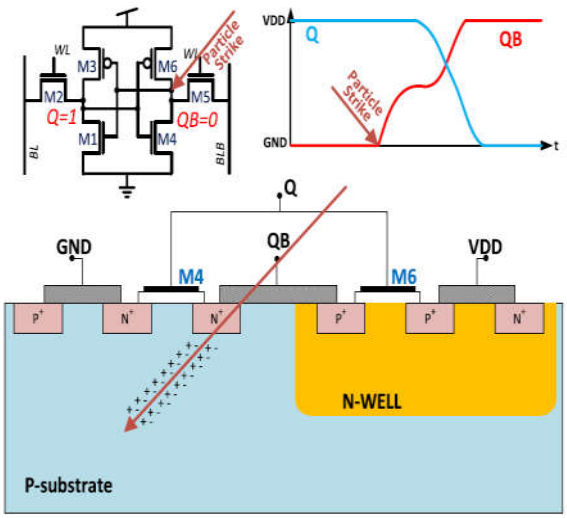

Fig.1. Particle strike hitting a silicon substrate junction, releasing electron– hole pairs, and causing a state flip in an SRAM cell.

In addition, when operating at low voltages for power reduction, the aforementioned switching threshold decreases, thereby increasing the error susceptibility of the circuit. These issues have led to the need for the development of SEU-aware SRAM design approaches for radiation-hardening.

The main approach to error mitigation over the past two decades has been to provide full immunity to errors through circuit redundancy. By simply adding a parity bit to a given number of bits, a single error can be detected with very little overhead. For enhanced protection, Error Correction Codes (ECCs) can be used to detect and correct multiple errors. However, the error detection and correction capabilities of such codes is directly correlated with the complexity and area overheads required for their implementation. For complete protection under the assumption that the probability of an error at two separate places on the chip within a defined timespan is extremely low, TMR replicates each storage node thrice and uses a majority gate to determine the correct value. While TMR is a simple and robust

solution, it incurs an increase in both area and power of over 3 times. Therefore the primary goal of the proposed technique is to increase the critical charge, Q_{crit} of the cell, and thereby improve their resilience to SEUs.

Disadvantages:

- Reliability is low
- More power consumption.
- More area size

IV. PROPOSED 4-T CDMR DYNAMIC MEMORY ARRAY

The problem which encountered in conventional SRAM cell is the positive feedback between the two internal storage nodes which leads to enable an SEU to flip the data. While this feedback is the means by which the static storage capabilities of the circuit are acquired, in the case of SERs, it is also the cell's vulnerability. Any voltage shift that causes one of the storage nodes to cross the switching threshold of the adjacent inverter will immediately be latched by the positive feedback, resulting in a catastrophic bit flip. Such a voltage shift can be quantified according to the charge transferred by the striking particle, and therefore, the critical charge metric is used to characterize the susceptibility of circuit-level solutions to SEUs. If a particle strike induces charge lower than the Q_{crit} of the circuit, the storage value will remain intact; however, if Q_{crit} is exceeded, a failure will occur.

While SRAM is the primary technology used to implement embedded memory arrays, another popular storage topology is eDRAM. GC-eDRAM is a fully logic-compatible implemen- tation of eDRAM, which provides a reduced silicon footprint compared with SRAM, but lacks the internal feedback that ensures strong storage levels, in spite of deteriorating leakage currents. Intuitively, such a topology is much more susceptible to SERs, as the circuit lacks any mechanism to mitigate a level change induced by a particle strike. However, we propose to employ CDMR, i.e., for each bit, to store both the data value and its inverse. Based on this concept, SEUs in the memory array can be both detected and corrected, while still achieving the low area and power aspirations of the target applications.

A. ARCHITECTURE

The proposed CDMR approach is implemented with the 4-T dynamic memory bitcell, illustrated in Fig.2. The circuit consists of two write transistors (MW1 and MW2), two read transistors (MR1 and MR2), and two storage nodes (SN and SNB). The data and its complementary values are stored on the parasitic capacitances at the storage nodes, comprising the gate capacitance of MR1/MR2 and the diffusion capacitance of MW1/MW2, respectively. Writing to the cell is performed by driving the write word line (to a negative voltage and passing the data and its complementary level from the write bit lines (WBL and WBLB) to SN and SNB, respectively. Readout is performed by pre-discharging the read bit lines (RBL and RBLB) to Ground and driving the read word line to V_{DD}, thereby charging RBL/RBLB only if SN/SNB holds a data '0.' The RBL/RBLB of each column is connected to a sensing circuit, which can be implemented with a simple inverter, in order to output the digital levels of the data and its complementary level stored in the selected cell.

During normal operation, the output of a read operation from a single bitcell will provide two opposite levels. If an SRAM cell is exposed to a particle strike surpassing the Q_{crit} of one of the storage nodes, the feedback will cause the complementary node to flip, as well, latching the erroneous value.

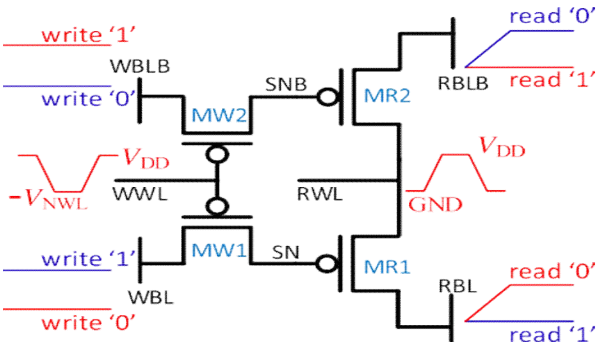

Fig.2. Schematic of the proposed 4-T gain cell.

However, since the proposed memory structure lacks a similar internal feedback mechanism, the complementary storage nodes are affected separately by a particle strike. In the case of a particle changing the data in one of the storage nodes, the complementary node will remain unaffected and both the nodes will store the same data level. Moreover, due to the choice of an all-pMOS implementation of the proposed bitcell, only a '0' to '1' upset can occur, resulting in both the data (SN) and its complementary value (SNB) storing a '1' following such an upset. Therefore, by integrating a single AND gate on the readout path of every column of the array, the outputs are compared and an error can be detected in any given bit.

By itself, the CDMR characteristic of the proposed topology provides a reduced area bitcell implementation with inherent multiple-bit error detection capabilities. However, while the location of the error is known, it is not inherently clear if the data or its complementary value was corrupted, as both of the values will store a logic '1.' This prevents the straight- forward correction of the error, but by simply adding a parity bit to each set of bits, such an error-correction capability can be provided. The parity bit for every set of *N* bits is written during write access to the memory and indicates whether the number of ones in the written set of bits is even or odd. If the parity is maintained despite the error, the complementary value (SNB in Fig. 2) of the erroneous bit has been corrupted and should be corrected, while if the parity is incorrect, the SN value should be corrected.

B. SEQUENTIAL DIAGRAM DEPICTION

A Sequential diagram professing the error detection and correction design is shown in Fig. early, an *N*-bit word (DI) and its reciprocal (DIB) are written to the input write address. In aligned, the parity of DI is calculated and stored in the memory array. Following some period of retention, the desired word in the array is read, outputting the data (DO) and its reciprocal value (DOB). These two values are bitwise distinguished, and if any of the bits are proportionate, an error has occurred, and a device checks the parity of the DO vector against the stored parity bit.

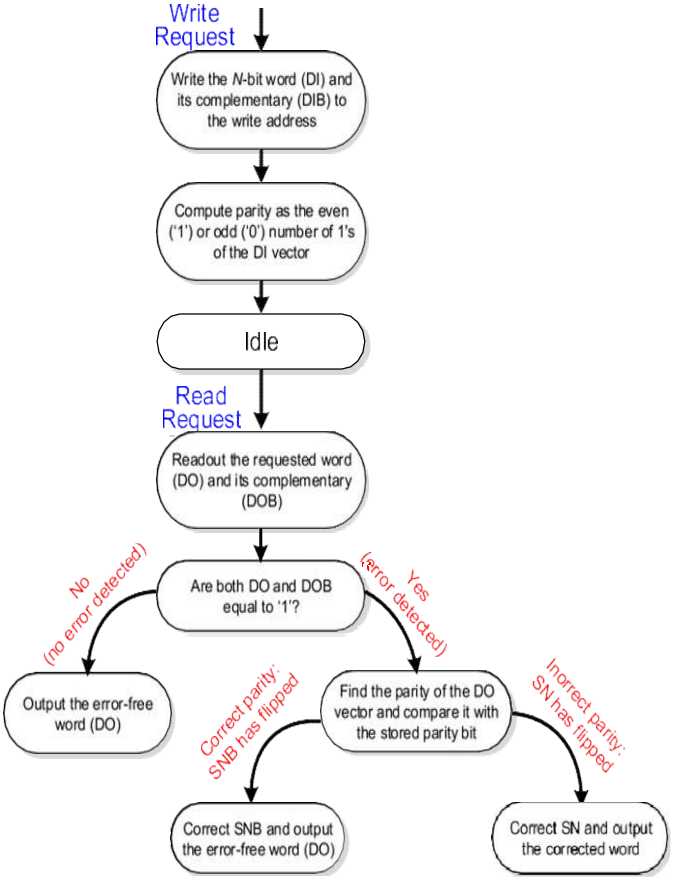

Fig.3. Flowchart illustrating the error detection and correction algorithm.

If the parity is constructing to be correct, the SNB of the erroneous bit has flipped, while if the parity is correct, the SN value is incorrect.

The erroneous data are then corrected to provide an error-free output. Note that the recommended error correction scheme with a single parity bit for an *N*-bit word does not handle to multiple bit upsets, which can be persuaded through highly forceful cosmic ray particles developing in a parasitic bipolar conduction, conceivably flipping numerous bits in a single well. To account for more than one error per every set of bits that includes parity, bit interleaving techniques can be used. However, for single-ended readout storage architectures, half-select susceptibility is a problem that must be addressed, if column multiplexing or byte masking is required. This can easily be solved by either writing entire words at a time, or by performing a read-modify-write operation, when byte masking is required. In addition, parity can be applied to every $k < N$ bits for additional protection.

C. Single Event Upset (SEU) Tolerance

Cell operation under SEUs is demonstrated in Fig. 4, showing consecutive write, upset, and read events for data '1' and '0' with a 400 mV supply voltage, which is suitable for low-power applications, often operating in the sub-threshold domain. The SEU was modeled by connecting a current source to the SN node of the bitcell and applying a double-exponential current pulse during the standby states of the cell. The physical composition of the cell only allows a positively charged upset, and therefore, in the example, only this type of particle strike is shown.

On the one hand, in the first demonstrated strike, the cell is storing a '1,' and the positive charge only strengthens the stored level, leaving RBL discharged during readout and not leading to an error.

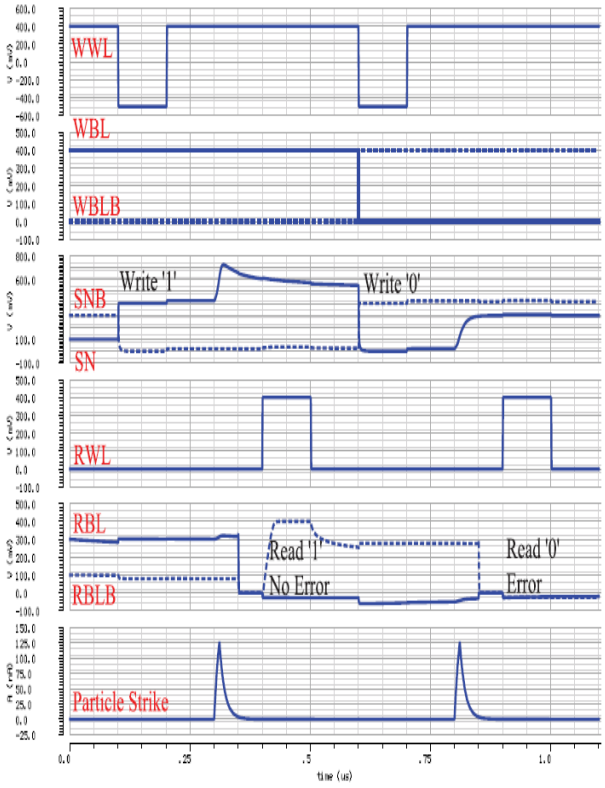

Fig.4. Waveform demonstration of write-upset-read events

On the other hand, when data '0' is stored, the applied pulse causes an increase in the voltage level stored at SN, causing the RBL to erroneously charge during readout. Since the complementary value, stored in SNB, is also a data '1,' both RBL and RBLB provide logic '1' at the output, indicating that an error has occurred. In addition, the parity will no longer be correct, which implies that the error occurred in the SN of the erroneous bit, and therefore, this node should be pulled back down to '0' to correct the error.

V. SIMULATION RESULTS

The proposed CDMR 4T implemented in a low-power 45-nm CMOS technology and designed and simulated in Tanner EDA Tool.

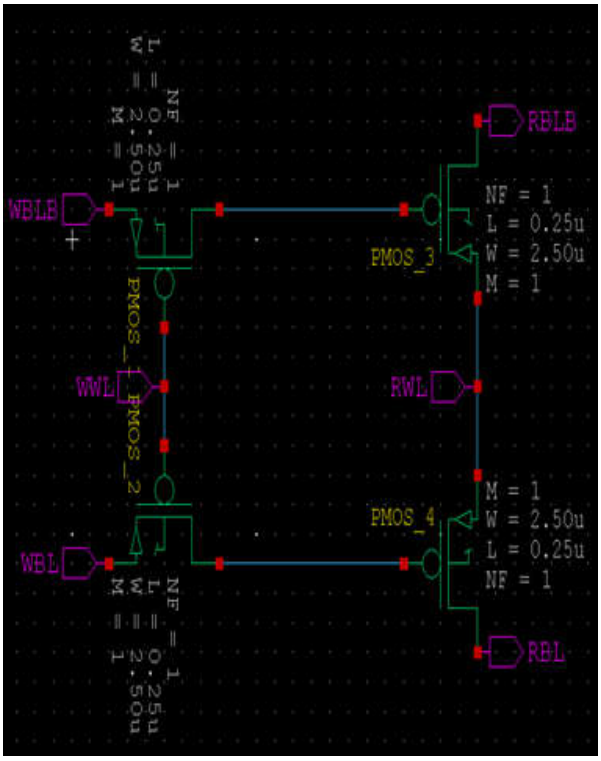

Fig.5. Schematic of CDMR-4T

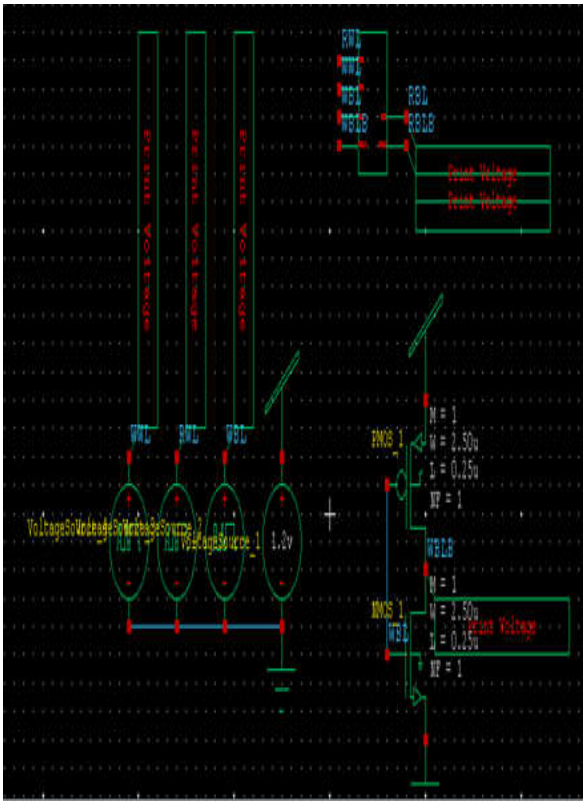

Fig.6. Testbench of CDMR-4T

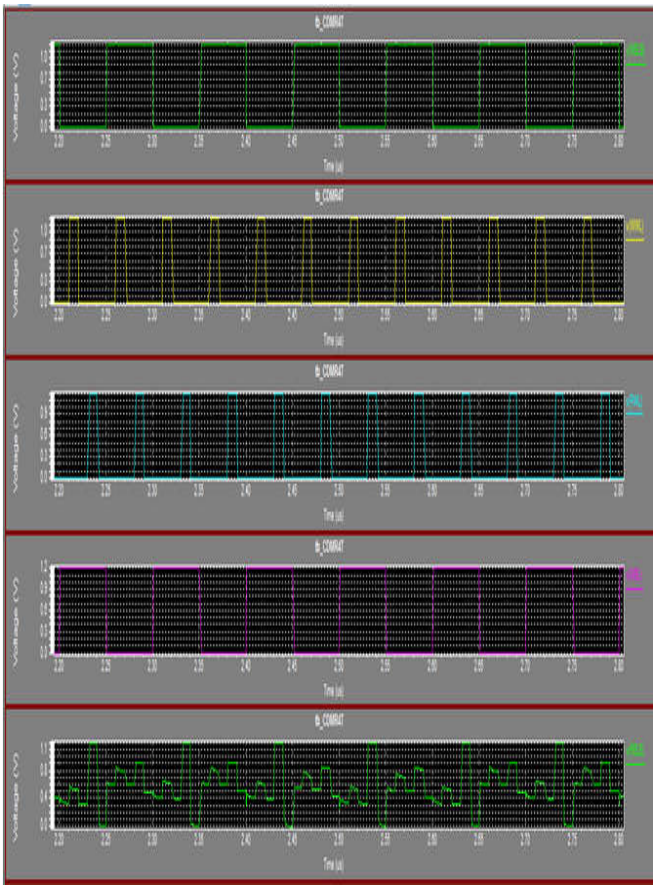

Fig.7. Output waveforms of CDMR-4T

```
* BEGIN NON-GRAPHICAL DATA

Power Results
VVoltageSource_1 from time 0 to 5e-006
Average power consumed -> 5.098164e-007 watts
Max power 5.435330e-005 at time 4.651e-006
Min power 3.446741e-014 at time 1.90983e-006


* END NON-GRAPHICAL DATA
*

* Parsing                        0.02 seconds
* Setup                          0.11 seconds
* DC operating point             0.01 seconds
* Transient Analysis             0.27 seconds
* Overhead                       1.44 seconds
* ---------------------------------------------
* Total                          1.85 seconds

* Simulation completed      with  2 Warnings

* End of T-Spice output file
```

Fig.8. Power Report of CDMR-4T

Comparison Table:

	CDMR-6T	CDMR -4T
Technology	65nm CMOS	45nm CMOS
Power	1.47µW	0.509µW

VI. CONCLUSION

Here, we presented a dynamic memory-based solution, lacking internal feedback, which utilizes CDMR and single-bit parity to achieve per-bit error detection and correction capabilities. To decrease soft error tolerance, the traditional attempt required to flip a cross-coupled feedback mechanism to increase the critical charge. The proposed work is designed for space bound applications by achieving the soft-error tolerance in embedded memory arrays and implemented using 45nm CMOS technology. The proposed work offers smaller silicon footprint than the conventional radiation hardened Bit-cell systems. When comparing with existing system, the proposed work provides effectiveness in reducing soft errors by consuming less power.

VII. REFERENCES

[1] L. W. Massengill, B. L. Bhuva, W. T. Holman, M. L. Alles, and T. D. Loveless, "Technology scaling and soft error reliability," in Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Apr. 2012, pp. 3C.1.1–3C.1.7.

[2] R. C. Baumann, "Soft errors in advanced computer systems," IEEE Des. Test Comput., vol. 22, no. 3, pp. 258–266, May/Jun. 2005.

[3] S. Lutkemeier, T. Jungeblut, H. K. O. Berge, S. Aunet, M. Porrmann, and U. Ruckert, "A 65 nm 32 b subthreshold processor with 9T multi-Vt SRAM and adaptive supply voltage control," IEEE J. SolidState Circuits, vol. 48, no. 1, pp. 8–19, Jan. 2013.

[4] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," IEEE Trans. Electron Devices, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[5] L. Atias, A. Teman, and A. Fish, "Single event upset mitigation in low power SRAM design," in Proc. IEEE Conv. Elect. Electron. Eng. Israel (IEEEI), Dec. 2014, pp. 1–5.

[6] M. A. Bajura et al., "Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs," IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 935–945, Aug. 2007.

[7] J. Maiz, S. Hareland, K. Zhang, and P. Armstrong, "Characterization of multi-bit soft error events in advanced SRAMs," in IEDM Tech. Dig., 2003, pp. 21.4.1–21.4.4.

[8] J. Teifel, "Self-voting dual-modular-redundancy circuits for singleevent-transient mitigation," IEEE Trans. Nucl. Sci., vol. 55, no. 6, pp. 3435–3439, Dec. 2008.

[9] L. Sterpone and M. Violante, "Analysis of the robustness of the TMR architecture in SRAM-based FPGAs," IEEE Trans. Nucl. Sci., vol. 52, no. 5, pp. 1545–1549, Oct. 2005.

[10] K. C. Mohr and L. T. Clark, "Delay and area efficient first-level cache soft error detection and correction," in Proc. Int. Conf. Comput. Design (ICCD), Oct. 2006, pp. 88–92.

[11] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[12] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3768–3773, Dec. 2009.

[13] O. Chertkow, A. Pescovsky, L. Atias, and A. Fish, "A novel low power bitcell design featuring inherent SEU prevention and self

correction capabilities," J. Low Power Electron. Appl., vol. 5, no. 2, pp. 130–150, 2015.

[14] L. T. Clark, D. W. Patterson, N. D. Hindman, K. E. Holbert, S. Maurya, and S. M. Guertin, "A dual mode redundant approach for microprocessor soft error hardness," IEEE Trans. Nucl. Sci., vol. 58, no. 6, pp. 3018–3025, Dec. 2011.

[15] V. Vashishtha, L. T. Clark, S. Chellappa, A. R. Gogulamudi, A. Gujja, and C. Farnsworth, "A soft-error hardened process portable embedded microprocessor," in Proc. IEEE Int. Custom Integr. Circuits Conf. (CICC), Sep. 2015, pp. 1–4.

[16] J. Karp, W. Regitz, and S. Chou, "A 4096-bit dynamic MOS RAM," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), vol. 15. Feb. 1972, pp. 10–11.

[17] N. Ikeda, T. Terano, H. Moriya, T. Emori, and T. Kobayashi, "A novel logic compatible gain cell with two transistors and one capacitor," in Symp. VLSI Technol. Dig. Tech. Papers., 2000, pp. 168–169.

[18]W. K. Luk and R. H. Dennard, "A novel dynamic memory cell with internal voltage gain," *IEEE J. Solid-State Circuits*, vol. 40, no. 4,PP.884–894, Apr. 2005.

[19]K. C. Chun, P. Jain, T.-H. Kim, and C. H. Kim, "A 667 MHz logic-compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," *IEEE J. Solid-State Circuits*, vol. 47, no. 2,PP.547–559, Feb. 2012.

[20]R. Giterman, A. Teman, P. Meinerzhagen, A. Burg, and A. Fish, "4T gain-cell with internal-feedback for ultra-low retention power at scaled CMOS nodes," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Jun. 2014, pp. 2177–2180.

[21]R. C. Baumann, "Radiation-induced soft errors in advanced semicon-ductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3,pp.305–316, Sep. 2005.

[22]P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[23]B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.

About Authors:

Bandi Siva Sankara Reddy is currently pursuing M.Tech in Dept. of ECE, St.Johns College of Engineering & Technology, Yemmiganur, AP, India.

H. Devanna, Associate Professor in Dept. of ECE, St.Johns College of Engineering & Technology, Yemmiganur, AP, India.